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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

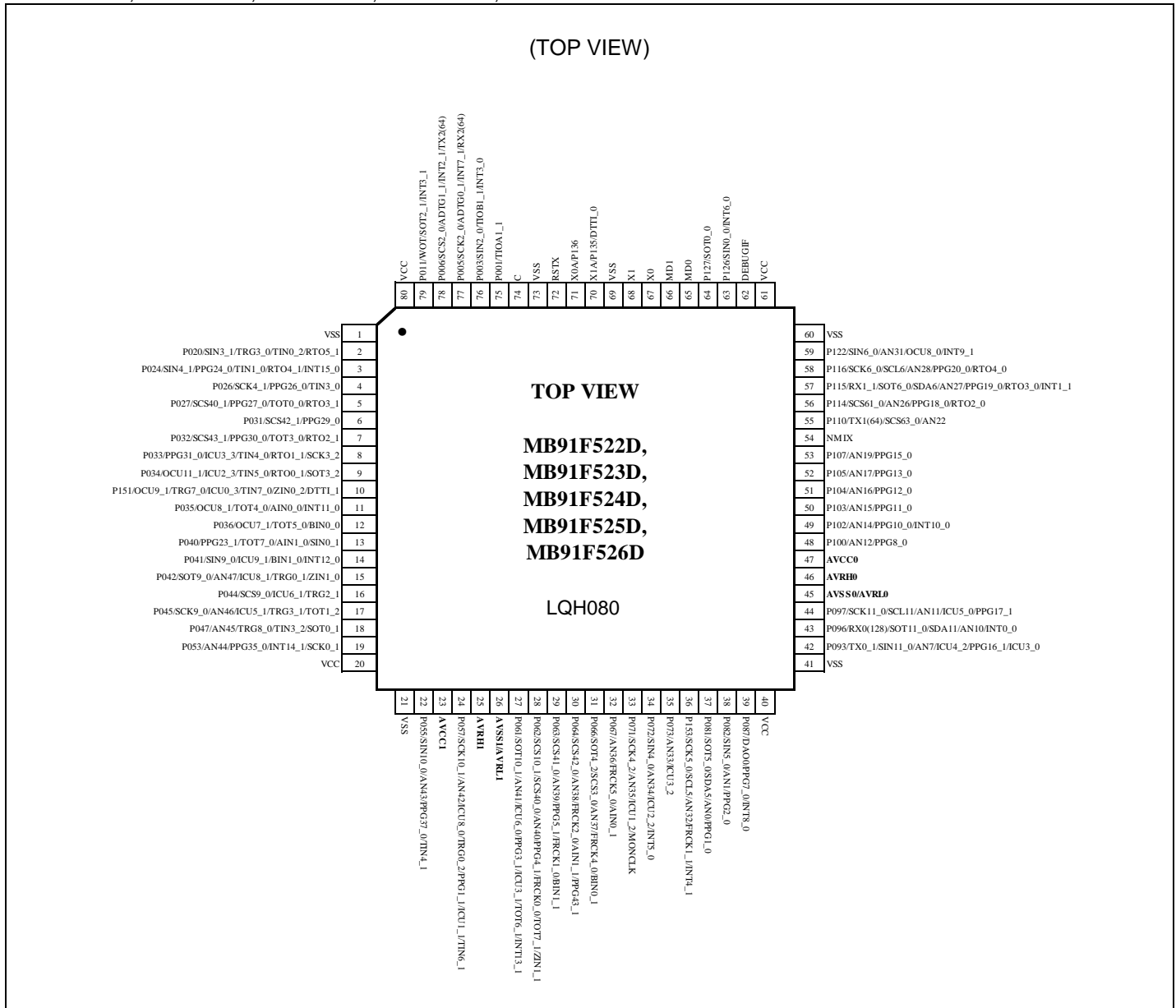
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524fhbpmc-gs-f4e1

MB91F52xD

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D



* In a single clock product, pin 70 and pin 71 are the general-purpose ports.

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
16 *1	19 *1	24 *1	29 *1	34	42	P053	-	B	General-purpose I/O port
						A21 *2, *3, *4, *5	-		External bus/Address bit21 output
						AN44	-		ADC analog 44 input
						PPG35_0	-		PPG ch.35 output (0)
						INT14_1	-		INT14 External interrupt input (1)
						SCK0_1	-		Multi-function serial ch.0 clock I/O (1)
-	-	-	-	35	43	P054	-	A	General-purpose I/O port
						SYSCCLK	-		External bus/System clock output
						PPG36_0	-		PPG ch.36 output (0)
17 *1	22 *1	27 *1	32 *1	38	46	P055	-	G	General-purpose I/O port
						CS2X *2, *3, *4, *5	-		External bus chip select 2 output
						SIN10_0	-		Multi-function serial ch.10 serial data input (0)
						AN43	-		ADC analog 43 input
						PPG37_0	-		PPG ch.37 output (0)
						TIN4_1	-		Reload timer ch.4 event input (1)
-	-	-	-	-	47	P180	-	A	General-purpose I/O port
						PPG40_0	-		PPG ch.40 output (0)
-	-	-	-	-	48	P181	-	A	General-purpose I/O port
						PPG41_0	-		PPG ch.41 output (0)
-	-	-	33 *1	39	49	P056	-	A	General-purpose I/O port
						CS3X *5	-		External bus chip select 3 output
						ICU9_0	-		Input capture ch.9 input (0)
						PPG0_1	-		PPG ch.0 output (1)
						ICU0_1	-		Input capture ch.0 input (1)
						TIN5_1	-		Reload timer ch.5 event input (1)
						DTTI_2	-		Waveform generator ch.0-ch.5 input pin (2)
19 *1	24 *1	29 *1	35 *1	41	51	P057	-	G	General-purpose I/O port
						RDY *2, *3, *4, *5	-		External bus/Ready input (0)
						SCK10_1	-		Multi-function serial ch.10 clock I/O (1)
						AN42	-		ADC analog 42 input
						ICU8_0	-		Input capture ch.8 input (0)
						TRG0_2	-		PPG trigger 0 input (2)
						PPG1_1	-		PPG ch.1 output (1)
						ICU1_1	-		Input capture ch.1 input (1)
						TIN6_1	-		Reload timer ch.6 event input (1)
-	-	-	-	44	54	P142	-	F	General-purpose I/O port
						SCK10_0/ SCL10	-		Multi-function serial ch.10 clock I/O (0)/ I ² C bus serial clock I/O
						PPG38_0	-		PPG ch.38 output (0)
						TIN7_1	-		Reload timer ch.7 event input (1)

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause

absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70 % relative humidity, and at temperatures between 5 °C and 30 °C.
When you open Dry Package that recommends humidity 40 % to 70 % relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40 % and 70 %. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

6. Handling Devices

This section explains the latch-up prevention and pin processing.

■ For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC, AVRH) and analog input must not be exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

■ Treatment of unused pins

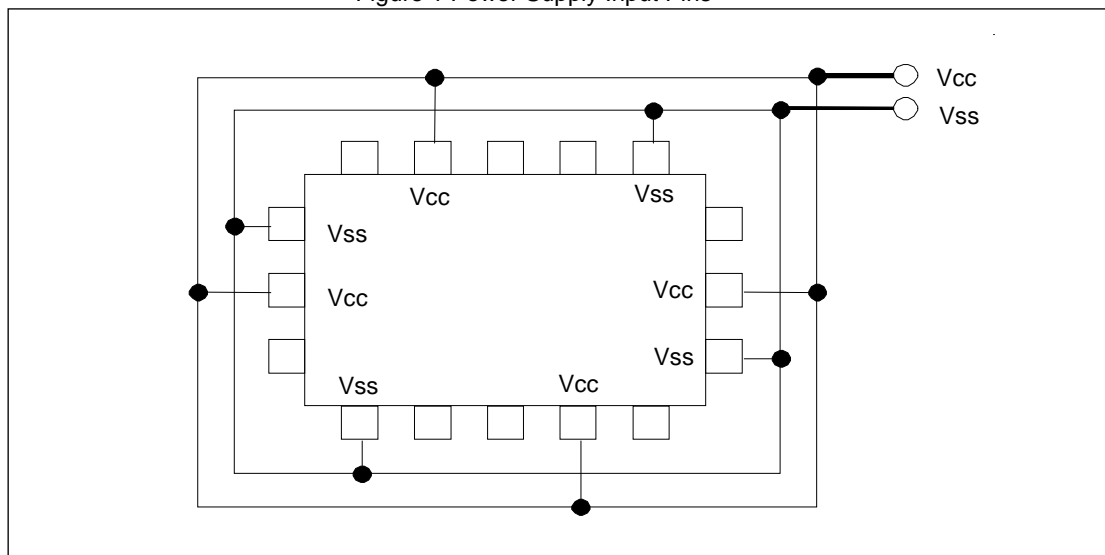
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2 kΩ resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

■ Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

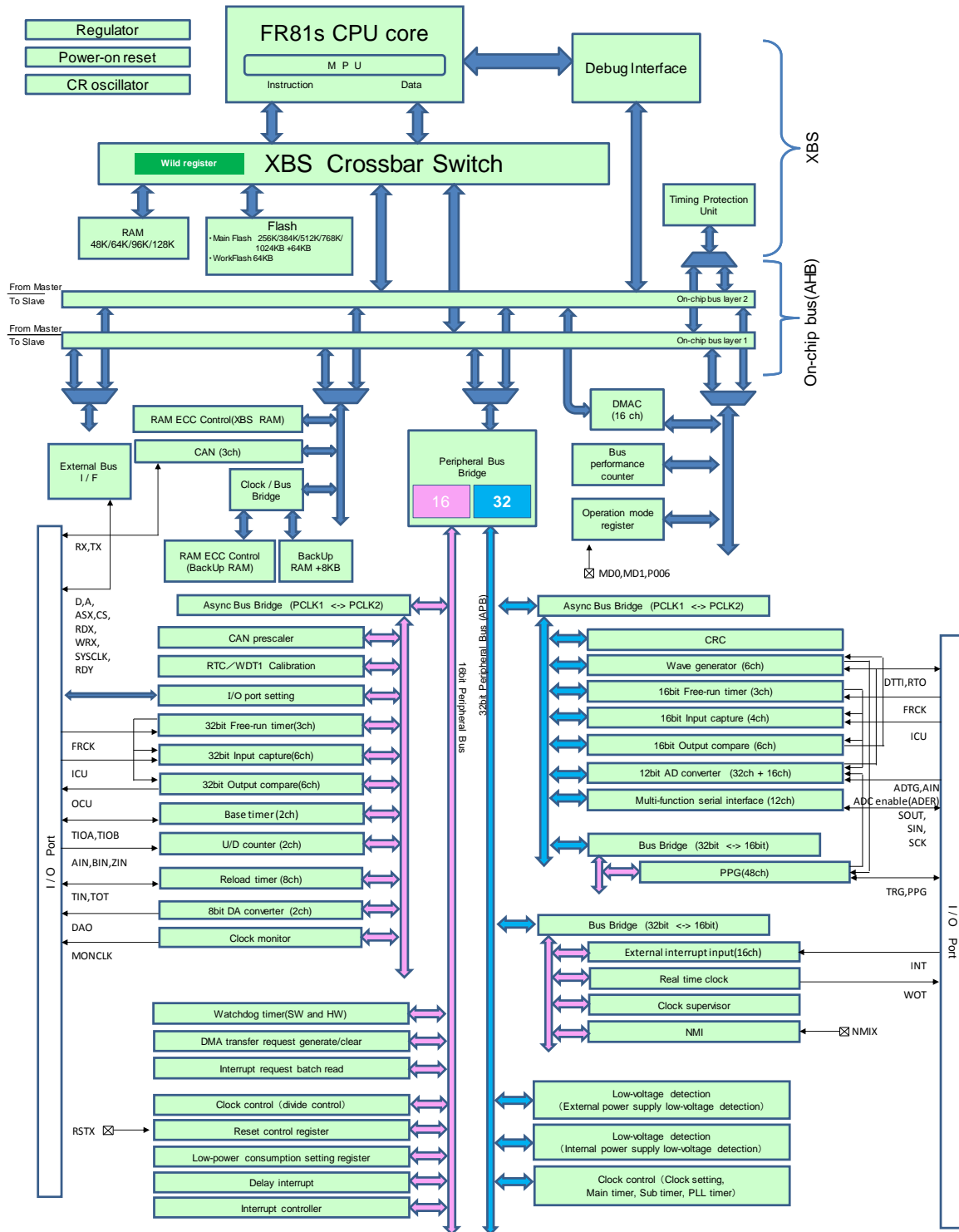
Figure 1 Power Supply Input Pins



The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000258 _H to 0002C0 _H	—	—	—	—	Reserved
0002C4 _H to 0002FC _H	—	—	—	—	Reserved
000300 _H to 00030C _H	—	—	—	—	Reserved
000310 _H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314 _H	—	—	—	—	
000318 _H	—				
00031C _H	—	—	—		
000320 _H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324 _H	—	—	DPVSR [R/W] H ----- 00000--0		
000328 _H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00032C _H	—	—	DESR [R/W] H ----- 00000--0		
000330 _H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334 _H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338 _H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00033C _H	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340 _H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344 _H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348 _H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00034C _H	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350 _H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354 _H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358 _H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035C _H	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360 _H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364 _H	—	—	PACR6 [R/W] H 000000-0 00000--0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000F68 _H	MSCY6 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 Cycle measurement data register 67
000F6C _H	MSCY7 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000F70 _H	RCRH0 [W] H,W XXXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/Down Counter 0
000F74 _H	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000	
000F78 _H to 000F7C _H	—	—	—	—	Reserved
000F80 _H	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/Down Counter 1
000F84 _H	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000	
000F88 _H	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W -----00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45
000F8C _H	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W -----00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
000F90 _H	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU
000F94 _H	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				
000F98 _H	—	—	OCSH1011 [R/W] B,H,W ---0--00	OCSL1011 [R/W] B,H,W 0000--00	Output Compare 10,11 32-bit OCU
000F9C _H	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU1011 Output level control register
000FA0 _H	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT
000FA4 _H	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FA8 _H	TCCSH5 [R/W]B,H,W 0-----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	
000FAC _H to 000FCC _H	—	—	—	—	Reserved
000FD0 _H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 32-bit ICU
000FD4 _H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8 _H	—	—	LSYNS1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001884 _H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W ----- *2	— /(ISBA7)[R/W] B,H,W ----- *2	Multi-UART7
001888 _H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
00188C _H	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890 _H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W]] B,H,W 00000000	Multi-UART8
001894 _H	— /(RDR18/(TDR18))[R/W] B,H,W ----- *3		RDR08/(TDR08)[R/W] B,H,W -----0 00000000 *1		
001898 _H	SACSR8[R/W] B,H,W 0---000 00000000		STMR8[R] B,H,W 00000000 00000000		
00189C _H	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W ----- *3 *4		
0018A0 _H	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W ----- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W ----- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W ----- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W ----- *3	
0018A4 _H	—	— /(SCSFR28) [R/W] B,H,W ----- *3	— /(SCSFR18) [R/W] B,H,W ----- *3	— /(SCSFR08) [R/W] B,H,W ----- *3	
0018A8 _H	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W ----- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W ----- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W ----- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	*4: Reserved because LIN2.1 mode is not set immediately after reset.
0018AC _H	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W ----- *2	— /(ISBA8)[R/W] B,H,W ----- *2	
0018B0 _H	FCR18[R/W] B,H,W ---00100	FCR08[R/W] B,H,W -0000000	FBYTE8[R/W] B,H,W 00000000 00000000		Multi-UART8
0018B4 _H	FTICR8[R/W] B,H,W 00000000 00000000		—	—	

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Used with the INT instruction	66 255	42 FF	-	2F4 _H 000 _H	000FFE4 _H 000FFC00 _H	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

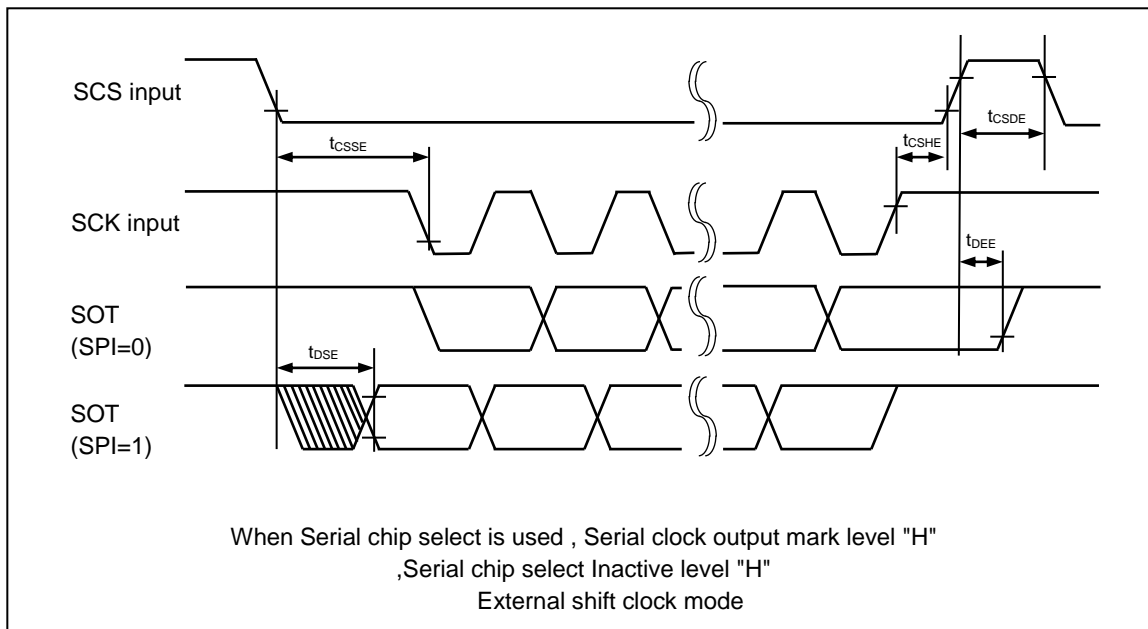
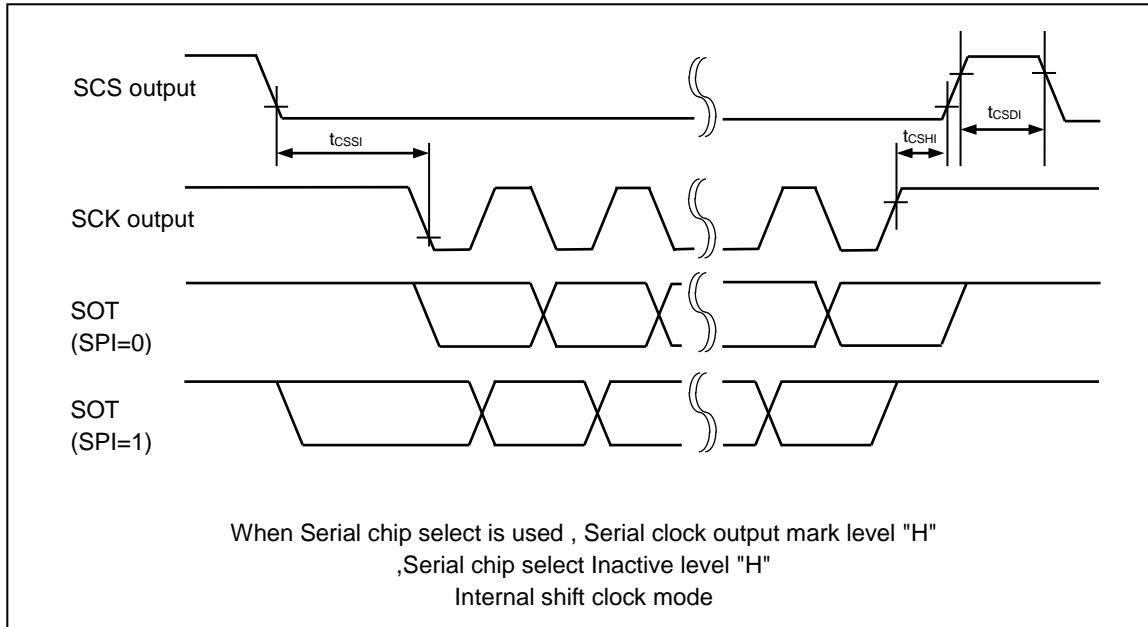
*4: The clock calibration unit does not support a DMA transfer by the interrupt.

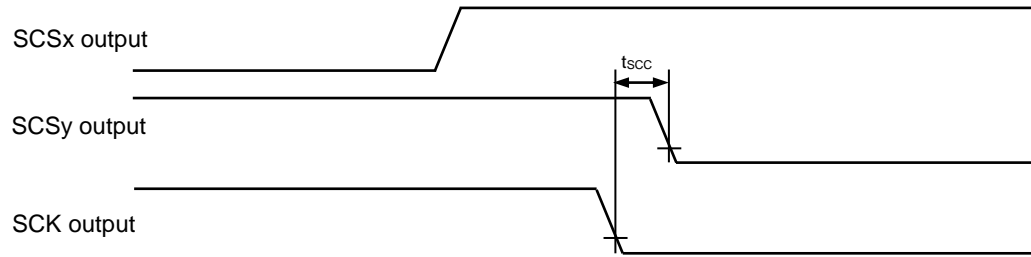
*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.





When Serial chip select is used , Serial clock output mark level "H"
 ,Serial chip select Inactive level "H"
 Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-6) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,

When Serial chip select is used : SCSCR:CSEN = 1,

Serial clock output mark level "L" : SMR,SCSFR:SCINV = 1,

Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL = 1

(TA: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t _{CSSt}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CSSt} -50 *1	t _{CSSt} +0 *1	ns	Internal shift clock mode output pin : C _L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSSt} -50 *1	t _{CSSt} +300 *1	ns	
SCK↓→SCS↑ hold time	t _{CSHt}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSHt} -10 *2	t _{CSHt} +50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSHt} -300 *2	t _{CSHt} +50 *2	ns	
SCS deselect time	t _{CSDt}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSDt} -50 *3	t _{CSDt} +50 *3	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \uparrow →SCK \uparrow setup time	t _{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: C _L = 50 pF
SCK \downarrow →SCS \downarrow hold time	t _{CSHE}			+0	-	ns	
SCS deselect time	t _{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		3t _{CPP} +30	-	ns	
SCS \uparrow →SOT delay time	t _{DSE}	SCS1 , SCS2, SCS50~SCS53, SCS60~SCS63, SCS70~SCS73, SCS8~SCS11 SOT1 , SOT2, SOT5~SOT11		-	40	ns	
		SCS3 , SCS40~SCS43 SOT3 ,SOT4		-	300	ns	
SCS \downarrow →SOT delay time	t _{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C _L = 50 pF
SCK \uparrow →SCS \uparrow clock switch time	t _{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: C _L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50		

*1: t_{CSSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

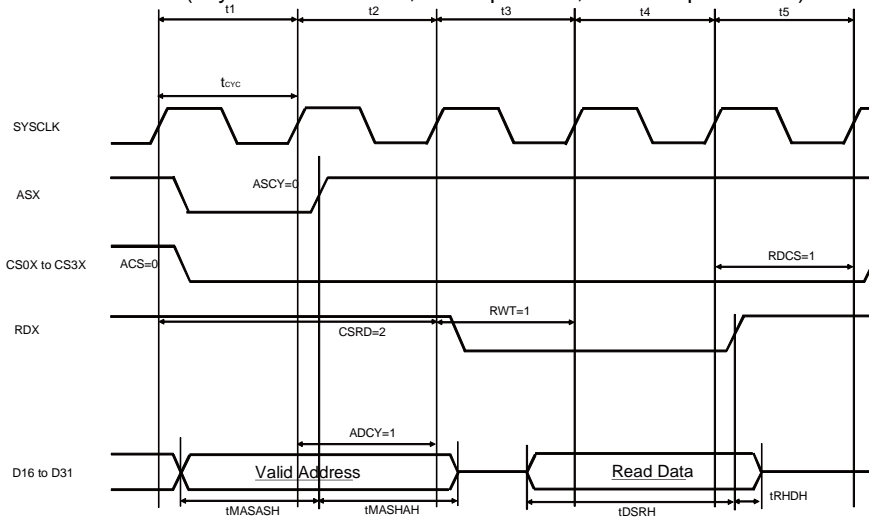
*2: t_{CSHD} = SCSTR:CSHD7-0 × Serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

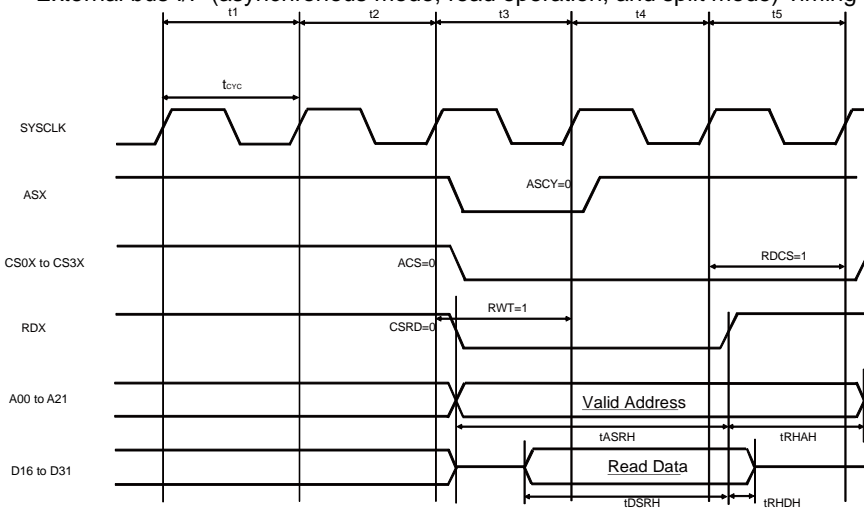
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1, *2, and *3.

External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing

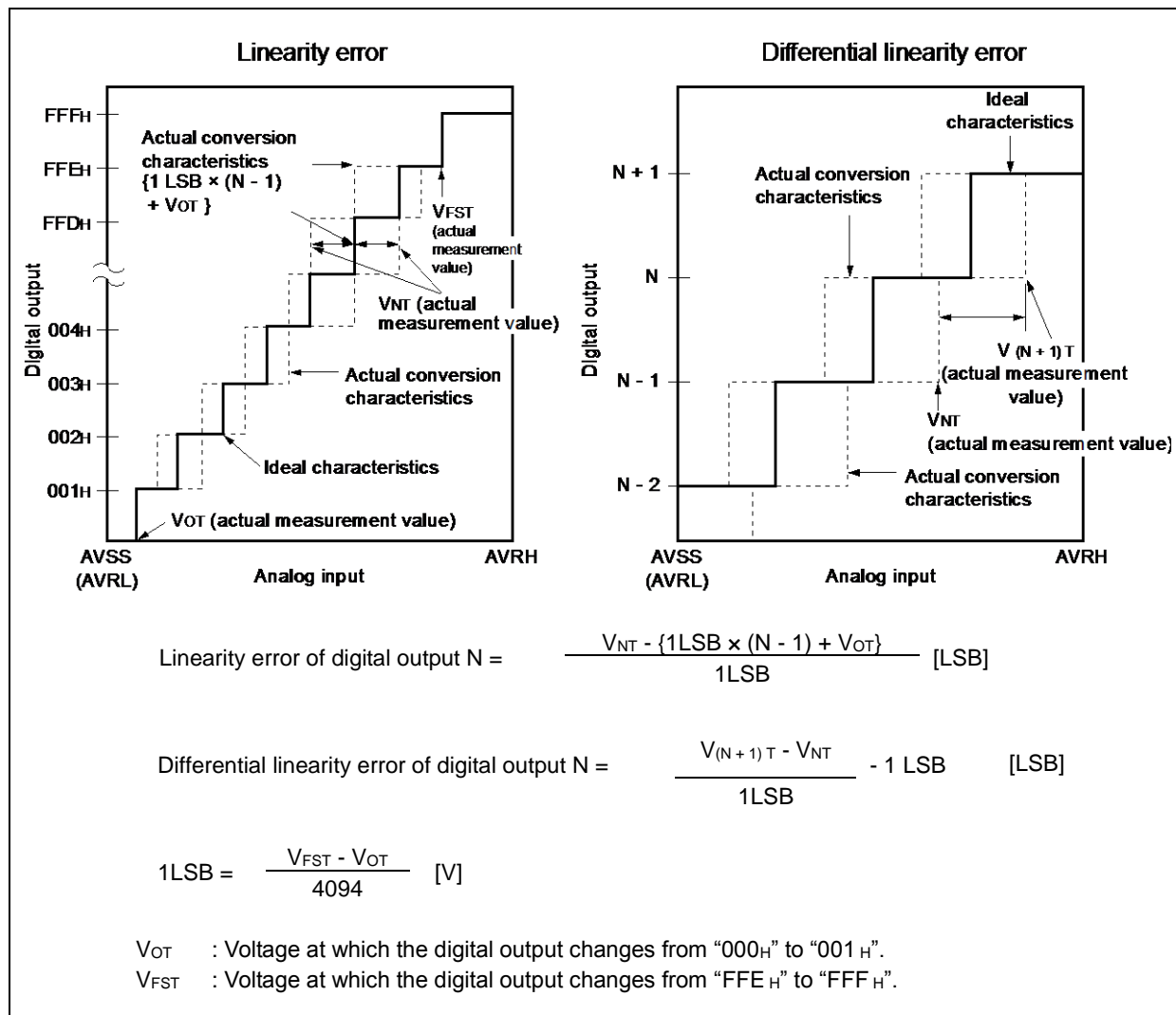


External bus I/F (asynchronous mode, read operation, and split mode) Timing

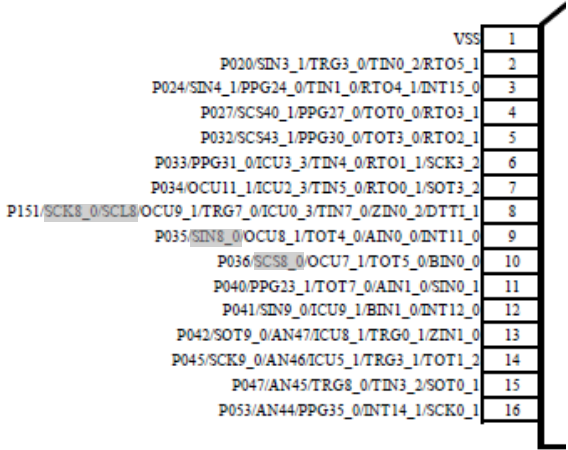
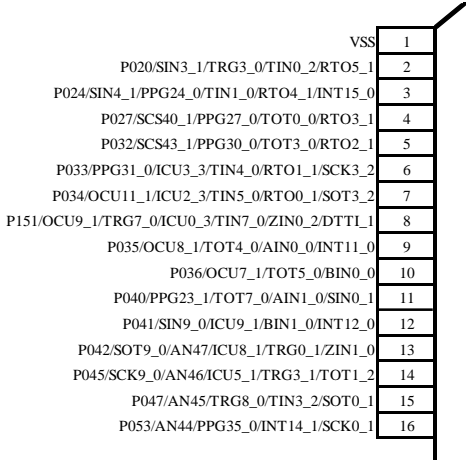


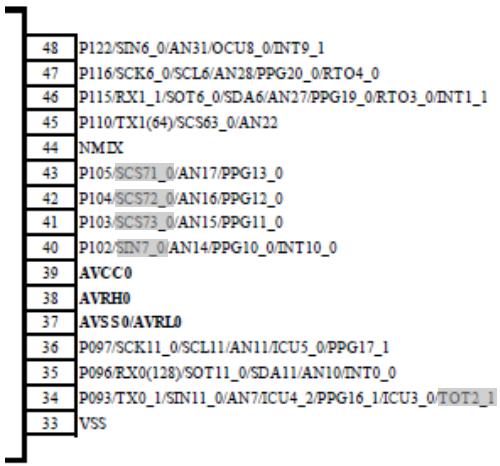
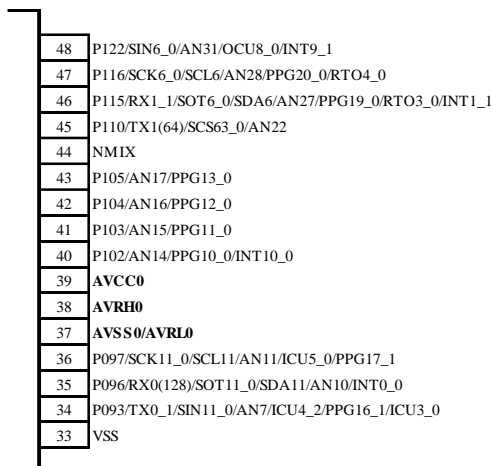
(2) Definition of A/D Converter Terms

- Resolution** : Analog variation that is recognized by an A/D converter.
- Linearity error** : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000" ← → "0000 0000 0001") to the full-scale transition point ("1111 1111 1110" ← → "1111 1111 1111").
- Differential linearity error** : Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



Page	Section	Change Results				
9	■Product Lineup	<p>Corrected the following description for Product lineup comparison(120 pin).</p> <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> <p>↓</p> <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
9	■Product Lineup	<p>Added the following sentences under Product lineup comparison(120 pin) *1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).</p> <p>Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).</p>				
10	■Product Lineup	<p>Corrected the following description for Product lineup comparison(144 pin).</p> <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> <p>↓</p> <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
10	■Product Lineup	<p>Added the following sentences under Product lineup comparison(144 pin) *1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).</p> <p>Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).</p>				
11	■Product Lineup	<p>Corrected the following description for Product lineup comparison(176 pin).</p> <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> <p>↓</p> <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
11	■Product Lineup	<p>Added the following sentences under Product lineup comparison(176 pin) *1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).</p> <p>Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).</p>				

Page	Section	Change Results
13	■ Pin Assignment MB91F52xB	<p>Signals indicated by the shading below deleted in Figure.</p> <p>- Left side</p>  <p>↓</p> 

Page	Section	Change Results
13	■ Pin Assignment MB91F52xB	<p>- Right side</p>  <p>↓</p> 

Page	Section	Change Results									
21, 22	■PIN Description	(Continued)									
		(Correct)									
		Pin no.						Pin Name			
		64	80	100	120	144	176				
		7 ^{*1}	9 ^{*1}	11 ^{*1}	14 ^{*1}	17	21	P034			
								A06 ^{*2, *3, *4, *5}			
								OCU11_1			
								ICU2_3			
								TIN5_0			
								RTO0_1			
								SOT3_2			
		8 ^{*1}	10 ^{*1}	13	16	19	23	P151			
								SCK8_0/ SCL8 ^{*2, *3}			
								OCU9_1			
								TRG7_0			
								ICU0_3			
								TIN7_0			
								ZIN0_2			
								DTTI_1			
		9 ^{*1}	11 ^{*1}	14 ^{*1}	17 ^{*1}	20	24	P035			
								A07 ^{*2, *3, *4, *5}			
								SIN8_0 ^{*2, *3}			
								OCU8_1			
								TOT4_0			
								AIN0_0			
								INT11_0			
		10 ^{*1}	12 ^{*1}	15 ^{*1}	18 ^{*1}	21	25	P036			
								A08 ^{*2, *3, *4, *5}			
								SCS8_0 ^{*2, *3}			
								OCU7_1			
								TOT5_0			
								BIN0_0			
		-	-	16 ^{*1}	19 ^{*1}	22	26	P037			
								A09 ^{*4, *5}			
								OCU6_1			
								TOT6_0			
								ZIN0_0			
		-	-	-	-	-	27	P174			
								TRG8_1			