Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525bsdpmc1-gse2

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
-	-	20 *1	23 *1	26	32	P043	-	A	General-purpose I/O port
						A13 *4, *5	-		External bus/Address bit13 output (0)
						ICU7_1	-		Input capture ch.7 input (1)
						TRG1_1	-		PPG trigger 1 input (1)
-	16 *1	21 *1	24 *1	27	33	P044	-	A	General-purpose I/O port
						A14 *3, *4, *5	-		External bus/Address bit14 output (0)
						SCS9_0	-		Serial chip select 9 I/O (0)
						ICU6_1	-		Input capture ch.6 input (1)
						TRG2_1	-		PPG trigger 2 input (1)
14 *1	17 *1	22 *1	25 *1	28	34	P045	-	G	General-purpose I/O port
						A15 *2, *3, *4, *5	-		External bus/Address bit15 output (0)
						SCK9_0	-		Multi-function serial ch.9 clock I/O (0)
						AN46	-		ADC analog 46 input
						ICU5_1	-		Input capture ch.5 input (1)
						TRG3_1	-		PPG trigger 3 input (1)
						TOT1_2	-		Reload timer ch.1 output (2)
-	-	-	26 *1	29	35	P046	-	A	General-purpose I/O port
						A16 *5	-		External bus/Address bit16 output (0)
						ICU4_1	-		Input capture ch.4 input (1)
						TRG4_1	-		PPG trigger 4 input (1)
-	-	-	-	-	36	P176	-	A	General-purpose I/O port
						TRG10_0	-		PPG trigger 10 input (0)
15 *1	18 *1	23 *1	27 *1	30	37	P047	-	B	General-purpose I/O port
						A17 *2, *3, *4, *5	-		External bus/Address bit17 output (0)
						AN45	-		ADC analog 45 input
						TRG8_0	-		PPG trigger 8 input (0)
						TIN3_2	-		Reload timer ch.3 event input (2)
						SOT0_1	-		Multi-function serial ch.0 serial data output (1)
-	-	-	-	-	38	P177	-	A	General-purpose I/O port
						TRG11_0	-		PPG trigger 11 input (0)
-	-	-	28 *1	31	39	P050	-	A	General-purpose I/O port
						A18 *5	-		External bus/Address bit18 output
						TRG5_1	-		PPG trigger 5 input (1)
						PPG33_0	-		PPG ch.33 output (0)
-	-	-	-	32	40	P051	-	A	General-purpose I/O port
						A19	-		External bus/Address bit19 output
						TRG9_0	-		PPG trigger 9 input (0)
-	-	-	-	33	41	P052	-	A	General-purpose I/O port
						A20	-		External bus/Address bit20 output
						PPG34_0	-		PPG ch.34 output (0)
						INT14_0	-		INT14 External interrupt input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	45	55	P143	-	F	General-purpose I/O port
						SOT10_0/SDA10	-		Multi-function serial ch.10 serial data output (0)/ I2C bus serial data I/O
						PPG39_0	-		PPG ch.39 output (0)
						TOT4_1	-		Reload timer ch.4 output (1)
-	-	-	-	-	56	P182	-	A	General-purpose I/O port
						PPG42_0	-		PPG ch.42 output (0)
-	-	32	38	46	57	P060	-	A	General-purpose I/O port
						SCS10_0	-		Serial chip select 10 I/O (0)
						PPG2_1	-		PPG ch.2 output (1)
						ICU2_1	-		Input capture ch.2 input (1)
						TOT5_1	-		Reload timer ch.5 output (1)
						INT13_0	-		INT13 External interrupt input (0)
22	27	33	39	47	58	P061	-	B	General-purpose I/O port
						SOT10_1	-		Multi-function serial ch.10 serial data output (1)
						AN41	-		ADC analog 41 input
						ICU6_0	-		Input capture ch.6 input (0)
						PPG3_1	-		PPG ch.3 output (1)
						ICU3_1	-		Input capture ch.3 input (1)
						TOT6_1	-		Reload timer ch.6 output (1)
						INT13_1	-		INT13 External interrupt input (1)
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

This section explains the latch-up prevention and pin processing.

- For latch-up prevention
  If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

  Also, the analog power supply (AVCC, AVRH) and analog input must not be exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

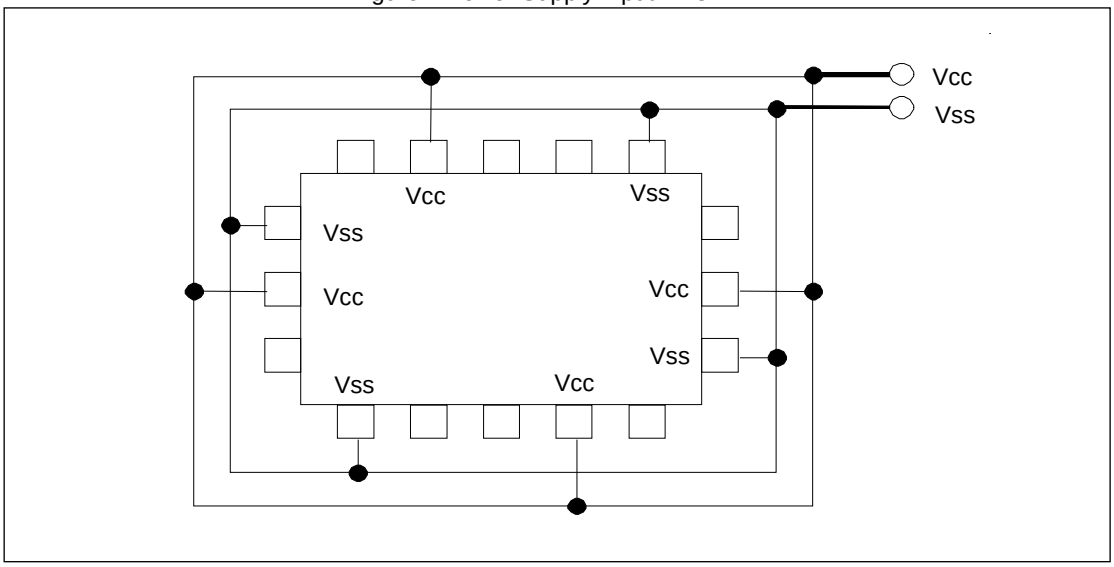
  In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

- Treatment of unused pins
  If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2 kΩ resistor to each of the unused pins for pull-up or pull-down processing.

  Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

- Power supply pins
  The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

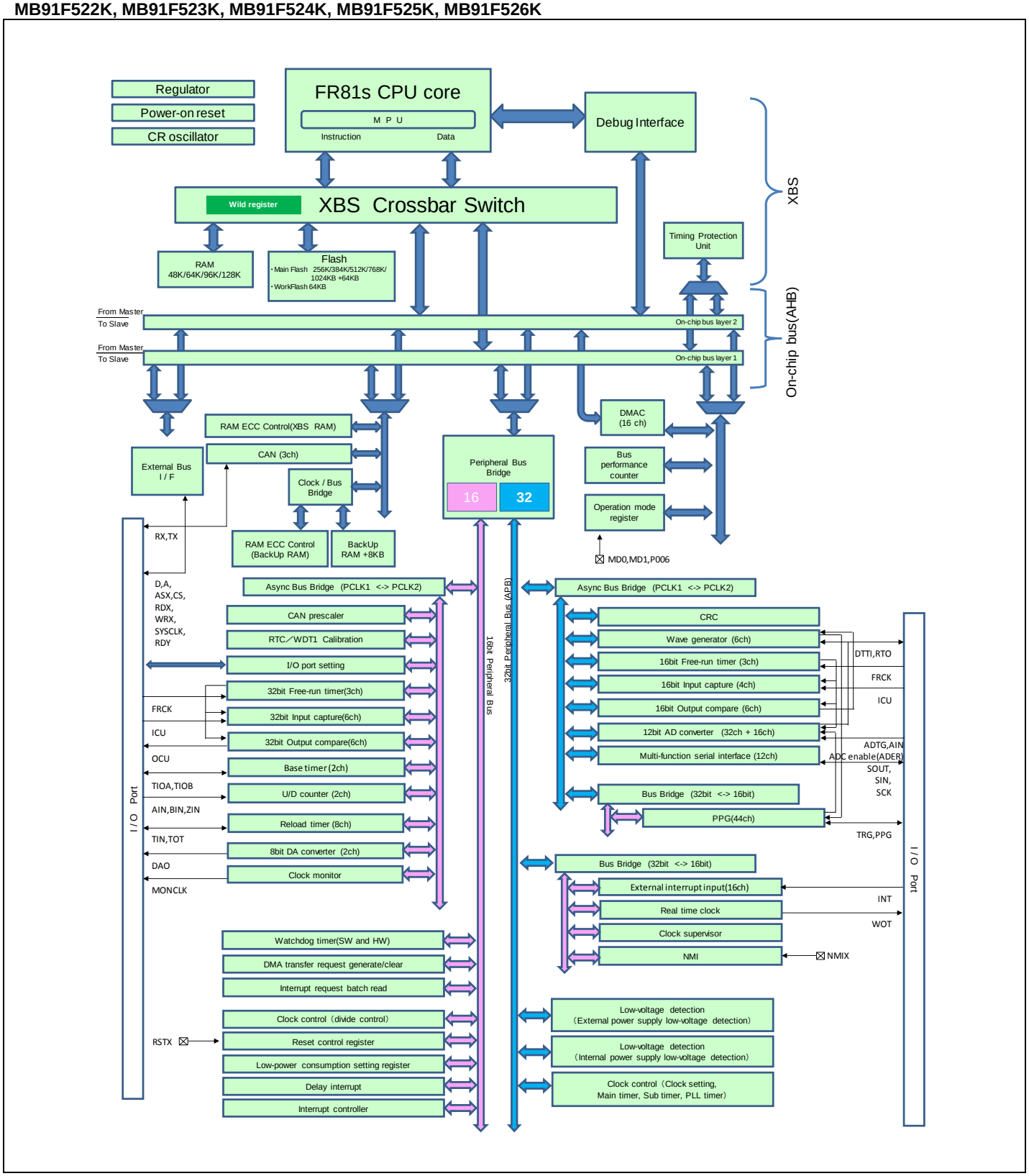
Figure 1 Power Supply Input Pins



The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000084H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	—	—	
000088H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
00008CH	—	—	—	—	Reserved
000090H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	—	—	
000098H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009CH	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base Timer 0,1
0000A0H to 0000FCH	—	—	—	—	Reserved
000100H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
00010CH	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45
00011CH	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000120H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	
00012CH	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138H to 0001B4H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0015B4H	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	12-bit A/D converter 2/2 unit
0015B8H	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
0015BCH	—	—	—	—	
0015C0H	—	—	—	—	
0015C4H	ADPRTF1 [R] B,H,W -------- -------- 00000000 00000000				
0015C8H	ADEOCF1 [R] B,H,W -------- -------- 11111111 11111111				
0015CCH	ADCS1 [R] B,H,W 0------- --------		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
0015D0H	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	
0015D4H to 00174CH	—	—	—	—	Reserved
001750H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I²C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754H	— /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001758H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175CH	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4		
001760H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3	
001764H	—	— /(SCSFR20) [R/W] B,H,W -------- *3	— /(SCSFR10) [R/W] B,H,W -------- *3	— /(SCSFR00) [R/W] B,H,W -------- *3	
001768H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176CH	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -------- *2	— /(ISBA0) [R/W] B,H,W -------- *2	
001770H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001A54H	PHDUT0 [W] H,W XXXXXXXX XXXXXXXX		PLDUT0 [W] H,W XXXXXXXX XXXXXXXX		PPG0 * for communication
001A58H	PCMDDT0 [R/W] H,W 00000000 00000000		—	—	
001A5CH	PCN1 [R/W] B,H,W 00000000 000000-0		PCSR1 [W] H,W XXXXXXXX XXXXXXXX		PPG1 * for communication
001A60H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PTMR1 [R] H,W 11111111 11111111		
001A64H	PCN201 [R/W] B,H,W --000000 -----110		PSDR1 [R/W] H,W 00000000 00000000		PPG1 * for communication
001A68H	PTPC1 [R/W] H,W 00000000 00000000		PCMDWD1 [R/W] B,H,W -------- ----0000		
001A6CH	PHCSR1 [W] H,W XXXXXXXX XXXXXXXX		PLCSR1 [W] H,W XXXXXXXX XXXXXXXX		
001A70H	PHDUT1 [W] H,W XXXXXXXX XXXXXXXX		PLDUT1 [W] H,W XXXXXXXX XXXXXXXX		
001A74H	PCMDDT1 [R/W] H,W 00000000 00000000		—	—	
001A78H	PCN2 [R/W] B,H,W 00000000 000000-0		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2 * for communication
001A7CH	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PTMR2 [R] H,W 11111111 11111111		
001A80H	PCN202 [R/W] B,H,W --000000 -----110		PSDR2 [R/W] H,W 00000000 00000000		PPG2 * for communication
001A84H	PTPC2 [R/W] H,W 00000000 00000000		PCMDWD2 [R/W] B,H,W -------- ----0000		
001A88H	PHCSR2 [W] H,W XXXXXXXX XXXXXXXX		PLCSR2 [W] H,W XXXXXXXX XXXXXXXX		
001A8CH	PHDUT2 [W] H,W XXXXXXXX XXXXXXXX		PLDUT2 [W] H,W XXXXXXXX XXXXXXXX		
001A90H	PCMDDT2 [R/W] H,W 00000000 00000000		—	—	
001A94H	PCN3 [R/W] B,H,W 00000000 000000-0		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3 * for communication
001A98H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PTMR3 [R] H,W 11111111 11111111		
001A9CH	PCN203 [R/W] B,H,W --000000 -----110		PSDR3 [R/W] H,W 00000000 00000000		
001AA0H	PTPC3 [R/W] H,W 00000000 00000000		PCMDWD3 [R/W] B,H,W -------- ----0000		
001AA4H	PHCSR3 [W] H,W XXXXXXXX XXXXXXXX		PLCSR3 [W] H,W XXXXXXXX XXXXXXXX		
001AA8H	PHDUT3 [W] H,W XXXXXXXX XXXXXXXX		PLDUT3 [W] H,W XXXXXXXX XXXXXXXX		
001AACH	PCMDDT3 [R/W] H,W 00000000 00000000		—	—	
001AB0H	PCN4 [R/W] B,H,W 00000000 000000-0		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
001AB4H	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PTMR4 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00204C$_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	CAN0 (128msb)
002050$_H$	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		
002054$_H$	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058$_H$	—	—	—	—	
00205C$_H$	—	—	—	—	
002060$_H$, 002064$_H$	Reserved(IF2 data mirror)				
002068$_H$ to 00207C$_H$	—				
002080$_H$	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		
002084$_H$	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088$_H$	TREQR60 [R] B,H,W 00000000 00000000		TREQR50 [R] B,H,W 00000000 00000000		
00208C$_H$	TREQR80 [R] B,H,W 00000000 00000000		TREQR70 [R] B,H,W 00000000 00000000		
002090$_H$	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094$_H$	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R] B,H,W 00000000 00000000		
002098$_H$	NEWDT60 [R] B,H,W 00000000 00000000		NEWDT50 [R] B,H,W 00000000 00000000		
00209C$_H$	NEWDT80 [R] B,H,W 00000000 00000000		NEWDT70 [R] B,H,W 00000000 00000000		
0020A0$_H$	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
0020A4$_H$	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
0020A8$_H$	INTPND60 [R] B,H,W 00000000 00000000		INTPND50 [R] B,H,W 00000000 00000000		
0020AC$_H$	INTPND80 [R] B,H,W 00000000 00000000		INTPND70 [R] B,H,W 00000000 00000000		
0020B0$_H$	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
0020B4$_H$	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
0020B8$_H$	MSGVAL60 [R] B,H,W 00000000 00000000		MSGVAL50 [R] B,H,W 00000000 00000000		
0020BC$_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0$_H$ to 0020FC$_H$	—				

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L = 50 pF
SCK↓→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50~SCS53, SCS60~SCS63, SCS70~SCS73, SCS8~SCS11 SOT1 , SOT2, SOT5~SOT11		-	40	ns	
		SCS3 , SCS40~SCS43 SOT3 ,SOT4		-	300	ns	
SCS↓→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L = 50 pF
SCK↑→SCS↑ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50		

*1: t_{CSSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: t_{CSHD} = SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: t_{CSDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

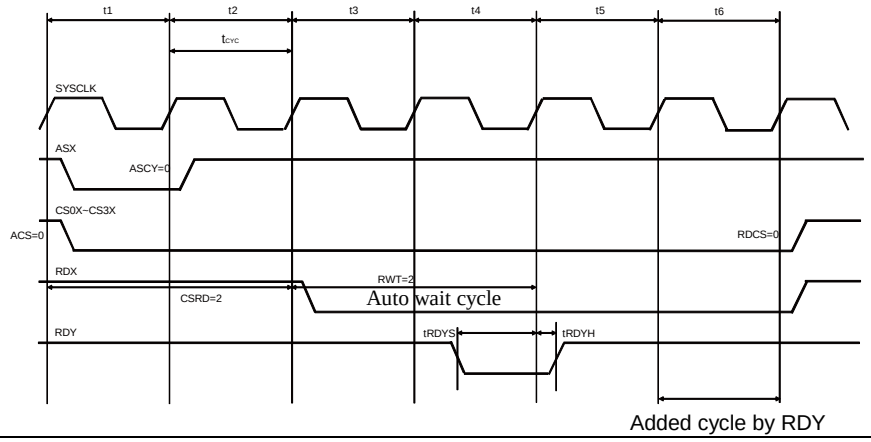
Please see the hardware manual for details of above-mentioned *1,*2, and *3.

(12) External bus I/F (ready) Timing

(T_A: -40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)
(external load capacitance 50 pF)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t_{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK, RDY	0	-	ns	

External bus I/F (ready) Timing

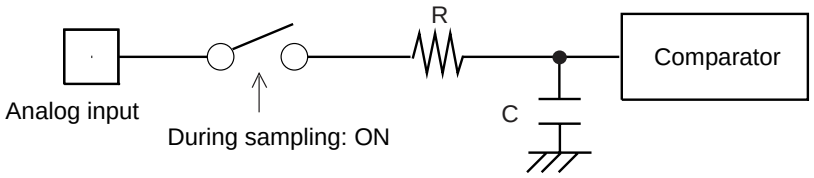


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

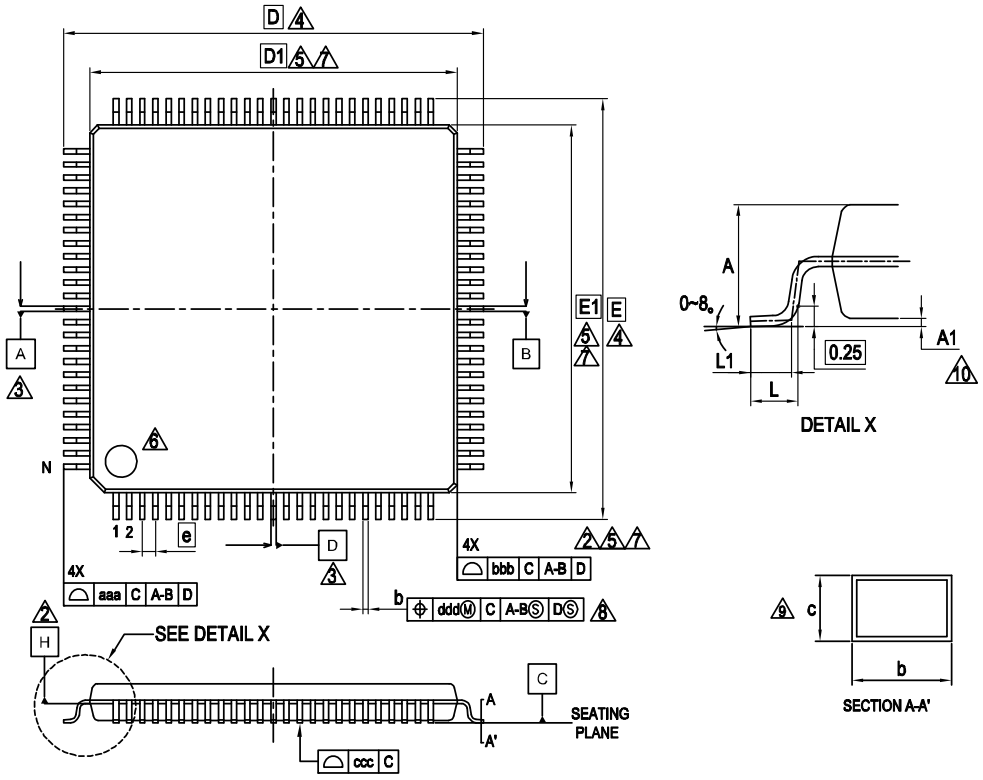
- Analog input circuit model



	R	C	
12-bit A/D	1.9 kΩ (Max)	8.30 pF (Max)	(4.5 V ≤ AV_{CC} ≤ 5.5 V)
	4.3 kΩ (Max)	8.30 pF (Max)	(3.0 V ≤ AV_{CC} ≤ 3.6 V)

Note: Listed values must be considered as reference values.

LQI100 , 100 Lead Plastic Low Profile Quad Flat Package



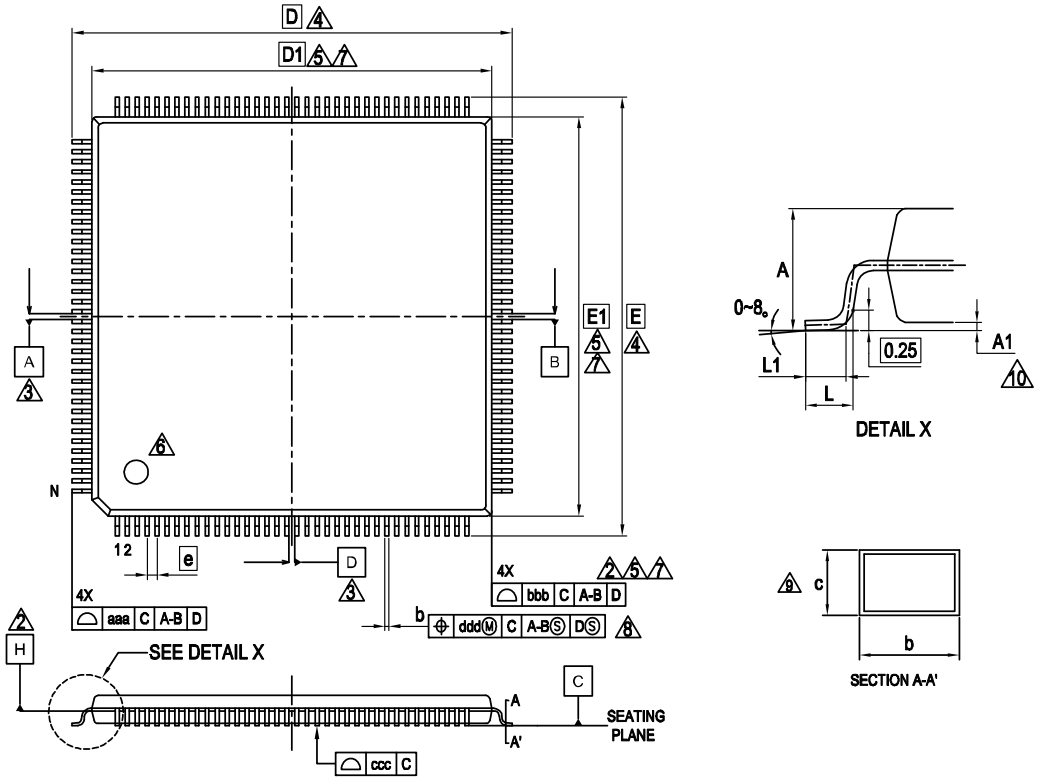
PACKAGE	LQI100		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	100		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.145	0.18	0.215
c	0.115	——	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.07
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

18. Errata

This section describes the errata for the MB91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB91F522B/D/F/J/K/L MB91F523B/D/F/J/K/L MB91F524B/D/F/J/K/L MB91F525B/D/F/J/K/L MB91F526B/D/F/J/K/L

MB91F522/3/4/5/6 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available MB91520 Series devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Power-on Conditions is not enough in the Datasheet Specification	MB91F522B/D/F/J/K/L MB91F523B/D/F/J/K/L MB91F524B/D/F/J/K/L MB91F525B/D/F/J/K/L MB91F526B/D/F/J/K/L	B, C	Will be fixed in production silicon version D, E
[2]. Limitation for Watch mode (power off)		B, C, D, E	-

1. Power-on Conditions is not enough in the Datasheet Specification

■ Problem Definition

If the Power-On-Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

■ Parameters Affected

t_{OFF} for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

■ Trigger Condition

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

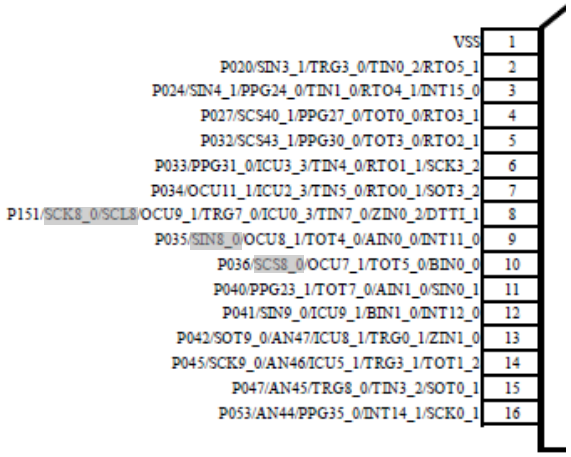
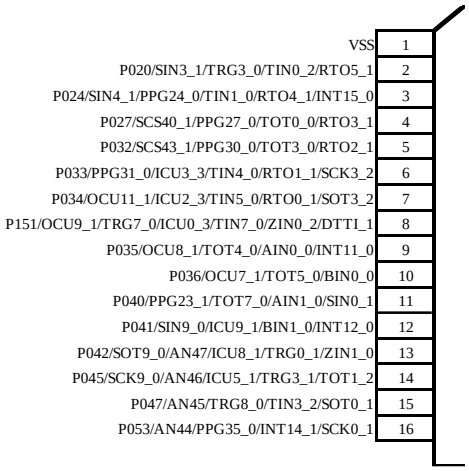
If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

Page	Section	Change Results
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVI} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVI} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max -
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVE} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300
150,152, 154,156	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_F Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11 Value: Min - Max 5

Page	Section	Change Results
13	■Pin Assignment MB91F52xB	Signals indicated by the shading below deleted in Figure. - Left side  ↓ 

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>21, 22</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="7">7 *1</td><td rowspan="7">9 *1</td><td rowspan="7">11 *1</td><td rowspan="7">14 *1</td><td rowspan="7">17</td><td rowspan="7">21</td><td>P034</td></tr>
<tr><td>A06 *2, *3, *4, *5</td></tr>
<tr><td>OCU11_1</td></tr>
<tr><td>ICU2_3</td></tr>
<tr><td>TIN5_0</td></tr>
<tr><td>RTO0_1</td></tr>
<tr><td>SOT3_2</td></tr>
<tr><td colspan="7"></td></tr>
<tr><td rowspan="8">8 *1</td><td rowspan="8">10 *1</td><td rowspan="8">13</td><td rowspan="8">16</td><td rowspan="8">19</td><td rowspan="8">23</td><td>P151</td></tr>
<tr><td>SCK8_0/ SCL8 *2, *3</td></tr>
<tr><td>OCU9_1</td></tr>
<tr><td>TRG7_0</td></tr>
<tr><td>ICU0_3</td></tr>
<tr><td>TIN7_0</td></tr>
<tr><td>ZIN0_2</td></tr>
<tr><td>DTTI_1</td></tr>
<tr><td rowspan="8">9 *1</td><td rowspan="8">11 *1</td><td rowspan="8">14 *1</td><td rowspan="8">17 *1</td><td rowspan="8">20</td><td rowspan="8">24</td><td>P035</td></tr>
<tr><td>A07 *2, *3, *4, *5</td></tr>
<tr><td>SIN8_0 *2, *3</td></tr>
<tr><td>OCU8_1</td></tr>
<tr><td>TOT4_0</td></tr>
<tr><td>AIN0_0</td></tr>
<tr><td>INT11_0</td></tr>
<tr><td rowspan="7">10 *1</td><td rowspan="7">12 *1</td><td rowspan="7">15 *1</td><td rowspan="7">18 *1</td><td rowspan="7">21</td><td rowspan="7">25</td><td>P036</td></tr>
<tr><td>A08 *2, *3, *4, *5</td></tr>
<tr><td>SCS8_0 *2, *3</td></tr>
<tr><td>OCU7_1</td></tr>
<tr><td>TOT5_0</td></tr>
<tr><td>BIN0_0</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">16 *1</td><td rowspan="5">19 *1</td><td rowspan="5">22</td><td rowspan="5">26</td><td>P037</td></tr>
<tr><td>A09 *4, *5</td></tr>
<tr><td>OCU6_1</td></tr>
<tr><td>TOT6_0</td></tr>
<tr><td>ZIN0_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">27</td><td>P174</td></tr>
<tr><td>TRG8_1</td></tr>
</table></td></tr>
</table>

Page	Section	Change Results
23, 24	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
15 *1	18 *1	23 *1	27 *1	30	37	P047
						A17 *2, *3, *4, *5
						AN45
						TRG8_0
						TIN3_2
						SOT0_1
-	-	-	-	-	38	P177
						TRG11_0
-	-	-	28 *1	31	39	P050
						A18 *5
						TRG5_1
						PPG33_0
-	-	-	-	32	40	P051
						A19
						TRG9_0
-	-	-	-	33	41	P052
						A20
						PPG34_0
						INT14_0
16 *1	19 *1	24 *1	29 *1	34	42	P053
						A21 *2, *3, *4, *5
						AN44
						PPG35_0
						INT14_1
						SCK0_1
-	-	-	-	35	43	P054
						SYSCLK
						PPG36_0
17 *1	22 *1	27 *1	32 *1	38	46	P055
						CS2X *2, *3, *4, *5
						SIN10_0
						AN43
						PPG37_0
						TIN4_1
-	-	-	33 *1	39	49	P056
						CS3X *5
						ICU9_0
						PPG0_1
						ICU0_1
						TIN5_1
						DTTI_2