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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

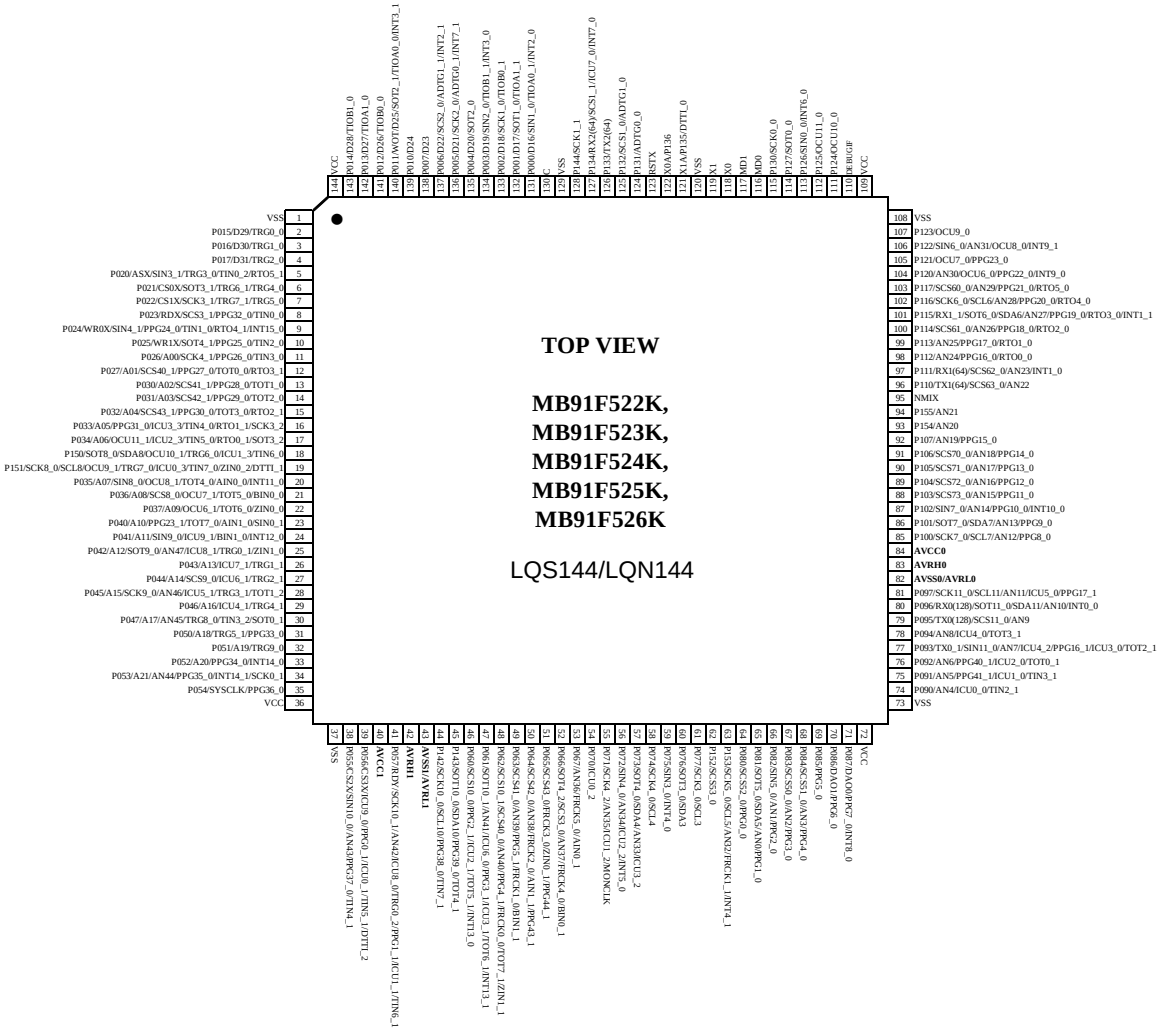
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525fsdpmc-gse2

MB91F52xK

MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K

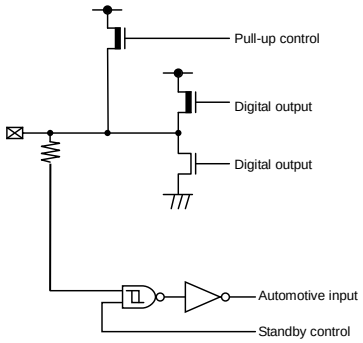
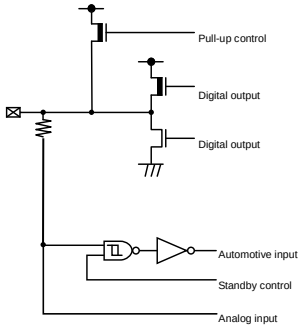
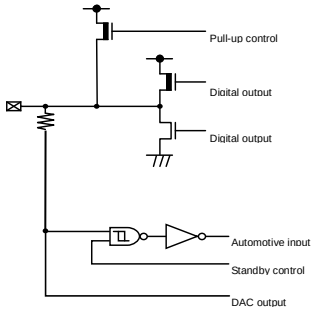
(TOP VIEW)



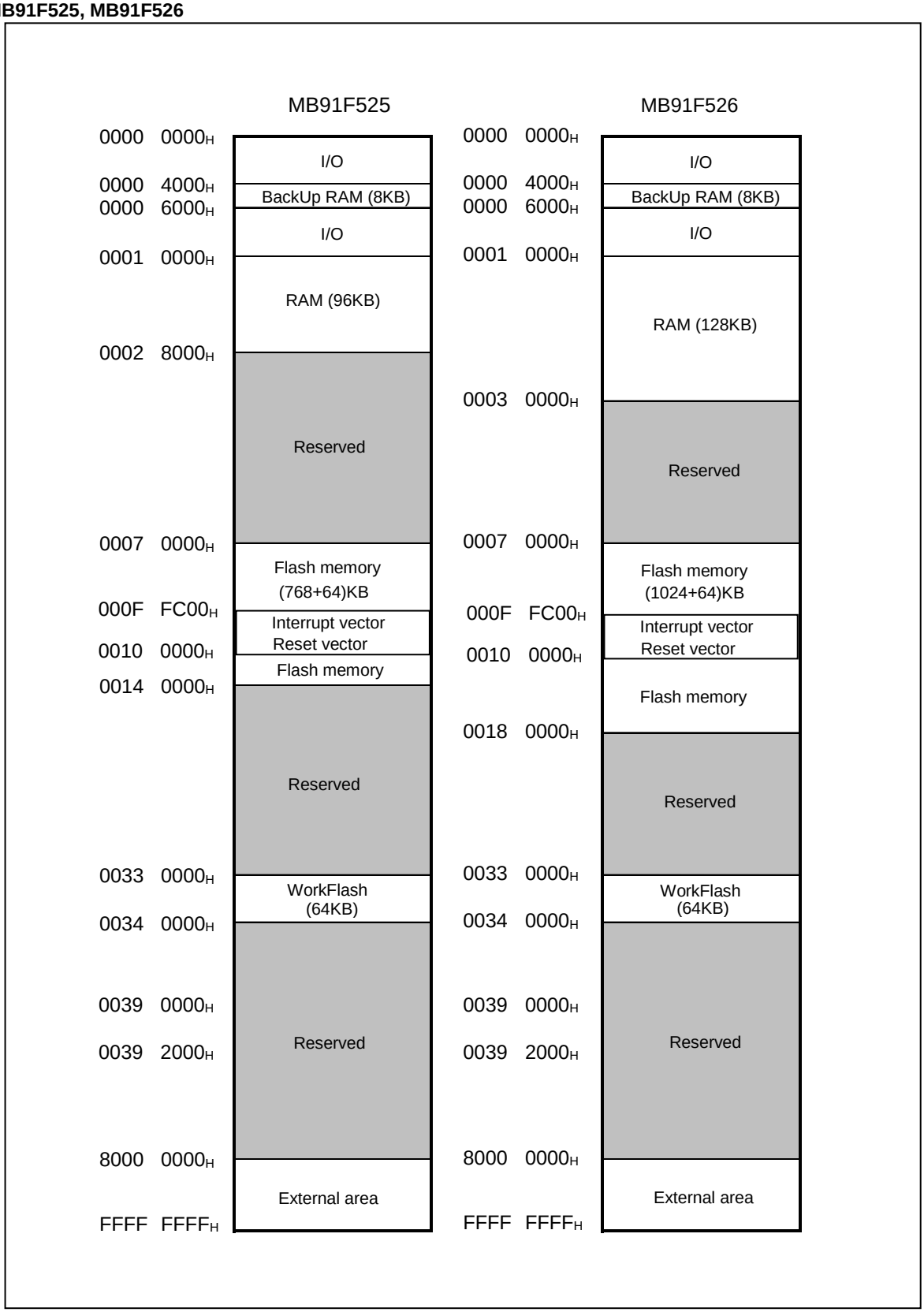
* In a single clock product, pin 121 and pin 122 are the general-purpose ports.

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	105	128	P121	-	A	General-purpose I/O port
						OCU7_0	-		Output compare ch.7 output (0)
						PPG23_0	-		PPG ch.23 output (0)
48	59	74	89	106	129	P122	-	J	General-purpose I/O port
						SIN6_0	-		Multi-function serial ch.6 serial data input (0)
						AN31	-		ADC analog 31 input
						OCU8_0	-		Output compare ch.8 output (0)
						INT9_1	-		INT9 External interrupt input (1)
-	-	-	-	-	130	P197	-	A	General-purpose I/O port
						PPG29_1	-		PPG ch.29 output (1)
-	-	-	-	107	131	P123	-	A	General-purpose I/O port
						OCU9_0	-		Output compare ch.9 output (0)
49	62	77	92	110	134	DEBUGIF	-	L	MDI I/O for debugger (OCD)
-	-	-	-	-	135	P160	-	A	General-purpose I/O port
						PPG30_1	-		PPG ch.30 output (1)
-	-	-	-	-	136	P161	-	A	General-purpose I/O port
						PPG31_1	-		PPG ch.31 output (1)
-	-	-	-	111	137	P124	-	A	General-purpose I/O port
						OCU10_0	-		Output compare ch.10 output (0)
-	-	-	93	112	138	P125	-	A	General-purpose I/O port
						OCU11_0	-		Output compare ch.11 output (0)
50	63	78	94	113	139	P126	-	F	General-purpose I/O port
						SIN0_0	-		Multi-function serial ch.0 serial data input (0)
						INT6_0	-		INT6 External interrupt input (0)
-	64	79	95	114	140	P127	-	A	General-purpose I/O port
						SOT0_0	-		Multi-function serial ch.0 serial data output (0)
-	-	80	96	115	141	P130	-	F	General-purpose I/O port
						SCK0_0	-		Multi-function serial ch.0 clock I/O (0)
-	-	-	-	-	142	P162	-	A	General-purpose I/O port
						TRG5_2	-		PPG trigger 5 input (2)
-	-	-	-	-	143	P163	-	A	General-purpose I/O port
						TRG6_2	-		PPG trigger 6 input (2)
51	65	81	97	116	144	MD0	-	K	Mode pin 0
52	66	82	98	117	145	MD1	-	K	Mode pin 1
53	67	83	99	118	146	X0	-	N	Main clock oscillation input
54	68	84	100	119	147	X1	-	N	Main clock oscillation output
56	70	86	102	121	149	P135	-	A	General-purpose I/O port
						DTTI_0	-		Waveform generator ch.0-ch.5 input pin (0)
						X1A	-	O	Sub clock oscillation output
57	71	87	103	122	150	P136	-	A	General-purpose I/O port
						X0A	-	O	Sub clock oscillation input

4. I/O Circuit Type

Type	Circuit	Remarks
A		•General-purpose I/O port •Output 4 mA •Pull-up resistor control 50 kΩ •Automotive input
B		•Analog input, General-purpose I/O port •Output 4 mA •Pull-up resistor control 50 kΩ •Automotive input
C		•DAC output, General-purpose I/O port •Output 4 mA •Pull-up resistor control 50 kΩ •Automotive input

MB91F525, MB91F526



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000084H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	—	—	
000088H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
00008CH	—	—	—	—	Reserved
000090H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	—	—	
000098H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009CH	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base Timer 0,1
0000A0H to 0000FCH	—	—	—	—	Reserved
000100H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
00010CH	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45
00011CH	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000120H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	
00012CH	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138H to 0001B4H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00121C$_H$ to 001230$_H$	—	—	—	—	Reserved
001234$_H$	FRS0 [R/W] B,H,W -------- --00--00 --00--00 --00--00				16-bit Free-run timer selection
001238$_H$	—		FRS1 [R/W] B,H,W --00--00 --00--00		
00123C$_H$	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001240$_H$	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001244$_H$	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001248$_H$	—	—	—	—	Reserved
00124C$_H$	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000		OCCPB1/OCCP1 [R/W] H,W 00000000 00000000		16-bit Output compare 0/1
001250$_H$	OCS01 [R/W] B,H,W -110--00 00001100		—	OCMOD01 [R/W] B,H,W ------00	
001254$_H$	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000		OCCPB3/OCCP3 [R/W] H,W 00000000 00000000		16-bit Output compare 2/3
001258$_H$	OCS23 [R/W] B,H,W -110--00 00001100		—	OCMOD23 [R/W] B,H,W ------00	
00125C$_H$	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000		OCCPB5/OCCP5 [R/W] H,W 00000000 00000000		16-bit Output compare 4/5
001260$_H$	OCS45 [R/W] B,H,W -110--00 00001100		—	OCMOD45 [R/W] B,H,W ------00	
001264$_H$ to 001278$_H$	—	—	—	—	Reserved
00127C$_H$	IPCP0 [R] H,W 00000000 00000000		IPCP1 [R] H,W 00000000 00000000		16-bit Input capture 0/1
001280$_H$	ICS01 [R/W] B,H,W ------00 00000000		—	LSYNS [R/W] B,H,W ----0000	
001284$_H$	IPCP2 [R] H,W 00000000 00000000		IPCP3 [R] H,W 00000000 00000000		16-bit Input capture 2/3
001288$_H$	ICS23 [R/W] B,H,W ------00 00000000		—	—	
00128C$_H$ to 001298$_H$	—	—	—	—	Reserved
00129C$_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001448H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	12-bit A/D converter 1/2 unit
00144CH	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
00145CH	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460H	ADCS0[R] B,H,W 0------- --------		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	
001468H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	
00146CH	—				12-bit A/D converter 2/2 unit
001470H	ADTSS1[R/W] B,H,W -------0	—	—	—	
001474H	ADTSE1[R/W] B,H,W -------- -------- 00000000 00000000				
001478H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		
00147CH	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit
001480H	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484H	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488H	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
00148CH	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490H	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		
001494H	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		
001498H to 0014B4H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B18H	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
001B1CH	PTPC10 [R/W] H,W 00000000 00000000		—	—	
001B20H	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11
001B24H	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PTMR11 [R] H,W 11111111 11111111		PPG11
001B28H	PCN211 [R/W] B,H,W --000000 -----110		PSDR11 [R/W] H,W 00000000 00000000		
001B2CH	PTPC11 [R/W] H,W 00000000 00000000		—	—	
001B30H	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
001B34H	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
001B38H	PCN212 [R/W] B,H,W --000000 -----110		PSDR12 [R/W] H,W 00000000 00000000		
001B3CH	PTPC12 [R/W] H,W 00000000 00000000		—	—	
001B40H	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
001B44H	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
001B48H	PCN213 [R/W] B,H,W --000000 -----110		PSDR13 [R/W] H,W 00000000 00000000		
001B4CH	PTPC13 [R/W] H,W 00000000 00000000		—	—	
001B50H	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
001B54H	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
001B58H	PCN214 [R/W] B,H,W --000000 -----110		PSDR14 [R/W] H,W 00000000 00000000		
001B5CH	PTPC14 [R/W] H,W 00000000 00000000		—	—	
001B60H	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
001B64H	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
001B68H	PCN215 [R/W] B,H,W --000000 -----110		PSDR15 [R/W] H,W 00000000 00000000		
001B6CH	PTPC15 [R/W] H,W 00000000 00000000		—	—	
001B70H	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXX XXXXXXXX		PPG16
001B74H	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PTMR16 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D50H	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
001D54H	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
001D58H	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
001D5CH	PTPC46 [R/W] H,W 00000000 00000000		—	—	
001D60H	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
001D64H	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
001D68H	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
001D6CH	PTPC47 [R/W] H,W 00000000 00000000		—	—	
001D70H to 001FFCH	—	—	—	—	Reserved
002000H	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0 [R/W] B,H,W -------- 00000000		CAN0 (128msb)
002004H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008H	INTR0 [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W -------- X00000--		
00200CH	BRPER0 [R/W] B,H,W -------- ----0000		—	—	
002010H	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201CH	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002020H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028H	—	—	—	—	
00202CH	—	—	—	—	
002030H, 002034H	Reserved(IF1 data mirror)				
002038H	—	—	—	—	
00203CH	—	—	—	—	
002040H	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		

(3) Power-on Conditions

(3-1) [MB9152xxxB/MB9152xxxC/MB9152xxxD]

(T_A: -40 °C to +125 °C, V_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF}	V_{CC}	–	50	–	–	ms	*2
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2 V to 2.376 V	–	–	4	mV/µs	*3
C pin voltage at Power-on	–	C	–	–	–	60	mV	*4

*1: This spec is at 4 mV/µs of power ramp rate. If the power ramp rate is faster than 4mV/µs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Vcc must be held below 0.2 V for a minimum period of t_{OFF}.

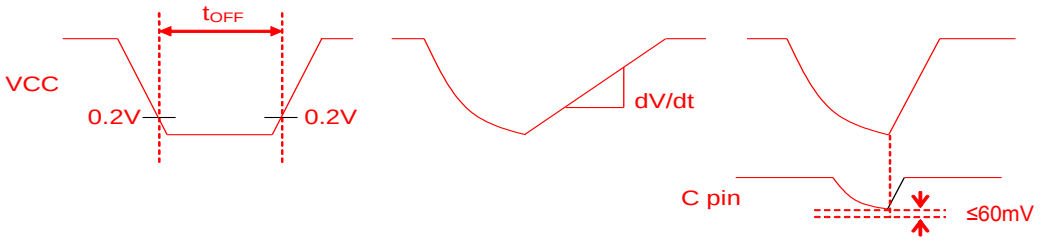
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when VCC is turned on again.

Note:

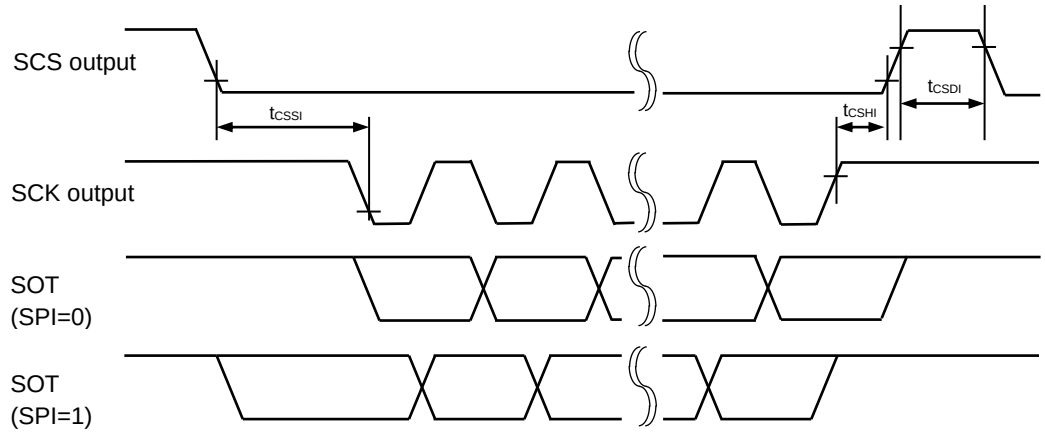
When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on

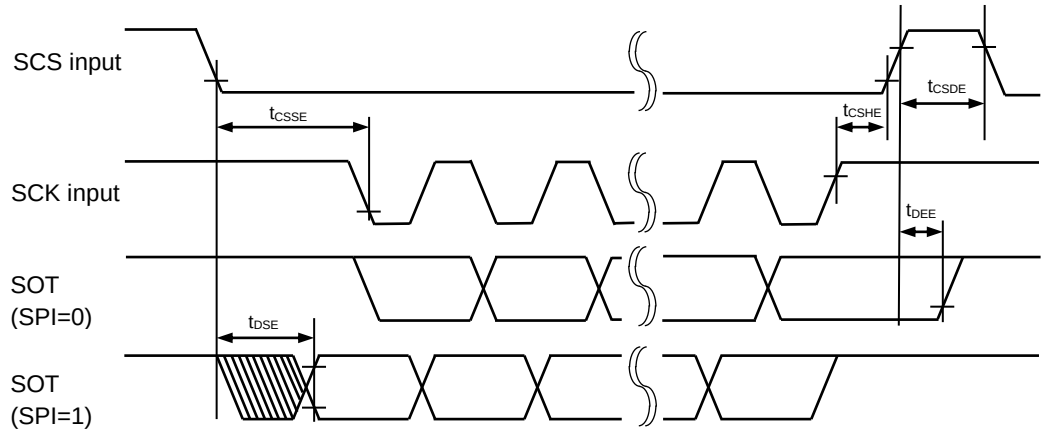


(4-1-5) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,
When Serial chip select is used : SCSCR:CSEN = 1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV = 0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL = 1
(T_A:-40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V±0.3 V, V_{SS} = AV_{SS} = 0.0V)

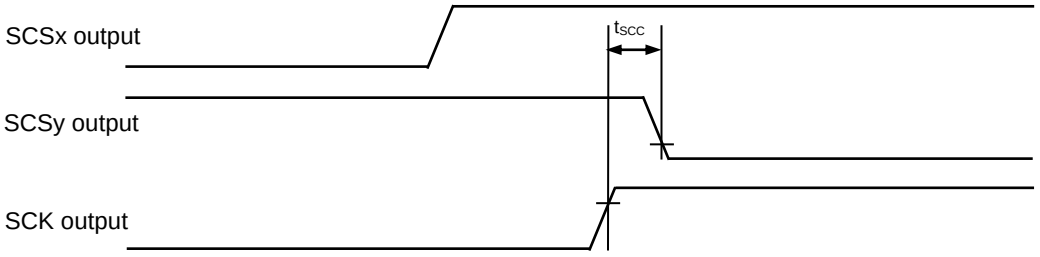
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↑→SCS↑ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
External shift clock mode



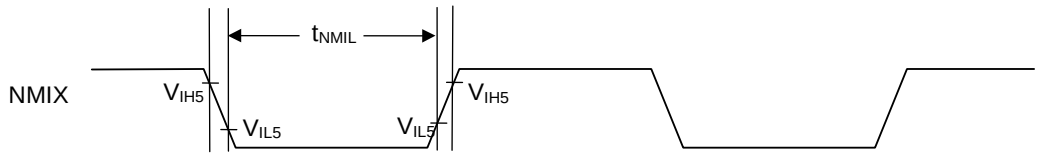
When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(7) NMI input timing

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

・ NMIX input timing



(8) Low voltage detection (External low-voltage detection)

(T_A: -40 °C to +125 °C, V_{SS} = AV_{SS} = 0.0 V)

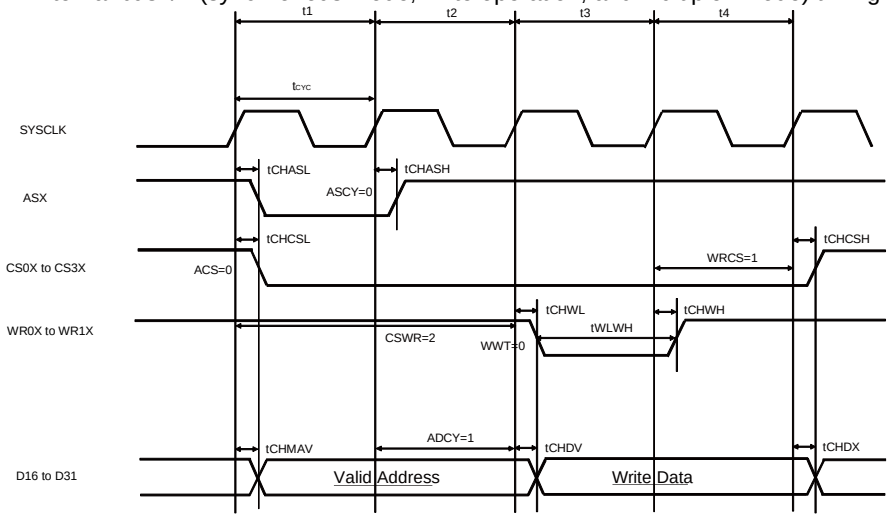
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	2.7	-	5.5	V	
Detection voltage*3	V_{DL}		*1	-8%	LVD5F_SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Hysteresis width	V_{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	Td	-		-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

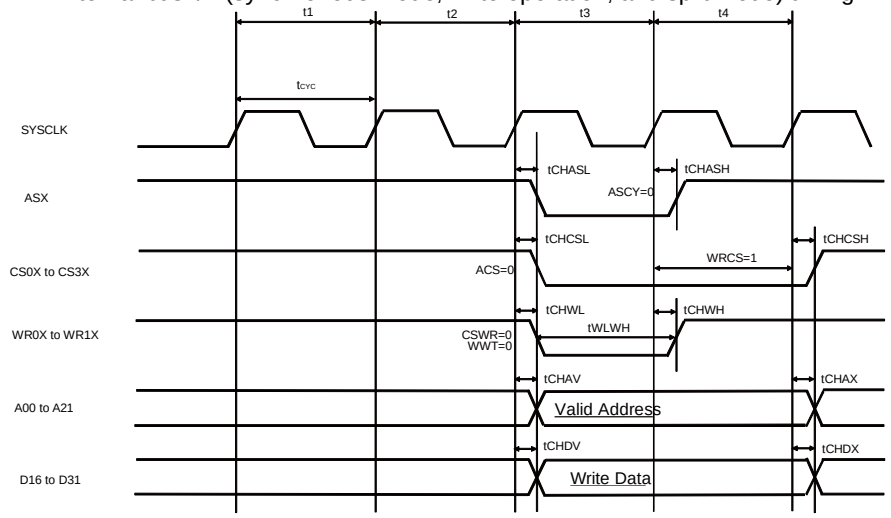
*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).

*3: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V).
This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7 V).
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing

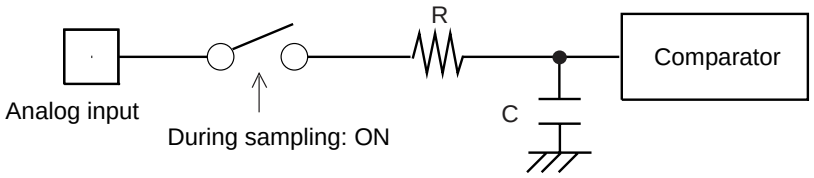


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

- Analog input circuit model



	R	C	
12-bit A/D	1.9 kΩ (Max)	8.30 pF (Max)	(4.5 V ≤ AV_{CC} ≤ 5.5 V)
	4.3 kΩ (Max)	8.30 pF (Max)	(3.0 V ≤ AV_{CC} ≤ 3.6 V)

Note: Listed values must be considered as reference values.

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
MB91F526BWBPMC1	Yes	ON	ON	LQD・64 pin, Plastic
MB91F526BYBPMC1			OFF	
MB91F526BJBPMC1		OFF	ON	
MB91F526BLBPMC1			OFF	
MB91F525BWBPMC1		ON	ON	
MB91F525BYBPMC1			OFF	
MB91F525BJBPMC1		OFF	ON	
MB91F525BLBPMC1			OFF	
MB91F524BWBPMC1		ON	ON	
MB91F524BYBPMC1			OFF	
MB91F524BJBPMC1		OFF	ON	
MB91F524BLBPMC1			OFF	
MB91F523BWBPMC1		ON	ON	
MB91F523BYBPMC1			OFF	
MB91F523BJBPMC1		OFF	ON	
MB91F523BLBPMC1			OFF	
MB91F522BWBPMC1		ON	ON	
MB91F522BYBPMC1			OFF	
MB91F522BJBPMC1		OFF	ON	
MB91F522BLBPMC1			OFF	
MB91F526BSBPMC1	None	ON	ON	
MB91F526BUBPMC1			OFF	
MB91F526BHBPMC1		OFF	ON	
MB91F526BKBPMC1			OFF	
MB91F525BSBPMC1		ON	ON	
MB91F525BUBPMC1			OFF	
MB91F525BHBPMC1		OFF	ON	
MB91F525BKBPMC1			OFF	
MB91F524BSBPMC1		ON	ON	
MB91F524BUBPMC1			OFF	
MB91F524BHBPMC1		OFF	ON	
MB91F524BKBPMC1			OFF	
MB91F523BSBPMC1		ON	ON	
MB91F523BUBPMC1			OFF	
MB91F523BHBPMC1		OFF	ON	
MB91F523BKBPMC1			OFF	
MB91F522BSBPMC1		ON	ON	
MB91F522BUBPMC1			OFF	
MB91F522BHBPMC1		OFF	ON	
MB91F522BKBPMC1			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see Package Dimensions.

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
MB91F526FWDPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FJDPMC		OFF	ON	
MB91F525FWDPMC		ON	ON	
MB91F525FJDPMC		OFF	ON	
MB91F524FWDPMC		ON	ON	
MB91F524FJDPMC		OFF	ON	
MB91F523FWDPMC		ON	ON	
MB91F523FJDPMC		OFF	ON	
MB91F522FWDPMC		ON	ON	
MB91F522FJDPMC		OFF	ON	
MB91F526FSDPMC	None	ON	ON	
MB91F526FHDPMC		OFF	ON	
MB91F525FSDPMC		ON	ON	
MB91F525FHDPMC		OFF	ON	
MB91F524FSDPMC		ON	ON	
MB91F524FHDPMC		OFF	ON	
MB91F523FSDPMC		ON	ON	
MB91F523FHDPMC		OFF	ON	
MB91F522FSDPMC		ON	ON	
MB91F522FHDPMC		OFF	ON	
MB91F526DWDPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DJDPMC		OFF	ON	
MB91F525DWDPMC		ON	ON	
MB91F525DJDPMC		OFF	ON	
MB91F524DWDPMC		ON	ON	
MB91F524DJDPMC		OFF	ON	
MB91F523DWDPMC		ON	ON	
MB91F523DJDPMC		OFF	ON	
MB91F522DWDPMC		ON	ON	
MB91F522DJDPMC		OFF	ON	
MB91F526DSDPMC	None	ON	ON	
MB91F526DHDPMC		OFF	ON	
MB91F525DSDPMC		ON	ON	
MB91F525DHDPMC		OFF	ON	
MB91F524DSDPMC		ON	ON	
MB91F524DHDPMC		OFF	ON	
MB91F523DSDPMC		ON	ON	
MB91F523DHDPMC		OFF	ON	
MB91F522DSDPMC		ON	ON	
MB91F522DHDPMC		OFF	ON	

Page	Section	Change Results
23, 24	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
15 *1	18 *1	23 *1	27 *1	30	37	P047
						A17 *2, *3, *4, *5
						AN45
						TRG8_0
						TIN3_2
						SOT0_1
-	-	-	-	-	38	P177
						TRG11_0
-	-	-	28 *1	31	39	P050
						A18 *5
						TRG5_1
						PPG33_0
-	-	-	-	32	40	P051
						A19
						TRG9_0
-	-	-	-	33	41	P052
						A20
						PPG34_0
						INT14_0
16 *1	19 *1	24 *1	29 *1	34	42	P053
						A21 *2, *3, *4, *5
						AN44
						PPG35_0
						INT14_1
						SCK0_1
-	-	-	-	35	43	P054
						SYSCLK
						PPG36_0
17 *1	22 *1	27 *1	32 *1	38	46	P055
						CS2X *2, *3, *4, *5
						SIN10_0
						AN43
						PPG37_0
						TIN4_1
-	-	-	33 *1	39	49	P056
						CS3X *5
						ICU9_0
						PPG0_1
						ICU0_1
						TIN5_1
						DTTI_2

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>33</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

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<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94</td><td rowspan="5">111</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75</td><td rowspan="4">95</td><td rowspan="4">112</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17</td></tr>
<tr><td>SOT1_0</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94 *1</td><td rowspan="5">111 *1</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16 *4, *5</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1 *4</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75 *1</td><td rowspan="4">95 *1</td><td rowspan="4">112 *1</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17 *3, *4, *5</td></tr>
<tr><td>SOT1_0 *3</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>
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</table>