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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526bhdpmc1-gs-f4e1

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)
-	-	40	46	54	68	P070	-	A	General-purpose I/O port
						ICU0_2	-		Input capture ch.0 input (2)
26	33	41	47	55	69	P071	-	G	General-purpose I/O port
						SCK4_2	-		Multi-function serial ch.4 clock I/O (2)
						AN35	-		ADC analog 35 input
						ICU1_2	-		Input capture ch.1 input (2)
						MONCLK	-		Clock monitor output pin
27	34	42	48	56	70	P072	-	G	General-purpose I/O port
						SIN4_0	-		Multi-function serial ch.4 serial data input (0)
						AN34	-		ADC analog 34 input
						ICU2_2	-		Input capture ch.2 input (2)
						INT5_0	-		INT5 External interrupt input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	83	99	119	P113	-	B	General-purpose I/O port
						AN25	-		ADC analog 25 input
						PPG17_0	-		PPG ch.17 output (0)
						RTO1_0	-		Waveform generator ch. 1 output pin (0)
-	-	-	-	-	120	P194	-	A	General-purpose I/O port
						FRCK5_1	-		Free-run timer 5 clock input (1)
						PPG26_1	-		PPG ch.26 output (1)
-	-	-	-	-	121	P195	-	A	General-purpose I/O port
						FRCK4_1	-		Free-run timer 4 clock input (1)
						PPG27_1	-		PPG ch.27 output (1)
-	56	70	84	100	122	P114	-	B	General-purpose I/O port
						SCS61_0	-		Serial chip select 61 output (0)
						AN26	-		ADC analog 26 input
						PPG18_0	-		PPG ch.18 output (0)
						RTO2_0	-		Waveform generator ch.2 output pin (0)
46	57	71	85	101	123	P115	-	G	General-purpose I/O port
						RX1_1	-		CAN reception data 1 input (1)
						SOT6_0/ SDA6	-		Multi-function serial ch.6 serial data output (0)/I^2C bus serial data I/O
						AN27	-		ADC analog 27 input
						PPG19_0	-		PPG ch.19 output (0)
						RTO3_0	-		Waveform generator ch.3 output pin (0)
						INT1_1	-		INT1 External interrupt input (1)
47	58	72	86	102	124	P116	-	G	General-purpose I/O port
						SCK6_0/ SCL6	-		Multi-function serial ch.6 clock I/O (0)/ I^2C bus serial clock I/O
						AN28	-		ADC analog 28 input
						PPG20_0	-		PPG ch.20 output (0)
						RTO4_0	-		Waveform generator ch.4 output pin (0)
-	-	73	87	103	125	P117	-	B	General-purpose I/O port
						SCS60_0	-		Serial chip select 60 I/O (0)
						AN29	-		ADC analog 29 input
						PPG21_0	-		PPG ch.21 output (0)
						RTO5_0	-		Waveform generator ch.5 output pin (0)
-	-	-	-	-	126	P196	-	A	General-purpose I/O port
						FRCK3_1	-		Free-run timer 3 clock input (1)
						PPG28_1	-		PPG ch.28 output (1)
-	-	-	88	104	127	P120	-	B	General-purpose I/O port
						AN30	-		ADC analog 30 input
						OCU6_0	-		Output compare ch.6 output (0)
						PPG22_0	-		PPG ch.22 output (0)
						INT9_0	-		INT9 External interrupt input (0)

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00055C$_H$	—	—	WTDR [R/W] H 00000000 00000000		Real Time Clock (RTC)
000560$_H$	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564$_H$	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568$_H$	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
00056C$_H$	—	CSVCR [R/W] B 000111--	—	—	Clock Supervisor
000570$_H$ to 00057C$_H$	—	—	—	—	Reserved
000580$_H$	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator Control / Low Voltage Detection
000584$_H$	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 00000001	LVD [R/W] B,H,W 01000--0	—	
000588$_H$ to 00058C$_H$	—	—	—	—	Reserved
000590$_H$	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594$_H$	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598$_H$	—	—	—	—	
00059C$_H$ to 0005BC$_H$	—	—	—	—	Reserved
0005C0$_H$ to 0005FC$_H$	—	—	—	—	Reserved
000600$_H$	ASR0 [R/W] W 00000000 00000000 -------- 1111-001				External Bus Interface [S]
000604$_H$	ASR1 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608$_H$	ASR2 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
00060C$_H$	ASR3 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610$_H$ to 00063C$_H$	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000C00H	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
000C04H	DCSR0 [R/W] H 0------- -----000		DTCR0 [R/W] H 00000000 00000000		
000C08H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0CH	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10H	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
000C14H	DCSR1 [R/W] H 0------- -----000		DTCR1 [R/W] H 00000000 00000000		
000C18H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1CH	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20H	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
000C24H	DCSR2 [R/W] H 0------- -----000		DTCR2 [R/W] H 00000000 00000000		
000C28H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2CH	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30H	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
000C34H	DCSR3 [R/W] H 0------- -----000		DTCR3 [R/W] H 00000000 00000000		
000C38H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3CH	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40H	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
000C44H	DCSR4 [R/W] H 0------- -----000		DTCR4 [R/W] H 00000000 00000000		
000C48H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C4CH	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C50H	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
000C54H	DCSR5 [R/W] H 0------- -----000		DTCR5 [R/W] H 00000000 00000000		
000C58H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C5CH	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C60H	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E20H	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
000E24H	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
000E28H	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
000E2CH	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
000E30H	—	—	—	—	
000E34H	—	—	—	—	
000E38H	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	
000E3CH	—	—	—	—	Reserved
000E40H	PDDR00 [R] B,H,W XXXXXXXX	PDDR01 [R] B,H,W XXXXXXXX	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
000E44H	PDDR04 [R] B,H,W XXXXXXXX	PDDR05 [R] B,H,W XXXXXXXX	PDDR06 [R] B,H,W XXXXXXXX	PDDR07 [R] B,H,W XXXXXXXX	
000E48H	PDDR08 [R] B,H,W XXXXXXXX	PDDR09 [R] B,H,W XXXXXXXX	PDDR10 [R] B,H,W XXXXXXXX	PDDR11 [R] B,H,W XXXXXXXX	
000E4CH	PDDR12 [R] B,H,W XXXXXXXX	PDDR13 [R] B,H,W -XXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
000E50H	—	—	—	—	
000E54H	—	—	—	—	
000E58H	PDDR16 [R] B,H,W XXXXXXXX	PDDR17 [R] B,H,W XXXXXXXX	PDDR18 [R] B,H,W XXXXXXXX	PDDR19 [R] B,H,W XXXXXXXX	
000E5CH	—	—	—	—	Reserved
000E60H	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
000E64H	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	
000E68H	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	
000E6CH	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W ------00	EPFR14 [R/W] B,H,W ------00	EPFR15 [R/W] B,H,W -----000	
000E70H	—	—	—	—	
000E74H	—	—	—	—	
000E78H	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
000E7CH	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80H	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C30H	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
001C34H	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
001C38H	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
001C3CH	PTPC28 [R/W] H,W 00000000 00000000		—	—	
001C40H	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
001C44H	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
001C48H	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
001C4CH	PTPC29 [R/W] H,W 00000000 00000000		—	—	
001C50H	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
001C54H	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
001C58H	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
001C5CH	PTPC30 [R/W] H,W 00000000 00000000		—	—	
001C60H	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
001C64H	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
001C68H	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
001C6CH	PTPC31 [R/W] H,W 00000000 00000000		—	—	
001C70H	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
001C74H	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		
001C78H	PCN232 [R/W] B,H,W --000000 -----110		PSDR32 [R/W] H,W 00000000 00000000		PPG32
001C7CH	PTPC32 [R/W] H,W 00000000 00000000		—	—	
001C80H	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXX XXXXXXXX		PPG33
001C84H	PDUT33 [W] H,W XXXXXXXX XXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
001C88H	PCN233 [R/W] B,H,W --000000 -----110		PSDR33 [R/W] H,W 00000000 00000000		PPG33
001C8CH	PTPC33 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002100H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
00210CH	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211CH	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128H	—	—	—	—	
00212CH	—	—	—	—	
002130H, 002134H	Reserved (IF1 data mirror)				CAN1 (64msb)
002138H	—	—	—	—	
00213CH	—	—	—	—	
002140H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214CH	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002150H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		
002154H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158H	—	—	—	—	
00215CH	—	—	—	—	
002160H, 002164H	Reserved (IF2 data mirror)				
002168H to 00217CH	—				
002180H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188H	—	—	—	—	
00218CH	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002190H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		CAN1 (64msb)
002194H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198H	—	—	—	—	
00219CH	—	—	—	—	
0021A0H	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
0021A4H	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
0021A8H	—	—	—	—	
0021ACH	—	—	—	—	
0021B0H	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
0021B4H	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
0021B8H	—	—	—	—	
0021BCH	—	—	—	—	
0021C0H to 0021FCH	—				
002200H	CTRLR2 [R/W] B,H,W -------- 000-0001		STATR2 [R/W] B,H,W -------- 00000000		CAN2 (64msb)
002204H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2 [R/W] B,H,W -0100011 00000001		
002208H	INTR2 [R] B,H,W 00000000 00000000		TESTR2 [R/W] B,H,W -------- X00000--		
00220CH	BRPER2 [R/W] B,H,W -------- ----0000		—		
002210H	IF1CREQ2 [R/W] B,H,W 0------- 00000001		IF1CMSK2 [R/W] B,H,W -------- 00000000		
002214H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111		
002218H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000		
00221CH	IF1MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002220H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000		
002224H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000		
002228H	—	—	—	—	
00222CH	—	—	—	—	
002230H, 002234H	Reserved (IF1 data mirror)				
002238H	—	—	—	—	
00223CH	—	—	—	—	
002240H	IF2CREQ2 [R/W] B,H,W 0------- 00000001		IF2CMSK2 [R/W] B,H,W -------- 00000000		

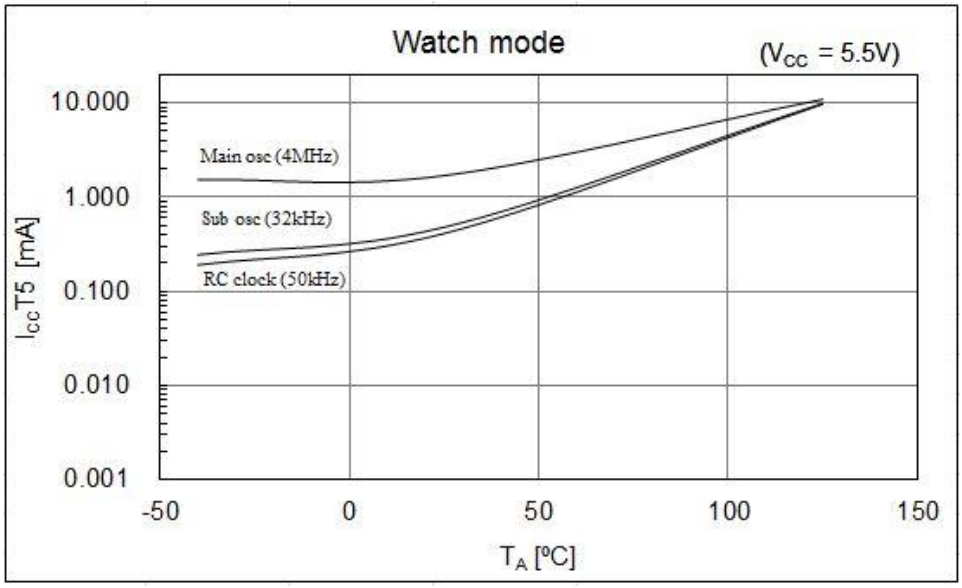
Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1,*4
A/D converter 0/1/7/10/11/14/15/16/17/22/27/28/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/34/35/37/38/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU7/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
-	60	3C	ICR44	$30C_H$	$000FFF0C_H$	-*6
- -	61	3D	ICR45	308_H	$000FFF08_H$	-
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS™*8)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-

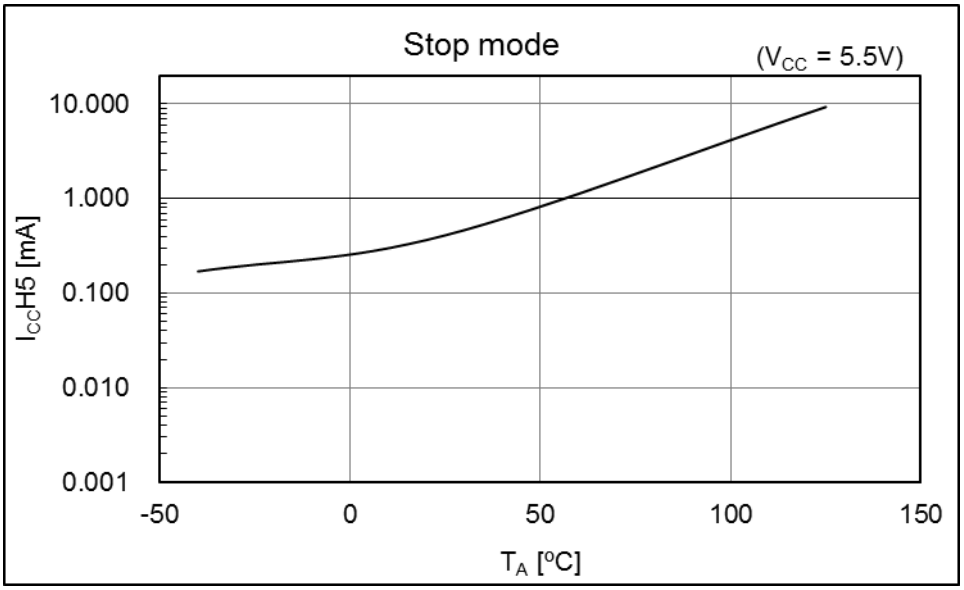
(4-1-3) Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 0, SMR:SCINV = 0, SCR:SPI = 1
(T_A:-40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L = 50 pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
SOT→SCK↓ delay time	t_{SOVLI}	SCK0 to SCK11 SOT0 to SOT11		$2t_{CPP}$ -30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+ 10	-	ns	External shift clock mode output pin: C_L = 50 pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$ -10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.
See Hardware Manual for details.

MB91F526


Watch mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
$I_{CC}T5$ [mA]
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
-50
0
50
100
150
T_A [°C]

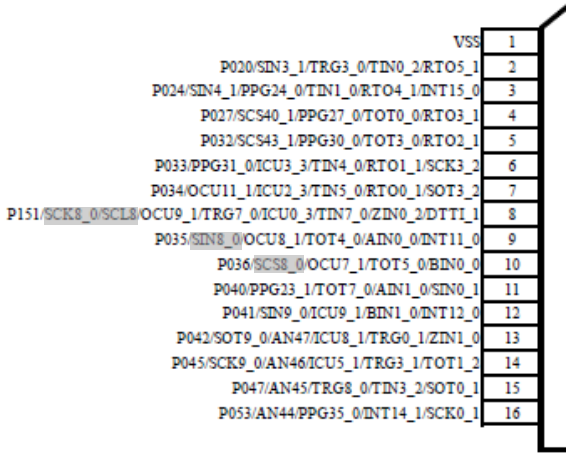
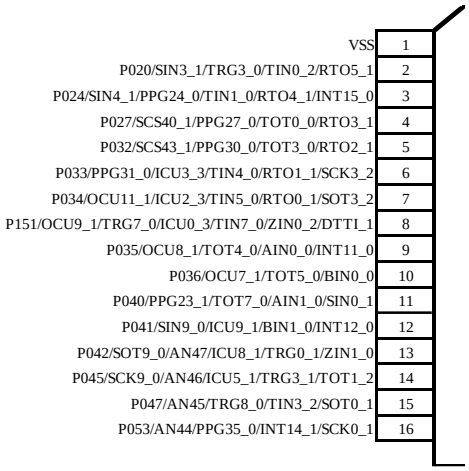

Stop mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
$I_{CC}H5$ [mA]
-50
0
50
100
150
T_A [°C]

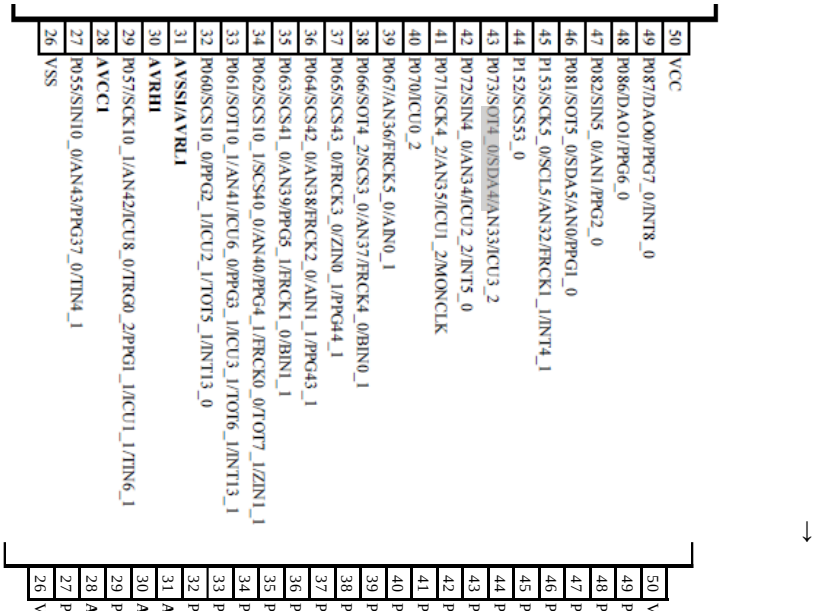
Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
MB91F526BWBPMC1	Yes	ON	ON	LQD・64 pin, Plastic
MB91F526BYBPMC1			OFF	
MB91F526BJBPMC1		OFF	ON	
MB91F526BLBPMC1			OFF	
MB91F525BWBPMC1		ON	ON	
MB91F525BYBPMC1			OFF	
MB91F525BJBPMC1		OFF	ON	
MB91F525BLBPMC1			OFF	
MB91F524BWBPMC1		ON	ON	
MB91F524BYBPMC1			OFF	
MB91F524BJBPMC1		OFF	ON	
MB91F524BLBPMC1			OFF	
MB91F523BWBPMC1		ON	ON	
MB91F523BYBPMC1			OFF	
MB91F523BJBPMC1		OFF	ON	
MB91F523BLBPMC1			OFF	
MB91F522BWBPMC1		ON	ON	
MB91F522BYBPMC1			OFF	
MB91F522BJBPMC1		OFF	ON	
MB91F522BLBPMC1			OFF	
MB91F526BSBPMC1	None	ON	ON	
MB91F526BUBPMC1			OFF	
MB91F526BHBPMC1		OFF	ON	
MB91F526BKBPMC1			OFF	
MB91F525BSBPMC1		ON	ON	
MB91F525BUBPMC1			OFF	
MB91F525BHBPMC1		OFF	ON	
MB91F525BKBPMC1			OFF	
MB91F524BSBPMC1		ON	ON	
MB91F524BUBPMC1			OFF	
MB91F524BHBPMC1		OFF	ON	
MB91F524BKBPMC1			OFF	
MB91F523BSBPMC1		ON	ON	
MB91F523BUBPMC1			OFF	
MB91F523BHBPMC1		OFF	ON	
MB91F523BKBPMC1			OFF	
MB91F522BSBPMC1		ON	ON	
MB91F522BUBPMC1			OFF	
MB91F522BHBPMC1		OFF	ON	
MB91F522BKBPMC1			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see Package Dimensions.

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
MB91F526KWDPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4 mm) Plastic
MB91F526KJDPMC1		OFF	ON	
MB91F525KWDPMC1		ON	ON	
MB91F525KJDPMC1		OFF	ON	
MB91F524KWDPMC1		ON	ON	
MB91F524KJDPMC1		OFF	ON	
MB91F523KWDPMC1		ON	ON	
MB91F523KJDPMC1		OFF	ON	
MB91F522KWDPMC1		ON	ON	
MB91F522KJDPMC1		OFF	ON	
MB91F526KSDPMC1	None	ON	ON	
MB91F526KHDPMC1		OFF	ON	
MB91F525KSDPMC1		ON	ON	
MB91F525KHDPMC1		OFF	ON	
MB91F524KSDPMC1		ON	ON	
MB91F524KHDPMC1		OFF	ON	
MB91F523KSDPMC1		ON	ON	
MB91F523KHDPMC1		OFF	ON	
MB91F522KSDPMC1		ON	ON	
MB91F522KHDPMC1		OFF	ON	
MB91F526JWDPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JJDPMC		OFF	ON	
MB91F525JWDPMC		ON	ON	
MB91F525JJDPMC		OFF	ON	
MB91F524JWDPMC		ON	ON	
MB91F524JJDPMC		OFF	ON	
MB91F523JWDPMC		ON	ON	
MB91F523JJDPMC		OFF	ON	
MB91F522JWDPMC		ON	ON	
MB91F522JJDPMC		OFF	ON	
MB91F526JSDPMC	None	ON	ON	
MB91F526JHDPMC		OFF	ON	
MB91F525JSDPMC		ON	ON	
MB91F525JHDPMC		OFF	ON	
MB91F524JSDPMC		ON	ON	
MB91F524JHDPMC		OFF	ON	
MB91F523JSDPMC		ON	ON	
MB91F523JHDPMC		OFF	ON	
MB91F522JSDPMC		ON	ON	
MB91F522JHDPMC		OFF	ON	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
MB91F526FWDPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FJDPMC		OFF	ON	
MB91F525FWDPMC		ON	ON	
MB91F525FJDPMC		OFF	ON	
MB91F524FWDPMC		ON	ON	
MB91F524FJDPMC		OFF	ON	
MB91F523FWDPMC		ON	ON	
MB91F523FJDPMC		OFF	ON	
MB91F522FWDPMC		ON	ON	
MB91F522FJDPMC		OFF	ON	
MB91F526FSDPMC	None	ON	ON	
MB91F526FHDPMC		OFF	ON	
MB91F525FSDPMC		ON	ON	
MB91F525FHDPMC		OFF	ON	
MB91F524FSDPMC		ON	ON	
MB91F524FHDPMC		OFF	ON	
MB91F523FSDPMC		ON	ON	
MB91F523FHDPMC		OFF	ON	
MB91F522FSDPMC		ON	ON	
MB91F522FHDPMC		OFF	ON	
MB91F526DWDPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DJDPMC		OFF	ON	
MB91F525DWDPMC		ON	ON	
MB91F525DJDPMC		OFF	ON	
MB91F524DWDPMC		ON	ON	
MB91F524DJDPMC		OFF	ON	
MB91F523DWDPMC		ON	ON	
MB91F523DJDPMC		OFF	ON	
MB91F522DWDPMC		ON	ON	
MB91F522DJDPMC		OFF	ON	
MB91F526DSDPMC	None	ON	ON	
MB91F526DHDPMC		OFF	ON	
MB91F525DSDPMC		ON	ON	
MB91F525DHDPMC		OFF	ON	
MB91F524DSDPMC		ON	ON	
MB91F524DHDPMC		OFF	ON	
MB91F523DSDPMC		ON	ON	
MB91F523DHDPMC		OFF	ON	
MB91F522DSDPMC		ON	ON	
MB91F522DHDPMC		OFF	ON	

Page	Section	Change Results
13	■Pin Assignment MB91F52xB	Signals indicated by the shading below deleted in Figure. - Left side  ↓ 

Page	Section	Change Results
15	■Pin Assignment MB91F52xF	Signals indicated by the shading below deleted in Figure. (Error) - Bottom  50 VCC 49 P087/DA00/PPG7_0/INT8_0 48 P086/DA01/PPG6_0 47 P082/SIN5_0/AN1/PPG2_0 46 P081/SOT5_0/SDA5/AN0/PPG1_0 45 P153/SCK5_0/SCL5/AN32/FRCK1_1/INT4_1 44 P152/SCS3_0 43 P073/SOT4_0/SDA4/AN33/ICU3_2 42 P072/SIN4_0/AN34/ICU2_2/INT5_0 41 P071/SCK4_2/AN35/ICU1_2/MONCLK 40 P070/ICU0_2 39 P067/AN36/FRCK5_0/AIN0_1 38 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 37 P065/SCS43_0/FRCK3_0/ZIN0_1/PPG44_1 36 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 35 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 34 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 33 P061/SOT10_1/AN41/ICU6_0/PPG3_1/ICU3_1/TOT6_1/INT13_1 32 P060/SCS10_0/PPG2_1/ICU2_1/TOT5_1/INT13_0 31 AVSS1/AVRL1 30 AVRH1 29 P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 28 AVCC1 27 P055/SIN10_0/AN43/PPG37_0/TIN4_1 26 VSS ↓ 26 VSS 27 P055/SIN10_0/AN43/PPG37_0/TIN4_1 28 AVCC1 29 P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 30 AVRH1 31 AVSS1/AVRL1 32 P060/SCS10_0/PPG2_1/ICU2_1/TOT5_1/INT13_0 33 P061/SOT10_1/AN41/ICU6_0/PPG3_1/ICU3_1/TOT6_1/INT13_1 34 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 35 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 36 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 37 P065/SCS43_0/FRCK3_0/ZIN0_1/PPG44_1 38 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 39 P067/AN36/FRCK5_0/AIN0_1 40 P070/ICU0_2 41 P071/SCK4_2/AN35/ICU1_2/MONCLK 42 P072/SIN4_0/AN34/ICU2_2/INT5_0 43 P073/AN33/ICU3_2 44 P152/SCS3_0 45 P153/SCK5_0/SCL5/AN32/FRCK1_1/INT4_1 46 P081/SOT5_0/SDA5/AN0/PPG1_0 47 P082/SIN5_0/AN1/PPG2_0 48 P086/DA01/PPG6_0 49 P087/DA00/PPG7_0/INT8_0 50 VCC

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>33</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94</td><td rowspan="5">111</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75</td><td rowspan="4">95</td><td rowspan="4">112</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17</td></tr>
<tr><td>SOT1_0</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94 *1</td><td rowspan="5">111 *1</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16 *4, *5</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1 *4</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75 *1</td><td rowspan="4">95 *1</td><td rowspan="4">112 *1</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17 *3, *4, *5</td></tr>
<tr><td>SOT1_0 *3</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>34, 35</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">113 *1</td><td rowspan="4">133</td><td rowspan="4">161</td><td>P002</td></tr>
<tr><td>D18 *5</td></tr>
<tr><td>SCK1_0</td></tr>
<tr><td>TIOB0_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">76 *1</td><td rowspan="5">96 *1</td><td rowspan="5">114 *1</td><td rowspan="5">134</td><td rowspan="5">162</td><td>P003</td></tr>
<tr><td>D19 *3, *4, *5</td></tr>
<tr><td>SIN2_0</td></tr>
<tr><td>TIOB1_1</td></tr>
<tr><td>INT3_0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">135</td><td rowspan="3">163</td><td>P004</td></tr>
<tr><td>D20</td></tr>
<tr><td>SOT2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">164</td><td>P164</td></tr>
<tr><td>PPG32_1</td></tr>
<tr><td rowspan="7">61 *1</td><td rowspan="7">77 *1</td><td rowspan="7">97 *1</td><td rowspan="7">115 *1</td><td rowspan="7">136 *1</td><td rowspan="7">165 *1</td><td>P005</td></tr>
<tr><td>D21 *2, *3, *4, *5</td></tr>
<tr><td>SCK2_0 *2</td></tr>
<tr><td>ADTG0_1</td></tr>
<tr><td>INT7_1</td></tr>
<tr><td>RX2(64) *4, *5, *6, *7</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">166</td><td>P165</td></tr>
<tr><td>PPG33_1</td></tr>
<tr><td rowspan="7">62 *1</td><td rowspan="7">78 *1</td><td rowspan="7">98 *1</td><td rowspan="7">116 *1</td><td rowspan="7">137 *1</td><td rowspan="7">167 *1</td><td>P006</td></tr>
<tr><td>D22 *2, *3, *4, *5</td></tr>
<tr><td>SCS2_0 *2</td></tr>
<tr><td>ADTG1_1</td></tr>
<tr><td>INT2_1</td></tr>
<tr><td>TX2(64) *4, *5, *6, *7</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">117 *1</td><td rowspan="2">138</td><td rowspan="2">168</td><td>P007</td></tr>
<tr><td>D23 *5</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">169</td><td>P166</td></tr>
<tr><td>PPG34_1</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">118 *1</td><td rowspan="2">139</td><td rowspan="2">170</td><td>P010</td></tr>
<tr><td>D24 *5</td></tr>
<tr><td rowspan="7">63 *1</td><td rowspan="7">79 *1</td><td rowspan="7">99 *1</td><td rowspan="7">119 *1</td><td rowspan="7">140</td><td rowspan="7">171</td><td>P011</td></tr>
<tr><td>WOT</td></tr>
<tr><td>D25 *2, *3, *4, *5</td></tr>
<tr><td>SOT2_1 *2</td></tr>
<tr><td>TIOA0_0 *2, *3, *4</td></tr>
<tr><td>INT3_1</td></tr>
</table></td></tr>
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