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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526dsdpmc-gs-ere2

Product Lineup Comparison 120 Pins

	MB91F522J	MB91F523J	MB91F524J	MB91F525J	MB91F526J
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)	64 KB				
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)	None				
DMA Transfer	16 ch				
16-bit Base Timer	2 ch				
Free-run Timer	16 bit × 3 ch, 32 bit × 3 ch				
Input capture	16 bit × 4 ch, 32 bit × 6 ch				
Output Compare	16 bit × 6 ch, 32 bit × 6 ch				
16-bit Reload Timer	8 ch				
PPG	16 bit × 38 ch				
Up/down Counter	2 ch				
Clock Supervisor	Yes				
External Interrupt	8 ch × 2 units				
A/D converter	12 bit × 26 ch (1 unit), 12 bit × 16 ch (1 unit)				
D/A converter (8 bit)	2 ch				
Multi-Function Serial Interface	12 ch*1				
CAN	64 msg × 2 ch/128 msg × 1 ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	96 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6 ch				
Operation guaranteed temperature (T_A)	-40 °C to +125 °C				
Power supply	2.7 V to 5.5 V *2				
Package	LQM120				

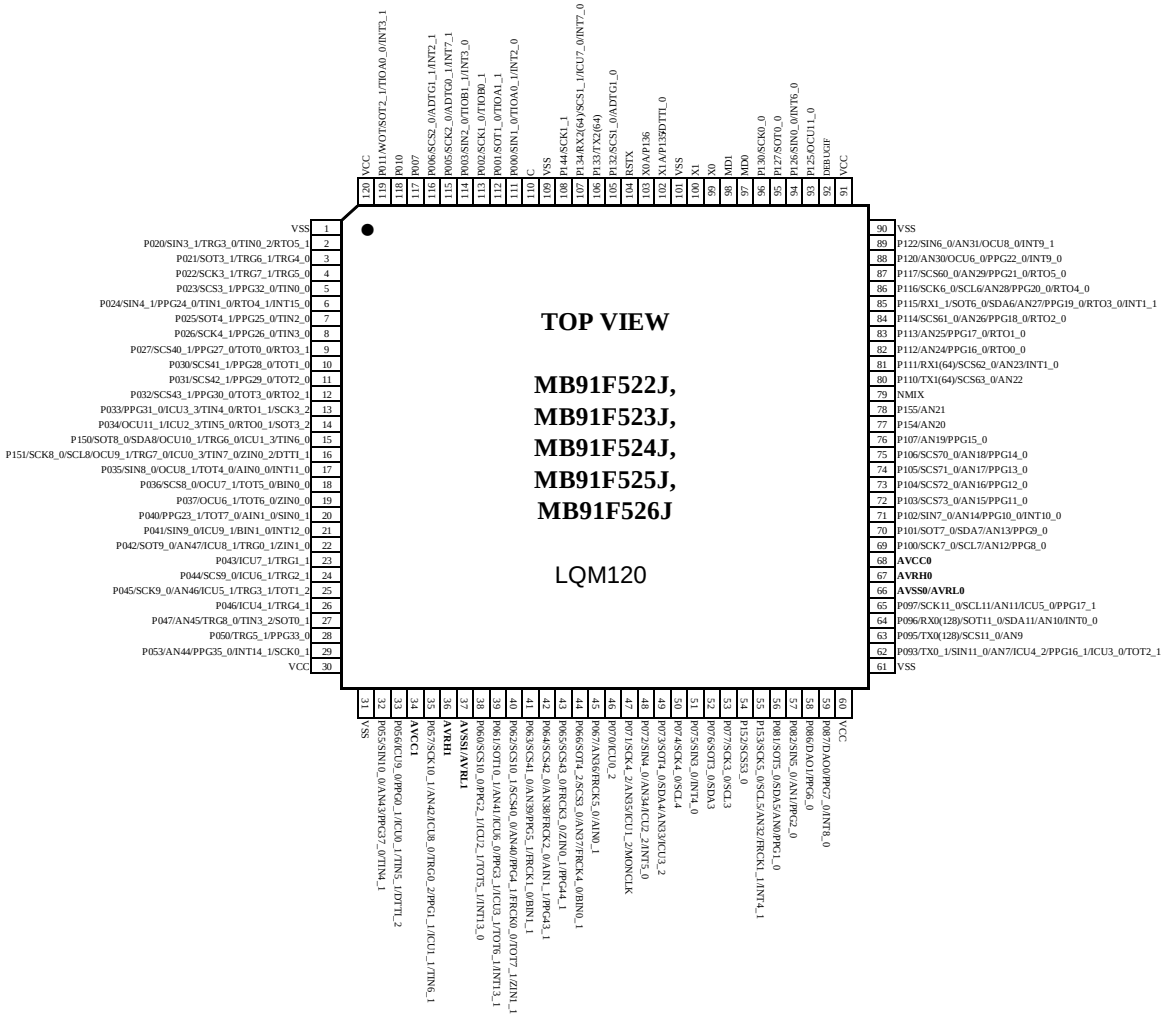
*1: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

MB91F52xJ

MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J

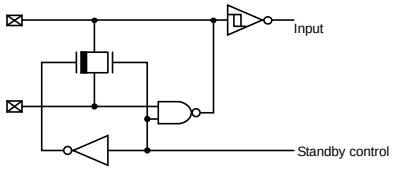
(TOP VIEW)



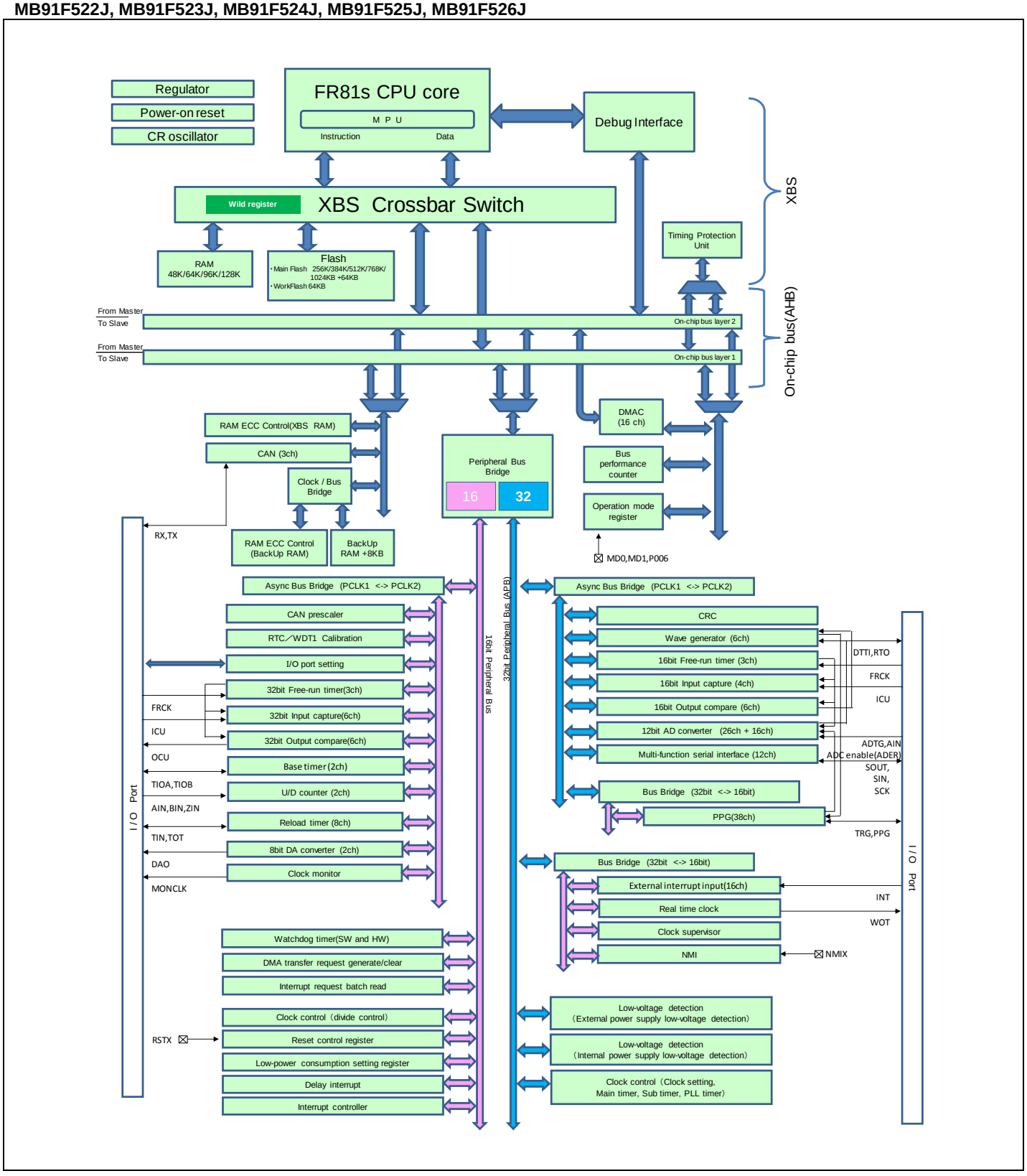
* In a single clock product, pin 102 and pin 103 are the general-purpose ports.

3. Pin Description

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	2	2	P015	-	A	General-purpose I/O port
						D29	-		External bus data bit29 I/O (0)
						TRG0_0	-		PPG trigger 0 input (0)
-	-	-	-	3	3	P016	-	A	General-purpose I/O port
						D30	-		External bus data bit30 I/O (0)
						TRG1_0	-		PPG trigger 1 input (0)
-	-	-	-	-	4	P170	-	A	General-purpose I/O port
						PPG36_1	-		PPG ch.36 output (1)
-	-	-	-	4	5	P017	-	A	General-purpose I/O port
						D31	-		External bus data bit31 I/O (0)
						TRG2_0	-		PPG trigger 2 input (0)
-	-	-	-	-	6	P171	-	A	General-purpose I/O port
						PPG37_1	-		PPG ch.37 output (1)
2 *1	2 *1	2 *1	2 *1	5	7	P020	-	F	General-purpose I/O port
						ASX *2, *3, *4, *5	-		External bus/Address strobe output
						SIN3_1	-		Multi-function serial ch.3 serial data input (1)
						TRG3_0	-		PPG trigger 3 input (0)
						TIN0_2	-		Reload timer ch.0 event input (2)
						RTO5_1	-		Waveform generator ch.5 output pin (1)
-	-	-	3 *1	6	8	P021	-	A	General-purpose I/O port
						CS0X *5	-		External bus chip select 0 output
						SOT3_1	-		Multi-function serial ch.3 serial data output (1)
						TRG6_1	-		PPG trigger 6 input (1)
						TRG4_0	-		PPG trigger 4 input (0)
-	-	-	4 *1	7	9	P022	-	F	General-purpose I/O port
						CS1X *5	-		External bus chip select 1 output
						SCK3_1	-		Multi-function serial ch.3 clock I/O (1)
						TRG7_1	-		PPG trigger 7 input (1)
						TRG5_0	-		PPG trigger 5 input (0)
-	-	-	5 *1	8	10	P023	-	A	General-purpose I/O port
						RDX *5	-		External bus/Read strobe output
						SCS3_1	-		Serial chip select 3 output (1)
						PPG32_0	-		PPG ch.32 output (0)
						TIN0_0	-		Reload timer ch.0 event input (0)

Type	Circuit	Remarks
O		•Sub oscillation I/O

MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000640H	ACR0 [R/W] W -------- -------- -------- 01--00--				External Bus Interface [S]
000644H	ACR1 [R/W] W -------- -------- -------- XX--XX--				
000648H	ACR2 [R/W] W -------- -------- -------- XX--XX--				
00064CH	ACR3 [R/W] W -------- -------- -------- XX--XX--				
000650H to 00067CH	—	—	—	—	Reserved [S]
000680H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]
000684H	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688H	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				External Bus Interface [S]
00068CH	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690H to 0006FCH	—	—	—	—	Reserved [S]
000700H to 00070CH	—	—	—	—	Reserved
000710H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
00071CH	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720H to 0007F8H	—	—	—	—	Reserved
0007FCH	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register
000800H to 00083CH	—	—	—	—	Reserved [S]
000840H	FCTLR [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844H to 000854H	—	—	—	—	Reserved [S]
000858H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
00085CH to 00087CH	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000FDC$_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 32-bit ICU
000FE0$_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4$_H$	—	—	—	ICS67 [R/W] B,H,W 00000000	
000FE8$_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
000FEC$_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FF0$_H$	—	—	—	ICS89 [R/W] B,H,W 00000000	
000FF4$_H$	MSCY8 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU Cycle measurement data register 89
000FF8$_H$	MSCY9 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FFC$_H$	—	—	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W ------00	Cycle and pulse width measurement control 89
001000$_H$	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Clock Control
001004$_H$ to 00112C$_H$	—	—	—	—	Reserved
001130$_H$	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit
001134$_H$	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111				
001138$_H$	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000				
00113C$_H$	CRCR [R] B,H,W 11111111 11111111 11111111 11111111				
001140$_H$ to 0011FC$_H$	—	—	—	—	Reserved
001200$_H$	TCGS [R/W] B,H,W ------00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation
001204$_H$	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 0
001208$_H$	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 --------				
00120C$_H$	CPCLRB1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 1
001210$_H$	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 --------				
001214$_H$	CPCLRB2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 2
001218$_H$	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 --------				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0012A0H	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0012A4H	TMRR2 [R/W] H,W 00000000 00000001		—	—	
0012A8H	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—	
0012ACH	—	DTIR0 [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000	
0012B0H	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1	
0012B4H	PICS0 [R/W] B,H,W 000000-- -------- -------- --------				
0012B8H to 0012CCH	—	—	—	—	Reserved
0012D0H	FRS5 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
0012D4H	FRS6 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
0012D8H	FRS7 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012DCH to 0012FCH	—	—	—	—	Reserved
001300H	—				Reserved
001304H	ADTSS0[R/W] B,H,W -------0	—	—	—	12-bit A/D converter 1/2 unit
001308H	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000				
00130CH	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
001310H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
001314H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
001318H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
00131CH	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
001320H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
001324H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001328H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

Interrupt Factor	Interrupt number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) / Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed) / Multi-function serial interface ch.5 (status)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed) / Multi-function serial interface ch.6 (status)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1 / RAM diagnosis end / RAM initialization completion / Error generation during RAM diagnosis / Backup RAM diagnosis end / Backup RAM initialization completion / Error generation during Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2 / Up/down counter 0 / Up/down counter 1	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed) / Multi-function serial interface ch.7 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit Free-running timer 0 (0 detection) / (compare clear) / Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/21/30/31 / 16-bit Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG 2/3/12/13/23/32/43 / 16-bit Free-run timer 2 (0 detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

144 Pins

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

DC Characteristics

(T_A: -40 °C to +105 °C, V_{CC} = AVcc = 5.0 V ± 10 %/3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at normal operation		-	60	80	mA	
			Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at Flash write		-	70	90	mA	
			Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at Flash erase		-	70	90	mA	
			Operating frequency F_{CP} = 64 MHz, Fcpp = 32 MHz, at normal operation		-	54	71	mA	
			Operating frequency F_{CP} = 64 MHz, Fcpp = 32 MHz, at Flash write		-	64	81	mA	
			Operating frequency F_{CP} = 64 MHz, Fcpp = 32 MHz, at Flash erase		-	64	81	mA	
			Operating frequency F_{CP} = 48 MHz, Fcpp = 24 MHz, at normal operation		-	46	62	mA	
			Operating frequency F_{CP} = 48 MHz, Fcpp = 24 MHz, at Flash write		-	56	72	mA	
			Operating frequency F_{CP} = 48 MHz, Fcpp = 24 MHz, at Flash erase		-	56	72	mA	
	$I_{CCS}5$		Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at CPU sleep mode		-	45	61	mA	
	$I_{CCBS}5$		Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at bus sleep mode		-	23	51	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4 MHz T_A = +25 °C*	-	1500	2610	µA	
				When using built-in CR clock 50 kHz T_A = +25 °C*	-	450	2000		
				When using sub clock 32 kHz T_A = +25 °C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A = +25 °C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4 MHz T_A = +25 °C*	-	1100	1300	µA	LVD/ RTC operation, Backup RAM 8 KB retention
				When using built-in CR clock 50 kHz , T_A = +25 °C*	-	77	267		
				When using sub clock 32 kHz T_A = +25 °C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A = +25 °C*	-	74	265	µA	Backup RAM 8 KB retention

(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR : MD0 = 0, SMR: SCINV = 0, SCR:SPI = 0

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V±0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L = 50 pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L = 50 pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

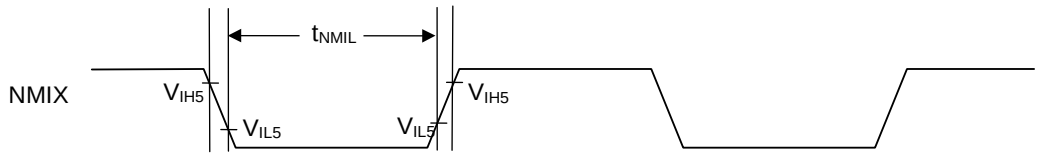
See Hardware Manual for details.

(7) NMI input timing

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

・ NMIX input timing



(8) Low voltage detection (External low-voltage detection)

(T_A: -40 °C to +125 °C, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	2.7	-	5.5	V	
Detection voltage*3	V_{DL}		*1	-8%	LVD5F_SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Hysteresis width	V_{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	Td	-		-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).

*3: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V).
This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7 V).
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT = 0 *2
SYSCLK↑→ data output time	t_{CHDV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.
SYSCLK↑→ address output time	t_{CHMAV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: □ Set CSWR and CSRD to 2 or more. □ ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

*1: Please use it with external load capacity 12 pF or less for VCC = 3.3 V ± 0.3 V (40 MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

D/A Converter

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	–	–	–	8	bit	
Differential linearity error	-	-	–	–	–	± 3.0	LSB	
Conversion time	-	-	–	0.47	0.58	0.69	µs	C_L = 20
			–	2.37	2.90	3.43	µs	C_L = 100
Output impedance	Ro	DA0, DA1	–	3.1	3.8	4.5	kΩ	
Power supply current *1	IA	AVCC	–	–	475	580	µA	Each channel
	IAH	AVCC	–	–	–	7.5	µA	When powerdown Each channel

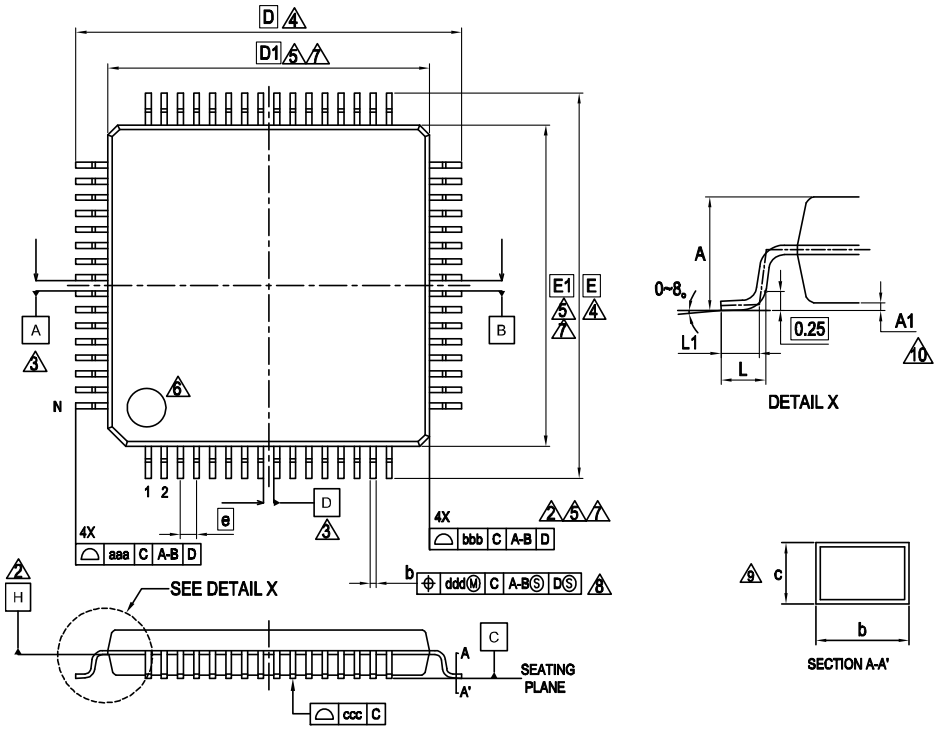
*1: The power supply current described only current value on D/A converter.
The total AVcc current value must be calculated the power supply current for D/A converter and A/D converter.

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
MB91F526BWEPMC1	Yes	ON	ON	LQE・64 pin, Plastic
MB91F526BJEPMC1		OFF	ON	
MB91F525BWEPMC1		ON	ON	
MB91F525BJEPMC1		OFF	ON	
MB91F524BWEPMC1		ON	ON	
MB91F524BJEPMC1		OFF	ON	
MB91F523BWEPMC1		ON	ON	
MB91F523BJEPMC1		OFF	ON	
MB91F522BWEPMC1		ON	ON	
MB91F522BJEPMC1		OFF	ON	
MB91F526BSEPMC1	None	ON	ON	
MB91F526BHEPMC1		OFF	ON	
MB91F525BSEPMC1		ON	ON	
MB91F525BHEPMC1		OFF	ON	
MB91F524BSEPMC1		ON	ON	
MB91F524BHEPMC1		OFF	ON	
MB91F523BSEPMC1		ON	ON	
MB91F523BHEPMC1		OFF	ON	
MB91F522BSEPMC1		ON	ON	
MB91F522BHEPMC1		OFF	ON	

*: For details of the package, see Package Dimensions.

17. Package Dimensions

LQD064 , 64 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQD64		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	64		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
23, 24	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
15 *1	18 *1	23 *1	27 *1	30	37	P047
						A17 *2, *3, *4, *5
						AN45
						TRG8_0
						TIN3_2
						SOT0_1
-	-	-	-	-	38	P177
						TRG11_0
-	-	-	28 *1	31	39	P050
						A18 *5
						TRG5_1
						PPG33_0
-	-	-	-	32	40	P051
						A19
						TRG9_0
-	-	-	-	33	41	P052
						A20
						PPG34_0
						INT14_0
16 *1	19 *1	24 *1	29 *1	34	42	P053
						A21 *2, *3, *4, *5
						AN44
						PPG35_0
						INT14_1
						SCK0_1
-	-	-	-	35	43	P054
						SYSCLK
						PPG36_0
17 *1	22 *1	27 *1	32 *1	38	46	P055
						CS2X *2, *3, *4, *5
						SIN10_0
						AN43
						PPG37_0
						TIN4_1
-	-	-	33 *1	39	49	P056
						CS3X *5
						ICU9_0
						PPG0_1
						ICU0_1
						TIN5_1
						DTTI_2

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>24</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table><tr><td>Function*2</td></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External Bus chip select 2 output pin(0)</td></tr><tr><td>Multi-function serial ch.10 serial data input pin(0)</td></tr><tr><td>ADC analog 43 input pin</td></tr><tr><td>PPG ch.37 output pin(0)</td></tr><tr><td>Reload timer ch.4 event input pin(1)</td></tr></table>
(Correct)
<table><tr><td>Function*9</td></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External Bus chip select 2 output pin</td></tr><tr><td>Multi-function serial ch.10 serial data input pin(0)</td></tr><tr><td>ADC analog 43 input pin</td></tr><tr><td>PPG ch.37 output pin(0)</td></tr><tr><td>Reload timer ch.4 event input pin(1)</td></tr></table></td></tr>
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