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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 42x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526jsepmc-gse1

Pin No.						Pin Name	Polarity	I/O Circuit types*8	Function*9
64	80	100	120	144	176				
61 *1	77 *1	97 *1	115 *1	136 *1	165 *1	P005	-	F	General-purpose I/O port
						D21 *2, *3, *4, *5	-		External bus data bit21 I/O (0)
						SCK2_0 *2	-		Multi-function serial ch.2 clock I/O (0)
						ADTG0_1	-		A/D converter external trigger input 0 (1)
						INT7_1	-		INT7 External interrupt input (1)
						RX2(64) *4, *5, *6, *7	-		CAN reception data 2 input
-	-	-	-	-	166	P165	-	A	General-purpose I/O port
						PPG33_1	-		PPG ch.33 output (1)
62 *1	78 *1	98 *1	116 *1	137 *1	167 *1	P006	-	A	General-purpose I/O port
						D22 *2, *3, *4, *5	-		External bus data bit22 I/O (0)
						SCS2_0 *2	-		Serial chip select 2 I/O (0)
						ADTG1_1	-		A/D converter external trigger input 1 (1)
						INT2_1	-		INT2 External interrupt input (1)
						TX2(64) *4, *5, *6, *7	-		CAN transmission data 2 output
-	-	-	117 *1	138	168	P007	-	A	General-purpose I/O port
						D23 *5	-		External bus data bit23 I/O
-	-	-	-	-	169	P166	-	A	General-purpose I/O port
						PPG34_1	-		PPG ch.34 output (1)
-	-	-	118 *1	139	170	P010	-	A	General-purpose I/O port
						D24 *5	-		External bus data bit24 I/O
63 *1	79 *1	99 *1	119 *1	140	171	P011	-	A	General-purpose I/O port
						WOT	-		RTC output signal
						D25 *2, *3, *4, *5	-		External bus data bit25 I/O
						SOT2_1 *2	-		Multi-function serial ch.2 serial data output (1)
						TIOA0_0 *2, *3, *4	-		TIOA output of Base timer ch.0 (0)
						INT3_1	-		INT3 External interrupt input (1)
-	-	-	-	141	172	P012	-	A	General-purpose I/O port
						D26	-		External bus data bit26 I/O
						TIOB0_0	-		TIOB input of Base timer ch.0 (0)
-	-	-	-	-	173	P167	-	A	General-purpose I/O port
						PPG35_1	-		PPG ch.35 output (1)
-	-	-	-	142	174	P013	-	A	General-purpose I/O port
						D27	-		External bus data bit27 I/O
						TIOA1_0	-		TIOA I/O of Base timer ch.1 (0)
-	-	-	-	143	175	P014	-	A	General-purpose I/O port
						D28	-		External bus data bit28 I/O
						TIOB1_0	-		TIOB input of Base timer ch.1 (0)
18	23	28	34	40	50	AVCC1	-	-	Analog power supply for AD/DA convertor unit1
39	47	58	68	84	103	AVCC0	-	-	Analog power supply for AD/DA convertor unit0

- Crystal oscillation circuit
  An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

  The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

- Mode pins (MD1, MD0)
  Connect the MD1 and MD0 mode pins to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

- During power-on
  To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

- Notes during PLL clock operation
  When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

- Treatment of A/D converter power supply pins
  Connect the pins to have AVCC = AVRH = VCC and AVSS/AVRL = VSS even if the A/D converter is not used.

- Notes on using external clock
  An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

- Power-on sequence of A/D converter analog inputs
  Be sure to turn on the digital power supply (Vcc) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN47). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc). When the AVRH pin voltage is turned on or off, it must not exceed AVCC. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

- Treatment of C pin
  This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

  Note: Please see the latest data sheet for a detailed specification of the operation voltage.

- Function switching of a multiplexed port
  To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see " I/O PORTS" in the hardware manual.

- Low-power consumption mode
  To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL" in the hardware manual.

  Take the following notes when using a monitor debugger.

  - Do not set a break point for the low-power consumption transition program.
  - Do not execute an operation step for the low-power consumption transition program.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0015B4H	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	12-bit A/D converter 2/2 unit
0015B8H	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
0015BCH	—	—	—	—	
0015C0H	—	—	—	—	
0015C4H	ADPRTF1 [R] B,H,W -------- -------- 00000000 00000000				
0015C8H	ADEOCF1 [R] B,H,W -------- -------- 11111111 11111111				
0015CCH	ADCS1 [R] B,H,W 0------- --------		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
0015D0H	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	
0015D4H to 00174CH	—	—	—	—	Reserved
001750H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I²C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754H	— /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001758H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175CH	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4		
001760H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3	
001764H	—	— /(SCSFR20) [R/W] B,H,W -------- *3	— /(SCSFR10) [R/W] B,H,W -------- *3	— /(SCSFR00) [R/W] B,H,W -------- *3	
001768H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176CH	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -------- *2	— /(ISBA0) [R/W] B,H,W -------- *2	
001770H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001884H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	Multi-UART7
001888H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
00188CH	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
00189CH	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
0018A0H	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
0018A4H	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
0018A8H	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
0018ACH	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	
0018B0H	FCR18[R/W] B,H,W ---00100	FCR08[R/W] B,H,W -0000000	FBYTE8[R/W] B,H,W 00000000 00000000		Multi-UART8
0018B4H	FTICR8[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B78H	PCN216 [R/W] B,H,W --000000 -----110		PSDR16 [R/W] H,W 00000000 00000000		PPG16
001B7CH	PTPC16 [R/W] H,W 00000000 00000000		—	—	
001B80H	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
001B84H	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
001B88H	PCN217 [R/W] B,H,W --000000 -----110		PSDR17 [R/W] H,W 00000000 00000000		
001B8CH	PTPC17 [R/W] H,W 00000000 00000000		—	—	
001B90H	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
001B94H	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
001B98H	PCN218 [R/W] B,H,W --000000 -----110		PSDR18 [R/W] H,W 00000000 00000000		
001B9CH	PTPC18 [R/W] H,W 00000000 00000000		—	—	
001BA0H	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
001BA4H	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
001BA8H	PCN219 [R/W] B,H,W --000000 -----110		PSDR19 [R/W] H,W 00000000 00000000		
001BACH	PTPC19 [R/W] H,W 00000000 00000000		—	—	
001BB0H	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
001BB4H	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
001BB8H	PCN220 [R/W] B,H,W --000000 -----110		PSDR20 [R/W] H,W 00000000 00000000		
001BBCH	PTPC20 [R/W] H,W 00000000 00000000		—	—	
001BC0H	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
001BC4H	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
001BC8H	PCN221 [R/W] B,H,W --000000 -----110		PSDR21 [R/W] H,W 00000000 00000000		
001BCCH	PTPC21 [R/W] H,W 00000000 00000000		—	—	PPG21

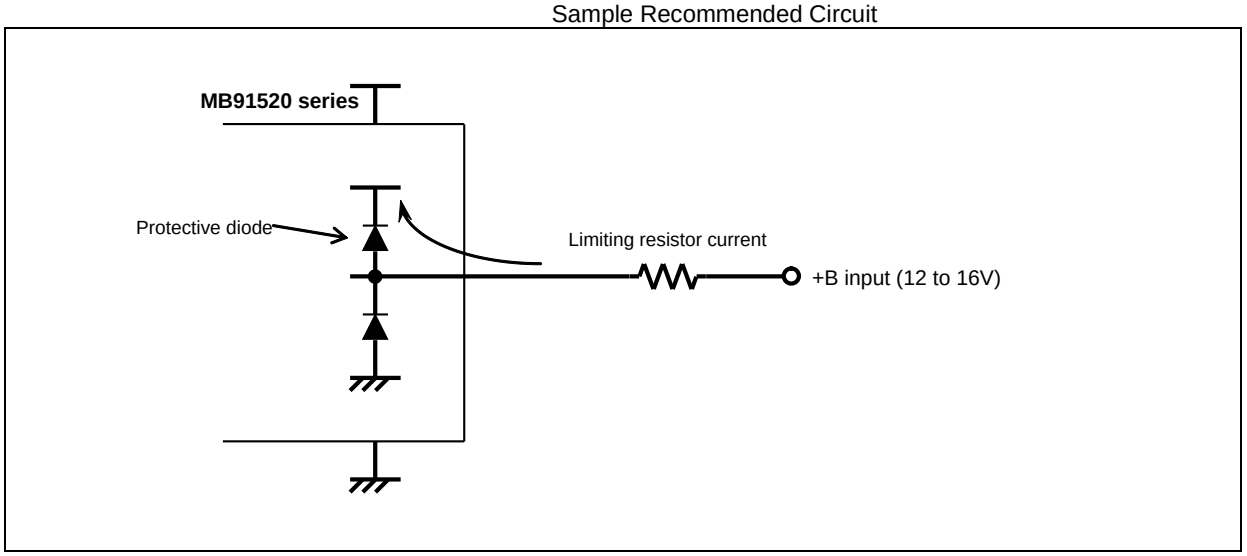
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C30H	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
001C34H	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
001C38H	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
001C3CH	PTPC28 [R/W] H,W 00000000 00000000		—	—	
001C40H	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
001C44H	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
001C48H	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
001C4CH	PTPC29 [R/W] H,W 00000000 00000000		—	—	
001C50H	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
001C54H	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
001C58H	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
001C5CH	PTPC30 [R/W] H,W 00000000 00000000		—	—	
001C60H	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
001C64H	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
001C68H	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
001C6CH	PTPC31 [R/W] H,W 00000000 00000000		—	—	
001C70H	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
001C74H	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		
001C78H	PCN232 [R/W] B,H,W --000000 -----110		PSDR32 [R/W] H,W 00000000 00000000		PPG32
001C7CH	PTPC32 [R/W] H,W 00000000 00000000		—	—	
001C80H	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXX XXXXXXXX		PPG33
001C84H	PDUT33 [W] H,W XXXXXXXX XXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
001C88H	PCN233 [R/W] B,H,W --000000 -----110		PSDR33 [R/W] H,W 00000000 00000000		PPG33
001C8CH	PTPC33 [R/W] H,W 00000000 00000000		—	—	

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344_H	$000FFF44_H$	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338_H	$000FFF38_H$	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334_H	$000FFF34_H$	34*5
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330_H	$000FFF30_H$	35*5
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU 6 (fetching/measurement)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)	53	35	ICR37	328_H	$000FFF28_H$	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324_H	$000FFF24_H$	38*1
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320_H	$000FFF20_H$	39
WG dead timer underflow 0 / 1/ 2						
WG dead timer reload 0 / 1/ 2						
WG DTTI 0						
32-bit ICU4 (fetching/measurement)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
Multi-function serial interface ch.11 (transmission completed)						

*8: It is a standard when four-layer substrate is used.

*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample Recommended Circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0 V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3 V is used)
		2.7	5.5	V	Operation guarantee range*1
Smoothing capacitor *2	C_S	4.7 (tolerance within ±50 %)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative.
The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the

DC Characteristics

(T_A: -40 °C to +105 °C, V_{CC} = AVcc = 5.0 V ± 10 %/3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at normal operation		-	60	80	mA	
			Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at Flash write		-	70	90	mA	
			Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at Flash erase		-	70	90	mA	
			Operating frequency F_{CP} = 64 MHz, Fcpp = 32 MHz, at normal operation		-	54	71	mA	
			Operating frequency F_{CP} = 64 MHz, Fcpp = 32 MHz, at Flash write		-	64	81	mA	
			Operating frequency F_{CP} = 64 MHz, Fcpp = 32 MHz, at Flash erase		-	64	81	mA	
			Operating frequency F_{CP} = 48 MHz, Fcpp = 24 MHz, at normal operation		-	46	62	mA	
			Operating frequency F_{CP} = 48 MHz, Fcpp = 24 MHz, at Flash write		-	56	72	mA	
			Operating frequency F_{CP} = 48 MHz, Fcpp = 24 MHz, at Flash erase		-	56	72	mA	
	$I_{CCS}5$		Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at CPU sleep mode		-	45	61	mA	
	$I_{CCBS}5$		Operating frequency F_{CP} = 80 MHz, Fcpp = 40 MHz, at bus sleep mode		-	23	51	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4 MHz T_A = +25 °C*	-	1500	2610	µA	
				When using built-in CR clock 50 kHz T_A = +25 °C*	-	450	2000		
				When using sub clock 32 kHz T_A = +25 °C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A = +25 °C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4 MHz T_A = +25 °C*	-	1100	1300	µA	LVD/ RTC operation, Backup RAM 8 KB retention
				When using built-in CR clock 50 kHz , T_A = +25 °C*	-	77	267		
				When using sub clock 32 kHz T_A = +25 °C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A = +25 °C*	-	74	265	µA	Backup RAM 8 KB retention

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/Vcc = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	All input pins	V_{CC} = AV_{CC} = 5.5 V V_{SS}<V_I<V_{CC}	-5	-	5	µA	
Input capacitance 1	C_{IN1}	Other than VCC,VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R_{UP1}	RSTX, NMIX	V_{CC} = 5.0 V ± 10 %	25	-	100	kΩ	
			Vcc = 3.3 V ± 0.3 V	45	-	140		
	R_{UP2}	P073,074 076,077	V_{CC} = 5.0 V ± 10 %	25	-	60		
			Vcc = 3.3 V ± 0.3 V	33	-	90		
	R_{UP3}	Port pin other than P035, 041,073,074, 076,077,093, 122	V_{CC} = 5.0 V ± 10 %	25	-	100	kΩ	
			Vcc = 3.3 V ± 0.3 V	45	-	140		
“H” level output voltage	V_{OH1}	Normal output pin	Vcc = 4.5 V I_{OH} = -4.0 mA	V_{CC} -0.5	-	V_{CC}	V	
			Vcc = 3.0 V I_{OH} = -2.0 mA					
	V_{OH2}	P073,074,076, 077	Vcc = 4.5 V I_{OH} = -3.0 mA	V_{CC} -0.5	-	V_{CC}	V	I^2C pin output
	V_{OH3}	P103 to 106	Vcc = 4.5 V I_{OH} = -12.0 mA	V_{CC} -0.5	-	V_{CC}	V	
			Vcc = 3.0 V I_{OH} = -8.0 mA					
“L” level output voltage	V_{OL1}	Normal output pin	Vcc = 4.5 V I_{OL} = 4.0 mA	0	-	0.4	V	
			Vcc = 3.0 V I_{OL} = 2.0 mA					
	V_{OL2}	P073,074,076, 077	Vcc = 4.5 V I_{OL} = 3.0 mA	0	-	0.4	V	I^2C pin output
	V_{OL3}	P103 to 106	Vcc = 4.5 V I_{OL} = 12.0 mA	0	-	0.4	V	
			Vcc = 3.0 V I_{OL} = 8.0 mA					

(4-1-4) Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 0, SMR:SCINV = 1, SCR:SPI = 1
(T_A:-40 °C to +125 °C, V_{CC} = A V_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ±0.3 V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L = 50 pF
SCK↓→ SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK↑setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK↑→ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
SOT→SCK↑ delay time	t_{SOVHI}	SCK0 to SCK11 SOT0 to SOT11		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L = 50 pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK↑setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK↑→ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.
See Hardware Manual for details.

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L = 50 pF
SCK↑→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2 , SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L = 50 pF
SCK↓→SCS↓ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

*1: t_{CSSU} = SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD7-0×Serial chip select timing operating clock

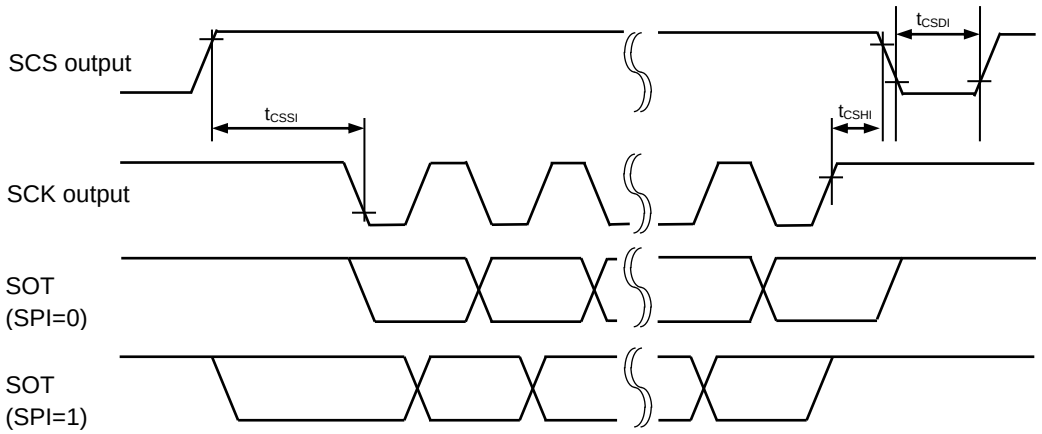
*3: t_{CSDS} = SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

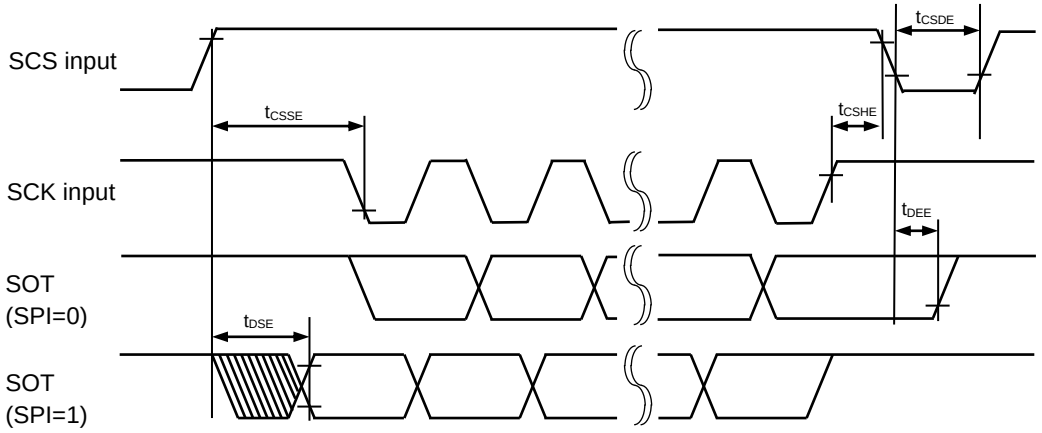
Please see the hardware manual for details of above-mentioned *1,*2, and *3.

(4-1-7) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,
When Serial chip select is used : SCSCR:CSEN = 1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV = 0,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL = 0
(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3V±0.3V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t_{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU} +300 *1	ns	
SCK↑→SCS↓ hold time	t_{CSHI}	SCK1 to SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	

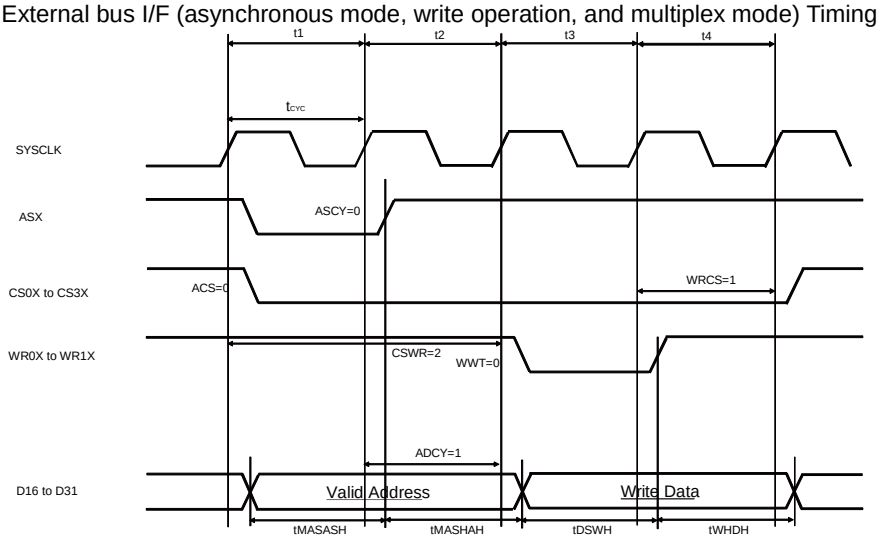


When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode

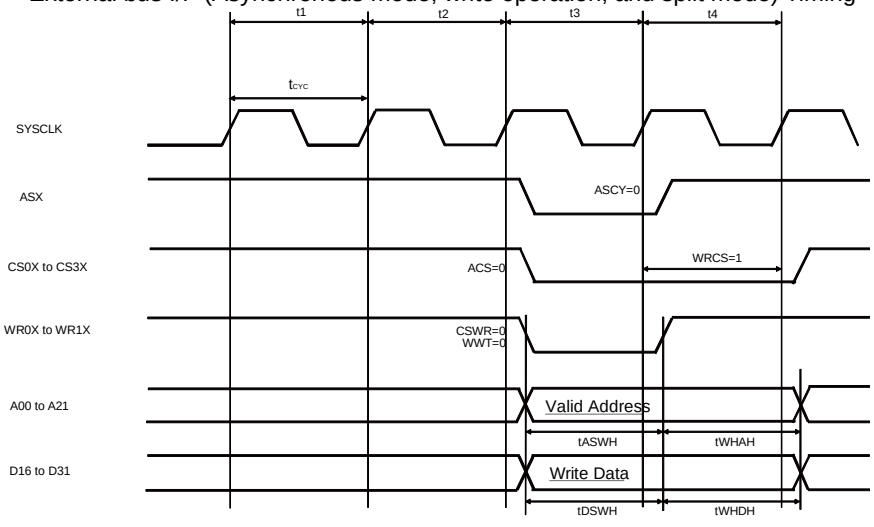


When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode

External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing



External bus I/F (Asynchronous mode, write operation, and split mode) Timing

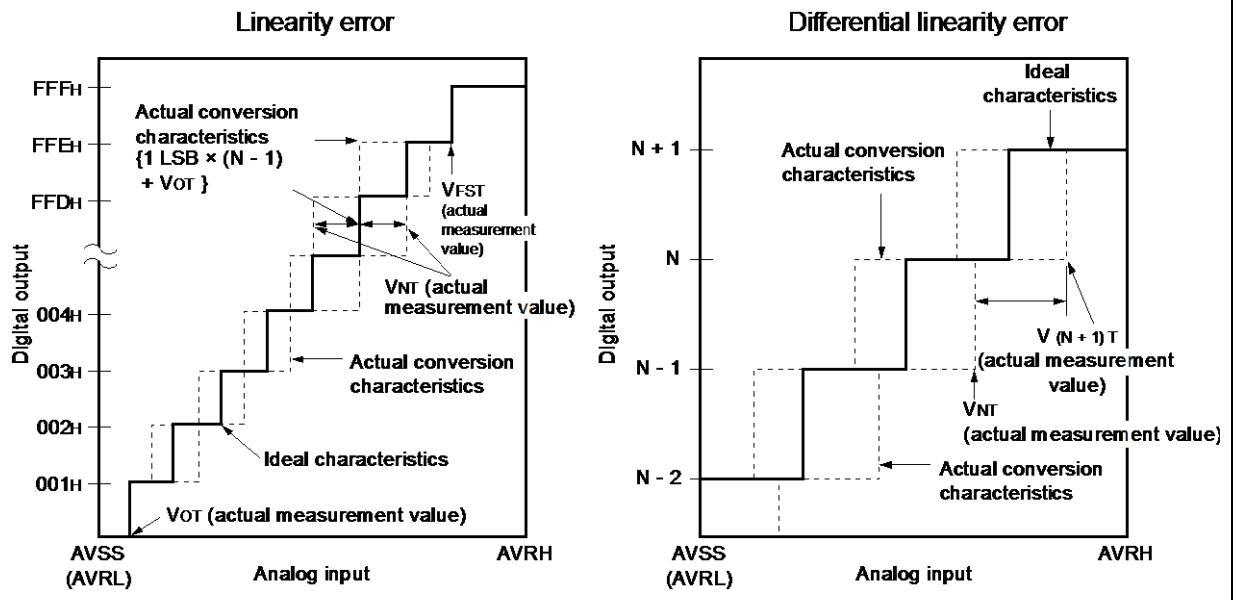


(2) Definition of A/D Converter Terms

Resolution : Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"← →"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"← →"1111 1111 1111").

Differential linearity error : Deviation of the input voltage from the ideal value that is required to change the output code by LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ LSB} \quad \text{[LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \text{ [V]}$$

V_{OT} : Voltage at which the digital output changes from "000_H" to "001_H".
V_{FST} : Voltage at which the digital output changes from "FFE_H" to "FFF_H".

Flash Memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A = +85 °C*3

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7 V or more within the duration calculated by the following expression:

$$Td^{*}[\mu s] + (\text{period of PCLK } [\mu s] \times 257) + 50\ [\mu s]$$

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
MB91F526KWBPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4 mm) Plastic
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	
MB91F526KSBPMC1	None	ON	ON	
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>34</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><td>Function*2</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit21 I/O (0)</td></tr>
<tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 0 (1)</td></tr>
<tr><td>INT7 External interrupt input (1)</td></tr>
<tr><td>(CAN reception data 2 input
MB91F52xB ,MB91F52xD only)</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit22 I/O (0)</td></tr>
<tr><td>Serial chip select 2 I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 1 (1)</td></tr>
<tr><td>INT2 External interrupt input (1)</td></tr>
<tr><td>(CAN transmission data 2 output
MB91F52xB ,MB91F52xD only)</td></tr>
</table>

(Correct)
<table>
<tr><td>Function*9</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit21 I/O (0)</td></tr>
<tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 0 (1)</td></tr>
<tr><td>INT7 External interrupt input (1)</td></tr>
<tr><td>CAN reception data 2 input</td></tr>
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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>129</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 100pin modified as follows:

(Error)
<table>
<tr><td>Base timer 0 IRQ0
Base timer 0 IRQ1</td><td>60</td><td>3C</td><td>ICR44</td><td>30C_H</td><td>000FFF0C_H</td><td>44</td></tr>
</table>

(Correct)
<table>
<tr><td>–
–</td><td>60</td><td>3C</td><td>ICR44</td><td>30C_H</td><td>000FFF0C_H</td><td>44</td></tr>
</table>
</td></tr>
<tr><td>129</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 100pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR45</td><td rowspan="4">308_H</td><td rowspan="4">000FFF08_H</td><td rowspan="4">45 *5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR45</td><td rowspan="4">308_H</td><td rowspan="4">000FFF08_H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>129</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 100pins.

(Error)
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>