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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526kjcpmc1-gse1

Product Lineup Comparison 80 Pins

	MB91F522D	MB91F523D	MB91F524D	MB91F525D	MB91F526D
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)	64 KB				
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)	None				
DMA Transfer	16 ch				
16-bit Base Timer	1 ch				
Free-run Timer	16 bit × 3 ch, 32 bit × 2 ch				
Input capture	16 bit × 4 ch, 32 bit × 5 ch				
Output Compare	16 bit × 6 ch, 32 bit × 4 ch				
16-bit Reload Timer	7 ch				
PPG	16 bit × 27 ch				
Up/down Counter	2 ch				
Clock Supervisor	Yes				
External Interrupt	8 ch × 2 units				
A/D converter	12 bit × 16 ch (1 unit), 12 bit × 16 ch (1 unit)				
D/A converter (8 bit)	1 ch				
Multi-Function Serial Interface	9 ch*1				
CAN	64 msg × 2 ch/128 msg × 1 ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	56 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6 ch				
Operation guaranteed temperature (T_A)	-40 °C to +125 °C				
Power supply	2.7 V to 5.5 V *2				
Package	LQH080				

*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 144 Pins

	MB91F522K	MB91F523K	MB91F524K	MB91F525K	MB91F526K
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)	64 KB				
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)	Yes				
DMA Transfer	16 ch				
16-bit Base Timer	2 ch				
Free-run Timer	16 bit × 3 ch, 32 bit × 3 ch				
Input capture	16 bit × 4 ch, 32 bit × 6 ch				
Output Compare	16 bit × 6 ch, 32 bit × 6 ch				
16-bit Reload Timer	8 ch				
PPG	16 bit × 44 ch				
Up/down Counter	2 ch				
Clock Supervisor	Yes				
External Interrupt	8 ch × 2 units				
A/D converter	12 bit × 32 ch (1 unit), 12 bit × 16 ch (1 unit)				
D/A converter (8 bit)	2 ch				
Multi-Function Serial Interface	12 ch*1				
CAN	64 msg × 2 ch/128 msg × 1 ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	120 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6 ch				
Operation guaranteed temperature (T_A)	-40 °C to +125 °C				
Power supply	2.7 V to 5.5 V *2				
Package	LQS144, LQN144				

*1: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 176 Pins

	MB91F522L	MB91F523L	MB91F524L	MB91F525L	MB91F526L
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)	64 KB				
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)	Yes				
DMA Transfer	16 ch				
16-bit Base Timer	2 ch				
Free-run Timer	16 bit × 3 ch, 32 bit × 3 ch				
Input capture	16 bit × 4 ch, 32 bit × 6 ch				
Output Compare	16 bit × 6 ch, 32 bit × 6 ch				
16-bit Reload Timer	8 ch				
PPG	16 bit × 48 ch				
Up/down Counter	2 ch				
Clock Supervisor	Yes				
External Interrupt	8 ch × 2 units				
A/D converter	12 bit × 32 ch (1 unit), 12 bit × 16 ch (1 unit)				
D/A converter (8 bit)	2 ch				
Multi-Function Serial Interface	12 ch*1				
CAN	64 msg × 2 ch/128 msg × 1 ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	152 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6 ch				
Operation guaranteed temperature (T_A)	-40 °C to +125 °C				
Power supply	2.7 V to 5.5 V *2				
Package	LQP176				

*1: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0018B8H	SCR9/(IBCR9) [R/W] B,H,W 0--00000	SMR9[R/W] B,H,W 000-00-0	SSR9[R/W] B,H,W 0-000011	ESCR9/(IBSR9)[R/W] B,H,W 00000000	Multi-UART9 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I²C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018BCH	— /(RDR19/(TDR19))[R/W] B,H,W -------- -------- *3		RDR09/(TDR09)[R/W] B,H,W -------0 00000000 *1		
0018C0H	SACSR9[R/W] B,H,W 0----000 00000000		STMR9[R] B,H,W 00000000 00000000		
0018C4H	STMCR9[R/W] B,H,W 00000000 00000000		— /(SCSCR9/SFUR9)[R/W] B,H,W -------- -------- *3 *4		
0018C8H	— /(SCSTR39)/ (LAMSR9) [R/W] B,H,W -------- *3	— /(SCSTR29)/ (LAMCR9) [R/W] B,H,W -------- *3	— /(SCSTR19)/ (SFLR19) [R/W] B,H,W -------- *3	— /(SCSTR09)/ (SFLR09) [R/W] B,H,W -------- *3	
0018CCH	—	— /(SCSFR29) [R/W] B,H,W -------- *3	— /(SCSFR19) [R/W] B,H,W -------- *3	— /(SCSFR09) [R/W] B,H,W -------- *3	
0018D0H	—/(TBYTE39)/ (LAMESR9) [R/W] B,H,W -------- *3	—/(TBYTE29)/ (LAMERT9) [R/W] B,H,W -------- *3	—/(TBYTE19)/ (LAMIER9) [R/W] B,H,W -------- *3	TBYTE09/(LAMRID9) / (LAMTID9) [R/W] B,H,W 00000000	
0018D4H	BGR9[R/W] H, W 00000000 00000000		— /(ISMK9)[R/W] B,H,W -------- *2	— /(ISBA9)[R/W] B,H,W -------- *2	
0018D8H	FCR19[R/W] B,H,W ---00100	FCR09[R/W] B,H,W -0000000	FBYTE9[R/W] B,H,W 00000000 00000000		
0018DCH	FTICR9[R/W] B,H,W 00000000 00000000		—	—	
0018E0H	SCR10/(IBCR10) [R/W] B,H,W 0--00000	SMR10[R/W] B,H,W 000-00-0	SSR10[R/W] B,H,W 0-000011	ESCR10/(IBSR10) [R/W] B,H,W 00000000	Multi-UART10 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I²C mode is not set immediately after reset.
0018E4H	— /(RDR110/(TDR110))[R/W] B,H,W -------- -------- *3		RDR010/(TDR010)[R/W] B,H,W -------0 00000000 *1		
0018E8H	SACSR10[R/W] B,H,W 0----000 00000000		STMR10[R] B,H,W 00000000 00000000		
0018ECH	STMCR10[R/W] B,H,W 00000000 00000000		— /(SCSCR10/SFUR10)[R/W] B,H,W -------- -------- *3 *4		

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1,*4
A/D converter 0/1/7/10/11/12/14/15/16/17/19/22/26/27/28/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU7/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
-	60	3C	ICR44	$30C_H$	$000FFF0C_H$	-*6
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-

100 Pins

Interrupt Factor	Interrupt number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*1
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358_H	$000FFF58_H$	25*3
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/36/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

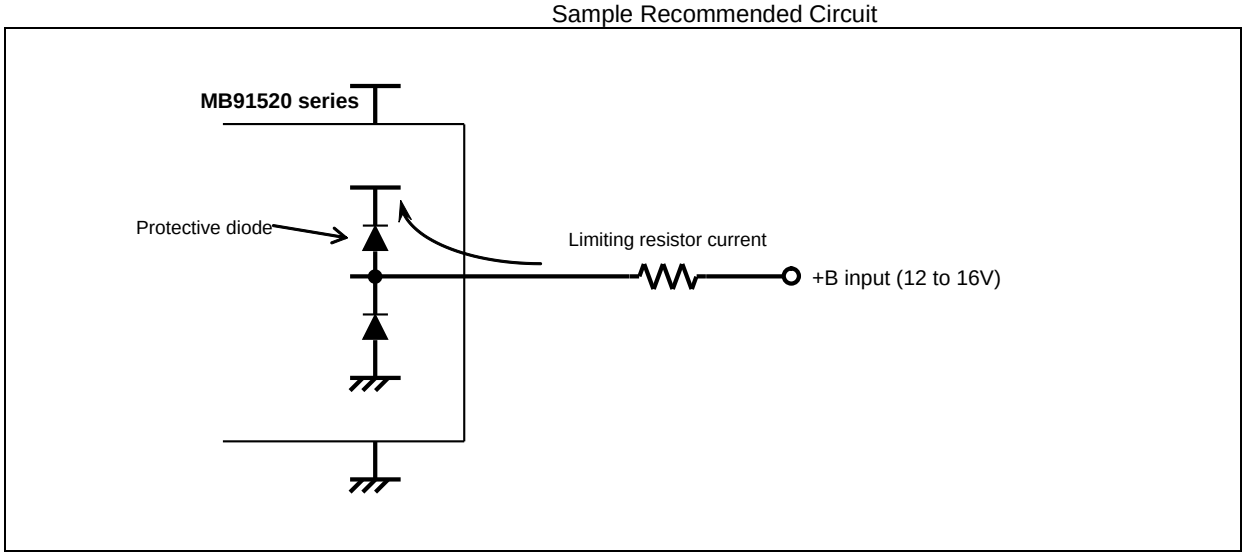
*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: It is a standard when four-layer substrate is used.

*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample Recommended Circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Recommended Operating Conditions

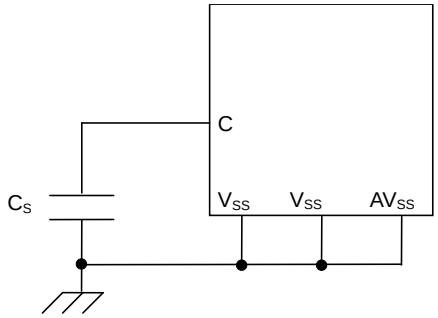
(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0 V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3 V is used)
		2.7	5.5	V	Operation guarantee range*1
Smoothing capacitor *2	C_S	4.7 (tolerance within ±50 %)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative.
The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the

minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
*2: See the following diagram for details on the connection of smoothing capacitor C_S.
*3: When it is used under this condition, contact your sales representative.

· C Pin Connection Diagram



<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	0.7× V_{CC}	-	V_{CC}	V	
	V_{IH3}	Port other than V_{IH1}	Automotive input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IH5}	RSTX,NMIX,MD 0,MD1	CMOS hysteresis input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IHT}	DEBUGIF	TTL input level	2	-	V_{CC}	V	
"L" level input voltage	V_{IL1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	Vss	-	0.3× V_{CC}	V	
	V_{IL3}	Port other than V_{IH1}	Automotive input level	Vss	-	0.5× V_{CC}	V	
	V_{IL5}	RSTX,NMIX,MD 0,MD1	CMOS hysteresis input level	Vss	-	0.2× V_{CC}	V	
	V_{ILT}	DEBUGIF	TTL input level	Vss	-	0.8	V	

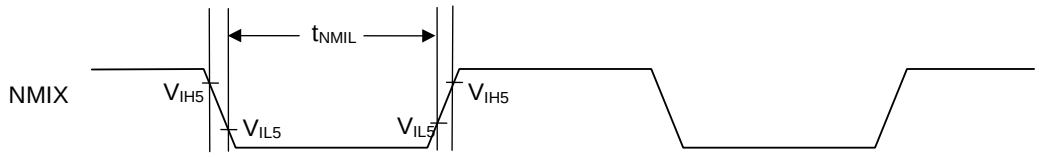
*: It is a standard in BRAMSC (Backup RAM sleep control bit) = 1 (Enter the state of the sleep at the standby mode) condition.

(7) NMI input timing

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

・ NMIX input timing



(8) Low voltage detection (External low-voltage detection)

(T_A: -40 °C to +125 °C, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	2.7	-	5.5	V	
Detection voltage*3	V_{DL}		*1	-8%	LVD5F_SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Hysteresis width	V_{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	Td	-		-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).

*3: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V).
This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7 V).
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT = 0 *2
SYSCLK↑→ data output time	t_{CHDV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.
SYSCLK↑→ address output time	t_{CHMAV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: □ Set CSWR and CSRD to 2 or more. □ ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

*1: Please use it with external load capacity 12 pF or less for VCC = 3.3 V ± 0.3 V (40 MHz operation).

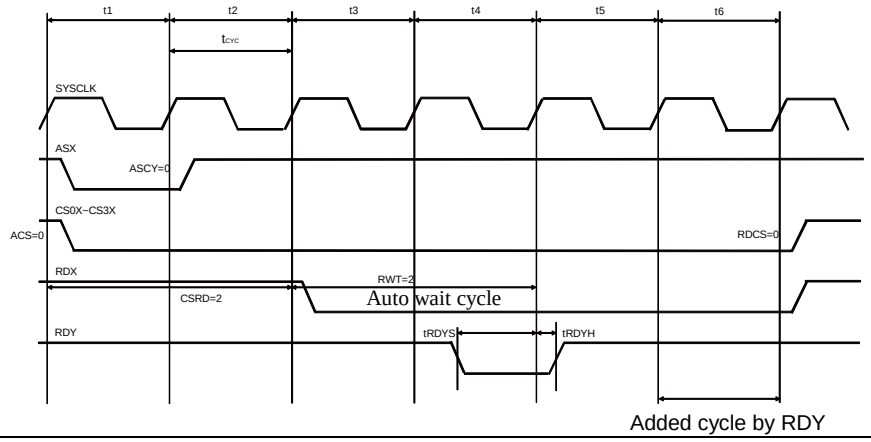
*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

(12) External bus I/F (ready) Timing

(T_A: -40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)
(external load capacitance 50 pF)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t_{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK, RDY	0	-	ns	

External bus I/F (ready) Timing

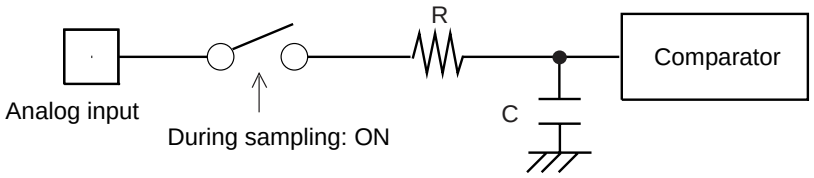


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

- Analog input circuit model



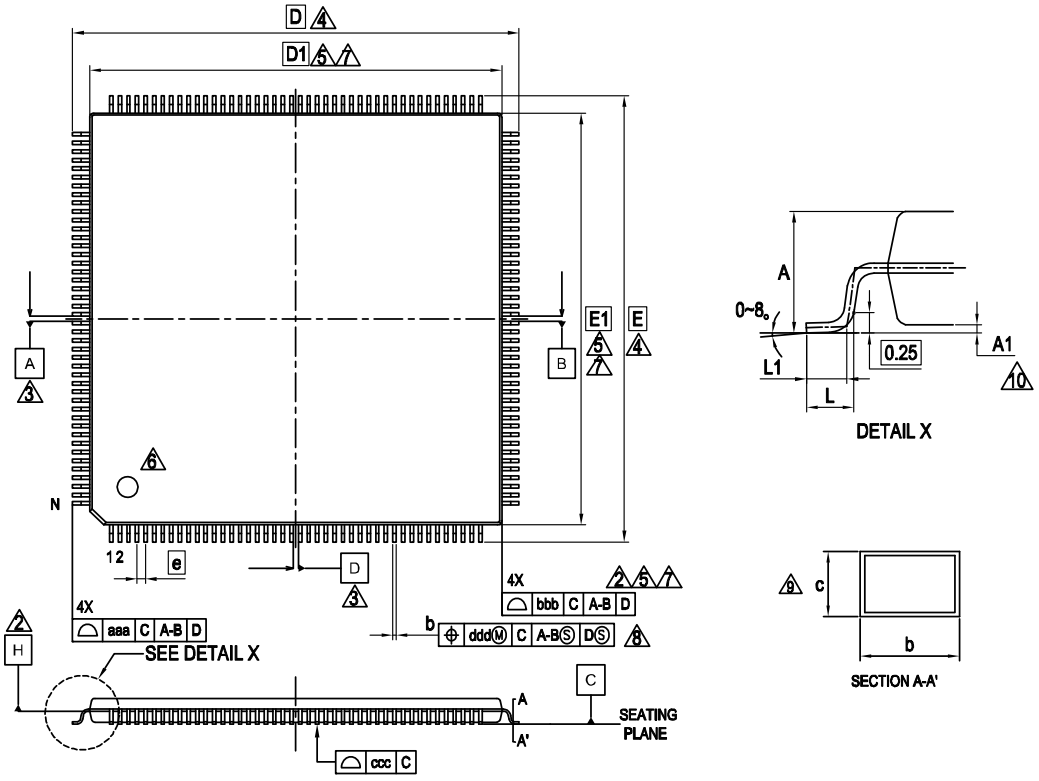
	R	C	
12-bit A/D	1.9 kΩ (Max)	8.30 pF (Max)	(4.5 V ≤ AV_{CC} ≤ 5.5 V)
	4.3 kΩ (Max)	8.30 pF (Max)	(3.0 V ≤ AV_{CC} ≤ 3.6 V)

Note: Listed values must be considered as reference values.

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
MB91F526JWCPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JYCPMC			OFF	
MB91F526JJCPMC		OFF	ON	
MB91F526JLCPMC			OFF	
MB91F525JWCPMC		ON	ON	
MB91F525JYCPMC			OFF	
MB91F525JJCPMC		OFF	ON	
MB91F525JLCPMC			OFF	
MB91F524JWCPMC		ON	ON	
MB91F524JYCPMC			OFF	
MB91F524JJCPMC		OFF	ON	
MB91F524JLCPMC			OFF	
MB91F523JWCPMC		ON	ON	
MB91F523JYCPMC			OFF	
MB91F523JJCPMC		OFF	ON	
MB91F523JLCPMC			OFF	
MB91F522JWCPMC		ON	ON	
MB91F522JYCPMC			OFF	
MB91F522JJCPMC		OFF	ON	
MB91F522JLCPMC			OFF	
MB91F526JSCPMC	None	ON	ON	
MB91F526JUCPMC			OFF	
MB91F526JHCPMC		OFF	ON	
MB91F526JKCPMC			OFF	
MB91F525JSCPMC		ON	ON	
MB91F525JUCPMC			OFF	
MB91F525JHCPMC		OFF	ON	
MB91F525JKCPMC			OFF	
MB91F524JSCPMC		ON	ON	
MB91F524JUCPMC			OFF	
MB91F524JHCPMC		OFF	ON	
MB91F524JKCPMC			OFF	
MB91F523JSCPMC		ON	ON	
MB91F523JUCPMC			OFF	
MB91F523JHCPMC		OFF	ON	
MB91F523JKCPMC			OFF	
MB91F522JSCPMC		ON	ON	
MB91F522JUCPMC			OFF	
MB91F522JHCPMC		OFF	ON	
MB91F522JKCPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
MB91F526KWDPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4 mm) Plastic
MB91F526KJDPMC1		OFF	ON	
MB91F525KWDPMC1		ON	ON	
MB91F525KJDPMC1		OFF	ON	
MB91F524KWDPMC1		ON	ON	
MB91F524KJDPMC1		OFF	ON	
MB91F523KWDPMC1		ON	ON	
MB91F523KJDPMC1		OFF	ON	
MB91F522KWDPMC1		ON	ON	
MB91F522KJDPMC1		OFF	ON	
MB91F526KSDPMC1	None	ON	ON	
MB91F526KHDPMC1		OFF	ON	
MB91F525KSDPMC1		ON	ON	
MB91F525KHDPMC1		OFF	ON	
MB91F524KSDPMC1		ON	ON	
MB91F524KHDPMC1		OFF	ON	
MB91F523KSDPMC1		ON	ON	
MB91F523KHDPMC1		OFF	ON	
MB91F522KSDPMC1		ON	ON	
MB91F522KHDPMC1		OFF	ON	
MB91F526JWDPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JJDPMC		OFF	ON	
MB91F525JWDPMC		ON	ON	
MB91F525JJDPMC		OFF	ON	
MB91F524JWDPMC		ON	ON	
MB91F524JJDPMC		OFF	ON	
MB91F523JWDPMC		ON	ON	
MB91F523JJDPMC		OFF	ON	
MB91F522JWDPMC		ON	ON	
MB91F522JJDPMC		OFF	ON	
MB91F526JSDPMC	None	ON	ON	
MB91F526JHDPMC		OFF	ON	
MB91F525JSDPMC		ON	ON	
MB91F525JHDPMC		OFF	ON	
MB91F524JSDPMC		ON	ON	
MB91F524JHDPMC		OFF	ON	
MB91F523JSDPMC		ON	ON	
MB91F523JHDPMC		OFF	ON	
MB91F522JSDPMC		ON	ON	
MB91F522JHDPMC		OFF	ON	

LQP176 , 176 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQP176		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.50 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	176		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
14	■Pin Assignment MB91F52xD	- Right side 60 VSS 59 P122/SIN6_0/AN31/OCU8_0/INT9_1 58 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0 57 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1 56 P114/SCS61_0/AN26/PPG18_0/RTO2_0 55 P110/TX1(64)/SCS63_0/AN22 54 NMIX 53 P107/AN19/PPG15_0 52 P105/SCS71_0/AN17/PPG13_0 51 P104/SCS72_0/AN16/PPG12_0 50 P103/SCS73_0/AN15/PPG11_0 49 P102/SIN7_0/AN14/PPG10_0/INT10_0 48 P100/SCK7_0/SCL7/AN12/PPG8_0 47 **AVCC0** 46 **AVRH0** 45 **AVSS0/AVRL0** 44 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1 43 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0 42 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT2_1 41 VSS ↓ 60 VSS 59 P122/SIN6_0/AN31/OCU8_0/INT9_1 58 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0 57 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1 56 P114/SCS61_0/AN26/PPG18_0/RTO2_0 55 P110/TX1(64)/SCS63_0/AN22 54 NMIX 53 P107/AN19/PPG15_0 52 P105/AN17/PPG13_0 51 P104/AN16/PPG12_0 50 P103/AN15/PPG11_0 49 P102/AN14/PPG10_0/INT10_0 48 P100/AN12/PPG8_0 47 **AVCC0** 46 **AVRH0** 45 **AVSS0/AVRL0** 44 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1 43 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0 42 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0 41 VSS

<table>
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<table>
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<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">2</td><td rowspan="3">2</td><td>P015</td></tr>
<tr><td>D29</td></tr>
<tr><td>TRG0_0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">3</td><td rowspan="3">3</td><td>P016</td></tr>
<tr><td>D30</td></tr>
<tr><td>TRG1_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">4</td><td>P170</td></tr>
<tr><td>PPG36_1</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">4</td><td rowspan="3">5</td><td>P017</td></tr>
<tr><td>D31</td></tr>
<tr><td>TRG2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">6</td><td>P171</td></tr>
<tr><td>PPG37_1</td></tr>
<tr><td rowspan="6">2</td><td rowspan="6">2</td><td rowspan="6">2</td><td rowspan="6">2</td><td rowspan="6">5</td><td rowspan="6">7</td><td>P020</td></tr>
<tr><td>ASX</td></tr>
<tr><td>SIN3_1</td></tr>
<tr><td>TRG3_0</td></tr>
<tr><td>TIN0_2</td></tr>
<tr><td>RTO5_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">3</td><td rowspan="5">6</td><td rowspan="5">8</td><td>P021</td></tr>
<tr><td>CS0X</td></tr>
<tr><td>SOT3_1</td></tr>
<tr><td>TRG6_1</td></tr>
<tr><td>TRG4_0</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">7</td><td rowspan="5">9</td><td>P022</td></tr>
<tr><td>CS1X</td></tr>
<tr><td>SCK3_1</td></tr>
<tr><td>TRG7_1</td></tr>
<tr><td>TRG5_0</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">5</td><td rowspan="5">8</td><td rowspan="5">10</td><td>P023</td></tr>
<tr><td>RDX</td></tr>
<tr><td>SCS3_1</td></tr>
<tr><td>PPG32_0</td></tr>
<tr><td>TIN0_0</td></tr>
<tr><td rowspan="6">3</td><td rowspan="6">3</td><td rowspan="6">3</td><td rowspan="6">6</td><td rowspan="6">9</td><td rowspan="6">11</td><td>P024</td></tr>
<tr><td>WR0X</td></tr>
<tr><td>SIN4_1</td></tr>
<tr><td>PPG24_0</td></tr>
<tr><td>TIN1_0</td></tr>
<tr><td>RTO4_1</td></tr>
<tr><td>INT15_0</td></tr>
</table></td></tr>
</table>