Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11648
Number of Logic Elements/Cells	291200
Total RAM Bits	17661952
Number of I/O	781
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4s100g3f45i2n

Chapter Revision Dates

The chapters in this document, Stratix IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. DC and Switching Characteristics for Stratix IV Devices
Revised: *September 2014*
Part Number: *SIV54001-5.9*

Chapter 2. Addendum to the Stratix IV Device Handbook
Revised: *February 2011*
Part Number: *SIV54002-1.5*

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–4 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–4 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half of a year.

Table 1–4. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	4.0	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%

Temperature Overshoot Above Maximum Allowed Temperature

The maximum allowed operating temperature for Stratix IV industrial grade devices is 100 °C. It is recommended that the operating temperature of the device is maintained below 100 °C at all times. The temperature excursions over 100 °C due to internal heating of the device should not exceed the number of cycles as specified in the Table 1–5. Exceeding the recommended number of cycles may cause solder interconnect failures. Altera® recommends using the Stratix IV military grade devices if the application requires operating temperatures over 100 °C.

Table 1–5. Temperature Overshoot Above Maximum Allowed Temperature

Description	Operating Temperature (°C)	Number of Cycles Over 100 °C
Device operating temperature (°C)	100	3200
	105	768
	110	640
	115	480
	120	320
	125	160

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Stratix IV devices. Table 1–6 lists the steady-state voltage and current values expected from Stratix IV devices. Power supply ramps must all be strictly monotonic, without plateaus.

For power supply ripple requirements, refer to the *Device-Specific Power Delivery Network (PDN) Tool User Guide*.

Table 1–6. Recommended Operating Conditions for Stratix IV Devices (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC} (Stratix IV GX and Stratix IV E)	Core voltage and periphery circuitry power supply	—	0.87	0.90	0.93	V
V_{CC} (Stratix IV GT)	Core voltage and periphery circuitry power supply	—	0.92	0.95	0.98	V
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.5	1.55	V
V_{CCAUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} (2)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_PLL} (Stratix IV GX and Stratix IV E)	PLL digital voltage regulator power supply	—	0.87	0.90	0.93	V
V_{CCD_PLL} (Stratix IV GT)	PLL digital voltage regulator power supply	—	0.92	0.95	0.98	V
V_{CC_CLKIN}	Differential clock input power supply	—	2.375	2.5	2.625	V
V_{CCBAT} (1)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.3	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J (Stratix IV GX and Stratix IV E)	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
		Military	–55	—	125	°C
T_J (Stratix IV GT)	Operating junction temperature	Industrial	0	—	100	°C

Table 1–8. Transceiver Power Supply Operating Conditions for Stratix IV GT Devices (Part 2 of 2) (1), (2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCR_R}	Receiver power (right side)	1.15	1.2	1.25	V
V_{CCT_L}	Transmitter power (left side)	1.15	1.2	1.25	V
V_{CCT_R}	Transmitter power (right side)	1.15	1.2	1.25	V
V_{CCL_GXBLn} (3)	Transceiver clock power (left side)	1.15	1.2	1.25	V
V_{CCL_GXBRn} (3)	Transceiver clock power (right side)	1.15	1.2	1.25	V
V_{CCH_GXBLn} (3)	Transmitter output buffer power (left side)	1.33	1.4	1.47	V
V_{CCH_GXBRn} (3)	Transmitter output buffer power (right side)	1.33	1.4	1.47	V

Notes to Table 1–8:

(1) For the recommended operating conditions for Stratix IV GT engineering sample (ES1) devices, contact your local Altera sales representative.

(2) Transceiver power supplies do not have power-on-reset circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

(3) n = 0, 1, 2, or 3.

DC Characteristics

This section lists the supply current, I/O pin leakage current, bus hold, on-chip termination (OCT) tolerance, input pin capacitance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 1–9 lists the Stratix IV I/O pin leakage current specifications.

Table 1–9. I/O Pin Leakage Current for Stratix IV Devices (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0V to $V_{CCIOMAX}$	-20	—	20	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0V to $V_{CCIOMAX}$	-20	—	20	µA

Note to Table 1–9:

(1) V_{REF} current refers to the input pin leakage current.

Bus Hold Specifications

Table 1–10 lists the Stratix IV device family bus hold specifications.

Table 1–10. Bus Hold Parameters

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	—	-160	—	-200	—	-300	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 1–11 lists the Stratix IV OCT termination calibration accuracy specifications.

Table 1–11. OCT Calibration Accuracy Specifications for Stratix IV Devices (Part 1 of 2) *(1)*

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3, M3	C4,I4	
25-Ω R_S *(2)* 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R_T 2.5, 1.8, 1.5, 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%
20-Ω , 40-Ω , and 60-Ω R_S *(3)* 3.0, 2.5, 1.8, 1.5, 1.2	Expanded range for internal series termination with calibration (20-Ω , 40-Ω , and 60-Ω R_S setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 1–13 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–13 to determine the OCT variation after power-up calibration and Equation 1–1 to determine the OCT variation without re-calibration.

Equation 1–1. OCT Variation Without Re-Calibration (1), (2), (3), (4), (5), (6)

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 1–1:

(1) The R_{OCT} value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1–13 lists the OCT variation after the power-up calibration.

Table 1–13. OCT Variation after Power-Up Calibration (1)

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 1–13:

(1) Valid for V_{CCIO} range of ±5% and temperature range of 0° to 85°C.

Pin Capacitance

Table 1–14 lists the Stratix IV device family pin capacitance.

Table 1–14. Pin Capacitance for Stratix IV Devices (Part 1 of 2)

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	4	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	4	pF
C_{CLKTB}	Input capacitance on the top and bottom non-dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on the left and right non-dedicated clock input pins	4	pF

Table 1–14. Pin Capacitance for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Value	Unit
C_{OUTFB}	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Hot Socketing

Table 1–15 lists the hot socketing specifications for Stratix IV devices.

Table 1–15. Hot Socketing Specifications for Stratix IV Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 1–16 lists the weak pull-up resistor values for Stratix IV devices.

Table 1–16. Internal Weak Pull-Up Resistor for Stratix IV Devices (1), (3)

Symbol	Description	Conditions (V)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.0 ±5% (2)	25	kΩ
		V_{CCIO} = 2.5 ±5% (2)	25	kΩ
		V_{CCIO} = 1.8 ±5% (2)	25	kΩ
		V_{CCIO} = 1.5 ±5% (2)	25	kΩ
		V_{CCIO} = 1.2 ±5% (2)	25	kΩ

Notes to Table 1–16:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

(4) These specifications are valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 1–17 through Table 1–22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix IV devices. These tables also show the Stratix IV device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of terms used in Table 1–17 through Table 1–22, refer to "Glossary" on page 1–64.

Table 1–17. Single-Ended I/O Standards

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V_{CCIO} - 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} - 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	3.6	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 * V_{CCIO}	0.5 * V_{CCIO}	—	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5

Table 1–18. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	0.47 * V_{CCIO}	V_{REF}	0.53 * V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	$V_{CCIO}/2$	—

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 2 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3)	10 KHz to 20 MHz	—	—	3	—	—	3	—	—	3	ps
R_{REF}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
`reconfig_clk` clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (5)	—	50	2.5/ 37.5 (5)	—	50	2.5/ 37.5 (5)	—	50	—
Delta time between `reconfig_clks` (19)	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down (`gxb_powerdown`) pulse width	—	1	—	—	1	—	—	1	—	—	µs
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (Single width, non-PMA Direct) (23)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct) (23)	—	1000	—	8500	1000	—	6500	1000	—	6375 (22)	Mbps
Data rate (Single width, PMA Direct) (23)	—	600	—	3250	600	—	3250	600	—	3250	Mbps

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 4 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, Serial RapidIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant									—
Programmable PPM detector (8)	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000									ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (18)	—	—	—	16	—	—	16	—	—	16	dB
t_{LTR} (9)	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR\_LTD\_Manual}$ (10)	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD_Manual} (11)	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} (12)	—	4000	—	—	4000	—	—	4000	—	—	ns
Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode	PCIe Gen1	20 - 35									MHz
	PCIe Gen2	40 - 65									MHz
	(OIF) CEI PHY at 6.375 Gbps	20 - 35									MHz
	XAUI	10 - 18									MHz
	Serial RapidIO 1.25 Gbps	10 - 18									MHz
	Serial RapidIO 2.5 Gbps	10 - 18									MHz
	Serial RapidIO 3.125 Gbps	6 - 10									MHz
	GIGE	6 - 10									MHz
	SONET OC12	3 - 6									MHz
	SONET OC48	14 - 19									MHz
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	18500	—	—	18500	—	—	18500	reconfig_clk cycles

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 6 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential and common mode return loss	PCIe Gen1 and Gen2 (TX V_{OD}=4), XAUI (TX V_{OD}=6), HiGig+ (TX V_{OD}=6), CEI SR/LR (TX V_{OD}=8), Serial RapidIO SR (V_{OD}=6), Serial RapidIO LR (V_{OD}=8), CPRI LV (V_{OD}=6), CPRI HV (V_{OD}=2), OBSAI (V_{OD}=6), SATA (V_{OD}=4),	Compliant									—
Rise time (14)	—	50	—	200	50	—	200	50	—	200	ps
Fall time (14)	—	50	—	200	50	—	200	50	—	200	ps
XAUI rise time	—	60	—	130	60	—	130	60	—	130	ps
XAUI fall time	—	60	—	130	60	—	130	60	—	130	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe ×4, Basic ×4	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8	—	—	500	—	—	500	—	—	500	ps

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 3 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military (3) and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter at 5 Gbps (Gen2)	Compliance pattern	Compliant			Compliant			—			UI
PCIe (Gen 1) Electrical Idle Detect Threshold											
$V_{RX-IDLE-DETDIFFp-p}$ (16)	Compliance pattern	65	—	175	65	—	175	65	—	175	UI
Serial RapidIO Transmit Jitter Generation (8)											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Serial RapidIO Receiver Jitter Tolerance (8)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation (9)											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 4 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military (3) and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance (9)											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation (10)											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance (10)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	—	—	—	UI
	Jitter Frequency = 1.875MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
(OIF) CEI Transmitter Jitter Generation (11)											
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance (11)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.675			> 0.675			—	—	>0.675	UI

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 8 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military (3) and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Transmit Jitter Generation (19)											
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
OBSAI Receiver Jitter Tolerance (19)											
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal Jitter tolerance at 768 Mbps	Jitter Frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
Sinusoidal Jitter tolerance at 1536 Mbps	Jitter Frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI

DSP Block Specifications

Table 1–35 lists the Stratix IV DSP block performance specifications.

Table 1–35. Block Performance Specifications for Stratix IV DSP Devices *(1)*

Mode	Resources Used	Performance					Unit
	Number of Multipliers	–1 Industrial and–2/–2× Commercial/ Industrial Speed Grade	–3 Commercial Speed Grade	–3 Industrial Speed Grade	–4 Commercial Speed Grade	–4 Industrial Speed Grade	
9×9-bit multiplier (A, C, E, G) *(2)*	1	520	460	460	400	400	MHz
9×9-bit multiplier (B, D, F, H) *(2)*	1	520	460	460	400	400	MHz
12×12-bit multiplier (A, E) *(3)*	1	540	500	500	440	440	MHz
12×12-bit multiplier (B, D, F, H) *(3)*	1	540	500	500	440	430	MHz
18×18-bit multiplier	1	600	550	550	480	480	MHz
36×36-bit multiplier	1	480	440	440	380	380	MHz
18×18-bit multiply accumulator	4	490	440	440	380	380	MHz
18×18-bit multiply adder	4	510	470	470	410	400	MHz
18×18-bit multiply adder-signed full precision	2	490	450	440	390	390	MHz
18×18-bit multiply adder with loopback *(4)*	2	390	350	350	310	300	MHz
36-bit shift (32-bit data)	1	490	440	440	380	380	MHz
Double mode	1	480	440	440	380	370	MHz

Notes to Table 1–35:

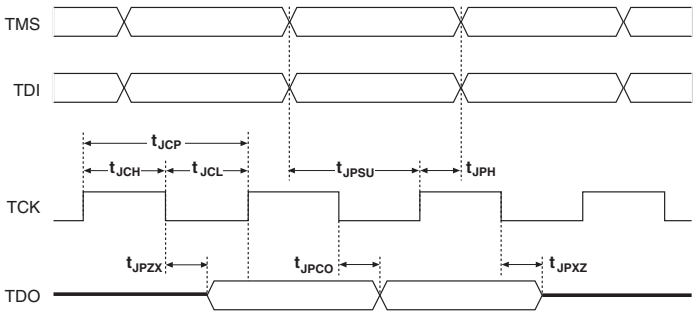
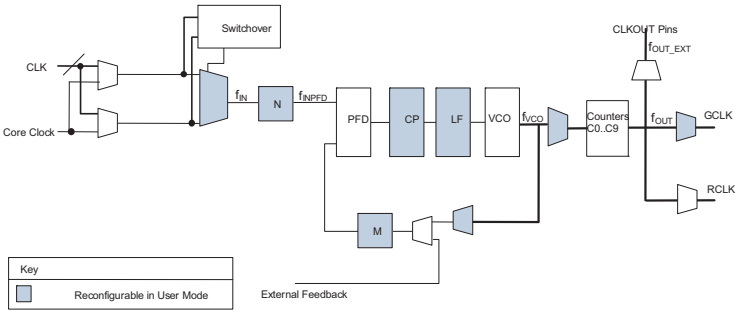
(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.

(2) The DSP block implements eight independent 9b´9b multiplies using A, B, C, D for the top DSP half block and E, F, G, H for the bottom DSP half block multipliers.

(3) The DSP block implements six independent 12b´12b multiplies using A, B, D for the top DSP half block and E, F, H for the bottom DSP half block multipliers.

(4) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

Table 1–54. Glossary Table (Part 2 of 4)

Letter	Subject	Definitions
J	J	High-speed I/O block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications: 
K, L, M, N, O	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Stratix IV device).