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Details	
Product Status	Obsolete
Number of LABs/CLBs	14144
Number of Logic Elements/Cells	353600
Total RAM Bits	23105536
Number of I/O	781
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4s100g4f45i2n

Contents

Table 1–6. Recommended Operating Conditions for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
t_{RAMP}	Power supply ramp time	Normal POR (PORSEL=0)	0.05	—	100	ms
		Fast POR (PORSEL=1)	0.05	—	4	ms

Notes to Table 1–6:

(1) If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.

(2) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

Table 1–7 lists the transceiver power supply recommended operating conditions for Stratix IV GX devices.

Table 1–7. Transceiver Power Supply Operating Conditions for Stratix IV GX Devices (1)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	2.85/2.375	3.0/2.5 (2)	3.15/2.625	V
V_{CCA_R}	Transceiver high voltage power (right side)				
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.87	0.9	0.93	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	0.87	0.9	0.93	V
V_{CCR_L}	Receiver power (left side)	1.045	1.1	1.155	V
V_{CCR_R}	Receiver power (right side)	1.045	1.1	1.155	V
V_{CCT_L}	Transmitter power (left side)	1.045	1.1	1.155	V
V_{CCT_R}	Transmitter power (right side)	1.045	1.1	1.155	V
V_{CCL_GXBLn} (3)	Transceiver clock power (left side)	1.05	1.1	1.15	V
V_{CCL_GXBRn} (3)	Transceiver clock power (right side)	1.05	1.1	1.15	V
V_{CCH_GXBLn} (3)	Transmitter output buffer power (left side)	1.33/1.425	1.4/1.5 (4)	1.47/1.575	V
V_{CCH_GXBRn} (3)	Transmitter output buffer power (right side)				

Notes to Table 1–7:

(1) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

(2) $V_{CCA\_L/R}$ must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(3) n = 0, 1, 2, or 3.

(4) $V_{CCH\_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

Table 1–8 lists the recommended operating conditions for the Stratix IV GT transceiver power supply.

Table 1–8. Transceiver Power Supply Operating Conditions for Stratix IV GT Devices (Part 1 of 2) (1), (2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	3.17	3.3	3.43	V
V_{CCA_R}	Transceiver high voltage power (right side)	3.17	3.3	3.43	V
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.92	0.95	0.98	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	0.92	0.95	0.98	V
V_{CCR_L}	Receiver power (left side)	1.15	1.2	1.25	V

Bus Hold Specifications

Table 1–10 lists the Stratix IV device family bus hold specifications.

Table 1–10. Bus Hold Parameters

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	—	-160	—	-200	—	-300	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 1–11 lists the Stratix IV OCT termination calibration accuracy specifications.

Table 1–11. OCT Calibration Accuracy Specifications for Stratix IV Devices (Part 1 of 2) *(1)*

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3, M3	C4,I4	
25-Ω R_S *(2)* 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R_T 2.5, 1.8, 1.5, 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%
20-Ω , 40-Ω , and 60-Ω R_S *(3)* 3.0, 2.5, 1.8, 1.5, 1.2	Expanded range for internal series termination with calibration (20-Ω , 40-Ω , and 60-Ω R_S setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%

Table 1–19. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.57	V_{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.76	V_{TT} + 0.76	16.2	-16.2
SSTL-18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	V_{TT} - 0.475	V_{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	-13.4
SSTL-15 Class I	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	-8
SSTL-15 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	-16
HSTL-18 Class I	—	V_{REF} -0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-18 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-15 Class I	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-15 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	-8
HSTL-12 Class II	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	-16

Table 1–20. Differential SSTL I/O Standards

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.15	—	$V_{CCIO}/2$ + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.125	—	$V_{CCIO}/2$ + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	$V_{CCIO}/2$	—	0.35	—	—	$V_{CCIO}/2$	—

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 1–23 lists the Stratix IV GX transceiver specifications.

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 1 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.4 V PCML 1.5 V PCML, 2.5 V PCML, Differential LVPECL (4), LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	697	50	—	697	50	—	637.5	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	425	50	—	325	50	—	325	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a REFCLK pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Rise/fall time (21)	—	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	1100 ± 10%			1100 ± 10%			1100 ± 10%			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 2 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3)	10 KHz to 20 MHz	—	—	3	—	—	3	—	—	3	ps
R_{REF}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
`reconfig_clk` clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (5)	—	50	2.5/ 37.5 (5)	—	50	2.5/ 37.5 (5)	—	50	—
Delta time between `reconfig_clks` (19)	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down (`gxb_powerdown`) pulse width	—	1	—	—	1	—	—	1	—	—	µs
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (Single width, non-PMA Direct) (23)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct) (23)	—	1000	—	8500	1000	—	6500	1000	—	6375 (22)	Mbps
Data rate (Single width, PMA Direct) (23)	—	600	—	3250	600	—	3250	600	—	3250	Mbps

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 6 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential and common mode return loss	PCIe Gen1 and Gen2 (TX V_{OD}=4), XAUI (TX V_{OD}=6), HiGig+ (TX V_{OD}=6), CEI SR/LR (TX V_{OD}=8), Serial RapidIO SR (V_{OD}=6), Serial RapidIO LR (V_{OD}=8), CPRI LV (V_{OD}=6), CPRI HV (V_{OD}=2), OBSAI (V_{OD}=6), SATA (V_{OD}=4),	Compliant									—
Rise time (14)	—	50	—	200	50	—	200	50	—	200	ps
Fall time (14)	—	50	—	200	50	—	200	50	—	200	ps
XAUI rise time	—	60	—	130	60	—	130	60	—	130	ps
XAUI fall time	—	60	—	130	60	—	130	60	—	130	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe ×4, Basic ×4	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8	—	—	500	—	—	500	—	—	500	ps

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 7 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block skew in Basic (PMA Direct) ×N mode (15)	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	—	—	400	—	—	400	ps
	N ≥ 18 channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks	—	—	650	—	—	650	—	—	650	ps
CMU0 PLL and CMU1 PLL											
Supported Data Range	—	600	—	8500	600	—	6500	600	—	6375	Mbps
`pll_powerdown` minimum pulse width (`tpll_powerdown`)	—	1									µs
CMU PLL lock time from `pll_powerdown` de-assertion	—	—	—	100	—	—	100	—	—	100	µs

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 9 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is two parallel clock cycles									—

Notes to Table 1–23:

(1) The –2× speed grade is the fastest speed grade offered in the following Stratix IV GX devices: EP4SGX70DF29, EP4SGX110DF29, EP4SGX110FF35, EP4SGX230DF29, EP4SGX110FF35, EP4SGX180DF29, EP4SGX230FF35, EP4SGX290FF35, EP4SGX180FF35, EP4SGX290FH29, EP4SGX360FF35, and EPSGX360FH29.

(2) Stratix IV GX devices in military speed grade only support selected transceiver configuration up to 3125 Mbps. For more information, contact Altera sales representative.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(5) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS.

(8) The rate matcher supports only up to ± 300 parts per million (ppm).

(9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–2 on page 1–33.

(10) Time for which the CDR must be kept in lock-to-reference (LTR) mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–2 on page 1–33.

(11) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–2 on page 1–33.

(12) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–3 on page 1–33.

(13) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the "Left/Right PLL Requirements in Basic (PMA Direct) Mode" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

(14) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(15) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of the device by configuring them in Basic (PMA Direct) xN mode. For more information about clocking requirements in this mode, refer to the "Basic (PMA Direct) Mode Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

(16) The Quartus II software automatically selects the appropriate /L divider depending on the configured data.

(17) The maximum transceiver-FPGA fabric interface speed of 265.625 MHz is allowed only in Basic low-latency PCS mode with a 32-bit interface width. For more information, refer to the "Basic Double-Width Mode Configurations" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

(18) Figure 1–1 shows the AC gain curves for each of the 16 available equalization settings.

(19) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(20) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with **Receiver Equalization** enabled.

(21) The rise and fall time transition is specified from 20% to 80%.

(22) Stratix IV GX devices in -4 speed grade support Basic mode and deterministic latency mode transceiver configurations up to 6375 Mbps. These configurations are shown in the figures 1-90, 1-92, 1-94, 1-96, and 1-101 in the *Transceiver Architecture in Stratix IV Devices* chapter.

(23) To support data rates lower than 600-Mbps specification through oversampling, use the CDR in LTR mode only.

Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part 2 of 8)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Rise/fall time	—	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1200	200	—	1200	200	—	1200	mV
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM}	—	1200 ± 10%			1200 ± 10%			1200 ± 10%			mV
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (2)	10 KHz to 20 MHz	—	—	3	—	—	3	—	—	3	ps
R_{REF}	—	—	—	2000 ± 1%	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
`reconfig_clk` clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (1)	—	—	2.5/ 37.5 (1)	—	50	2.5/ 37.5 (1)	—	50	MHz
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Delta time between `reconfig_clks` (15)	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum (`gxb_powerdown`) power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (Single width, non-PMA Direct) (16)	—	600	—	3750	600	—	3750	600	—	3750	Mbps

Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part 7 of 8)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block skew in Basic (PMA Direct) ×N mode (14)	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	—	—	400	—	—	400	ps
	N ≥ 18 channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks	—	—	650	—	—	650	—	—	650	ps
CMU PLL0 and CMU PLL1											
Supported data range	—	600	—	11300	600	—	10312.5	600	—	8500	Mbps
CMU PLL lock time from `pll_powerdown` de-assertion	—	—	—	100	—	—	100	—	—	100	µs
ATX PLL (6G)											
Supported Data Range	/L = 1	4800-5400 and 6000-6500			4800-5400 and 6000-6500			4800-5400 and 6000-6500			Mbps
	/L = 2	2400-2700 and 3000-3250			2400-2700 and 3000-3250			2400-2700 and 3000-3250			Mbps
	/L = 4	1200-1350 and 1500-1625			1200-1350 and 1500-1625			1200-1350 and 1500-1625			Mbps
ATX PLL (10G)											
Supported Data Range	—	9900	—	11300	9900	—	10312.5	—			Mbps
Transceiver-FPGA Fabric Interface											
Interface speed (non-PMA Direct)	—	25	—	325	25	—	325	25	—	265.625	MHz
Interface speed (PMA Direct)	—	50	—	325	50	—	325	50	—	325	MHz

Table 1–25 through Table 1–28 lists the typical differential V_{OD} termination settings for Stratix IV GX and GT devices.

Table 1–25. Typical V_{OD} Setting, TX Term = 85 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	170 ± 20%	340 ± 20%	510 ± 20%	595 ± 20%	680 ± 20%	765 ± 20%	850 ± 20%	1020 ± 20%

Table 1–26. Typical V_{OD} Setting, TX Term = 100 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	200 ± 20%	400 ± 20%	600 ± 20%	700 ± 20%	800 ± 20%	900 ± 20%	1000 ± 20%	1200 ± 20%

Table 1–27. Typical V_{OD} Setting, TX Term = 120 Ω

Symbol	V_{OD} Setting (mV)						
	0	1	2	3	4	5	6
V_{OD} differential peak-to-peak Typical (mV)	240 ± 20%	480 ± 20%	720 ± 20%	840 ± 20%	960 ± 20%	1080 ± 20%	1200 ± 20%

Table 1–28. Typical V_{OD} Setting, TX Term = 150 Ω

Symbol	V_{OD} Setting (mV)					
	0	1	2	3	4	5
V_{OD} differential peak-to-peak Typical (mV)	300 ± 20%	600 ± 20%	900 ± 20%	1050 ± 20%	1200 ± 20%	1350 ± 20%

Table 1–29 lists typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–29 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Stratix IV HSSI HSPICE models.

Table 1–29. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 1 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0

Table 1–29. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 6 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military (3) and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Receiver Jitter Tolerance (12)											
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 2			> 2			> 2			UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3			> 0.3			> 0.3			UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3			> 0.3			> 0.3			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 1			> 1			> 1			UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 0.2			> 0.2			> 0.2			UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 0.2			> 0.2			> 0.2			UI
SAS Transmit Jitter Generation (17)											
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.25	—	—	0.25	—	—	0.25	UI

PLL Specifications

Table 1–34 lists the Stratix IV PLL specifications when operating in the commercial (0° to 85°C), industrial (–40° to 100°C), and military (–55°C to 125°C) junction temperature ranges.

Table 1–34. PLL Specifications for Stratix IV Devices (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–2/–2x speed grade)	5	—	800 (1)	MHz
	Input clock frequency (–3 speed grade)	5	—	717 (1)	MHz
	Input clock frequency (–4 speed grade)	5	—	717 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO} (2)	PLL VCO operating range (–2 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–3 speed grade)	600	—	1300	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–2/–2x speed grade)	—	—	800 (3)	MHz
	Output frequency for internal global or regional clock (–3 speed grade)	—	—	717 (3)	MHz
	Output frequency for internal global or regional clock (–4 speed grade)	—	—	717 (3)	MHz
f_{OUT_EXT}	Output frequency for external clock output (–2 speed grade)	—	—	800 (3)	MHz
	Output frequency for external clock output (–3 speed grade)	—	—	717 (3)	MHz
	Output frequency for external clock output (–4 speed grade)	—	—	717 (3)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain	—	3.5	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (8)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} (6)	Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)

Table 1–42. High-Speed I/O Specifications (1), (2) (Part 2 of 3)

Symbol	Conditions	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (10), (11)	(5)	—	1600	(5)	—	1250	(5)	—	1250	Mbps
	SERDES factor J = 2, Uses DDR Registers	(5)	—	(6)	(5)	—	(6)	(5)	—	(6)	Mbps
	SERDES factor J = 1, Uses an SDR Register	(5)	—	(6)	(5)	—	(6)	(5)	—	(6)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (7)	SERDES factor J = 4 to 10	(5)	—	1250	(5)	—	1152	(5)	—	800	Mbps
Emulated Differential I/O Standards with One External Output Resistor - f_{HSDR} (data rate)		(5)	—	311	(5)	—	200	(5)	—	200	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.25	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.125	—	—	0.15	—	—	0.15	UI
t_{DUTY}	Tx output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor	—	—	460	—	—	500	—	—	500	ps

Table 1–43 lists the DPA lock time specifications for Stratix IV ES devices.

Table 1–43. DPA Lock Time Specifications—Stratix IV ES Devices Only (1), (2), (3)

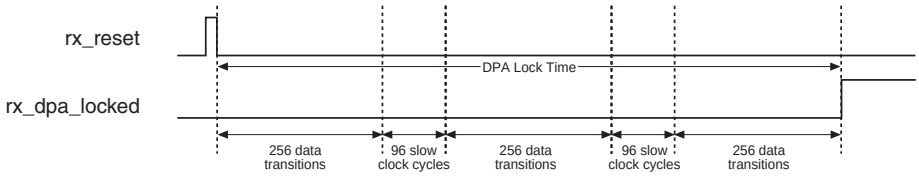
Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetitions per 256 data transitions (4)	Condition	Maximum
SPI-4	00000000001111111111	2	128	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
Parallel Rapid I/O	00001111	2	128	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
	10010000	4	64	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
Miscellaneous	10101010	8	32	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
	01010101	8	32	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)

Notes to Table 1–43:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time applies to commercial, industrial, and military speed grades.
(4) This is the number of repetition for the stated training pattern to achieve 256 data transitions.
(5) Slow clock = Data rate (Mbps)/Deserialization factor.

Figure 1–4 shows the DPA lock time specifications with DPA PLL calibration enabled.

Figure 1–4. DPA Lock Time Specification with DPA PLL Calibration Enabled



Programmable IOE Delay

Table 1–52 lists the Stratix IV IOE programmable delay settings.

Table 1–52. IOE Programmable Delay for Stratix IV Devices

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model					
			Industrial/ Military	Commercial (3)	C2 (3)	C3	C4	I3/M3	I4	Unit
D1	16	0	0.462	0.505	0.732	0.795	0.857	0.801	0.864	ns
D2	8	0	0.234	0.232	0.337	0.372	0.407	0.371	0.405	ns
D3	8	0	1.700	1.769	2.695	2.927	3.157	2.948	3.178	ns
D4	16	0	0.508	0.554	0.813	0.882	0.952	0.889	0.959	ns
D5	16	0	0.472	0.500	0.747	0.799	0.875	0.817	0.882	ns
D6	7	0	0.186	0.195	0.294	0.319	0.345	0.321	0.347	ns

Notes to Table 1–52:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
(2) Minimum offset does not include the intrinsic delay.
(3) For the EP4SGX530 device density, the IOE programmable delays have an additional 5% maximum offset.

Programmable Output Buffer Delay

Table 1–53 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 1–53. Programmable Output Buffer Delay (1)

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Note to Table 1–53:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Table 1–55. Document Revision History (Part 2 of 3)

Date	Version	Changes
December 2011	5.2	■ Added Figure 1–7. ■ Updated Table 1–22 and Table 1–41.
June 2011	5.1	■ Added military speed grade information. ■ Updated Table 1–1 and Table 1–30. ■ Updated (Note 3) in Table 1–42 and (Note 3) in Table 1–43. ■ Added military speed grade to Table 1–5, Table 1–10, Table 1–11, Table 1–23, Table 1–30, Table 1–36, and Table 1–51.
April 2011	5.0	■ Updated Table 1–1, Table 1–5, Table 1–6, Table 1–13, Table 1–16, Table 1–23, and Table 1–24.
March 2011	4.9	■ Updated Table 1–24.
March 2011	4.8	■ Removed (Note 17) in Table 1-24.
February 2011	4.7	■ Added (Note 17) to Table 1–24.
February 2011	4.6	■ Updated Table 1–1, Table 1–5, Table 1–23, Table 1–24, Table 1–30, Table 1–31, Table 1–32, Table 1–34, Table 1–37, Table 1–41, and Table 1–51. ■ Updated the “Recommended Operating Conditions” section. ■ Added the “Schmitt Trigger Input” section.September ■ Minor text edits.
November 2010	4.5	■ Updated Table 1–29. ■ Updated chapter title. ■ Minor text edits.
September 2010	4.4	■ Applied new template. ■ Updated Table 1–1 and Table 1–5.
July 2010	4.3	■ Updated Table 1–7, Table 1–22, Table 1–23, Table 1–33, Table 1–35, Table 1–36, and Table 1–40. ■ Added Table 1–39. ■ Changed “PCI Express” to “PCIe” throughout. ■ Minor text edits
March 2010	4.2	■ Updated Table 1–22, Table 1–23, Table 1–30, Table 1–46, and Table 1–49. ■ Added Table 1–31. ■ Minor text edits.
February 2010	4.1	■ Updated Table 1–11, Table 1–22, Table 1–23, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–29, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–39, Table 1–40, Table 1–43, Table 1–46, and Table 1–49. ■ Added Stratix IV GT speed grade note to Table 1–32, Table 1–35, Table 1–39, Table 1–43, Table 1–44, Table 1–45, and Table 1–46. ■ Added Table 1–28 and Table 1–30. ■ Minor text edits.

This chapter provides additional information about the document and Altera.

About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® IV family of devices.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."