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Details	
Product Status	Obsolete
Number of LABs/CLBs	21248
Number of Logic Elements/Cells	531200
Total RAM Bits	28033024
Number of I/O	781
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4s100g5f45i2n

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Table 1–6. Recommended Operating Conditions for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
t_{RAMP}	Power supply ramp time	Normal POR (PORSEL=0)	0.05	—	100	ms
		Fast POR (PORSEL=1)	0.05	—	4	ms

Notes to Table 1–6:

(1) If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.

(2) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

Table 1–7 lists the transceiver power supply recommended operating conditions for Stratix IV GX devices.

Table 1–7. Transceiver Power Supply Operating Conditions for Stratix IV GX Devices (1)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	2.85/2.375	3.0/2.5 (2)	3.15/2.625	V
V_{CCA_R}	Transceiver high voltage power (right side)				
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.87	0.9	0.93	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	0.87	0.9	0.93	V
V_{CCR_L}	Receiver power (left side)	1.045	1.1	1.155	V
V_{CCR_R}	Receiver power (right side)	1.045	1.1	1.155	V
V_{CCT_L}	Transmitter power (left side)	1.045	1.1	1.155	V
V_{CCT_R}	Transmitter power (right side)	1.045	1.1	1.155	V
V_{CCL_GXBLn} (3)	Transceiver clock power (left side)	1.05	1.1	1.15	V
V_{CCL_GXBRn} (3)	Transceiver clock power (right side)	1.05	1.1	1.15	V
V_{CCH_GXBLn} (3)	Transmitter output buffer power (left side)	1.33/1.425	1.4/1.5 (4)	1.47/1.575	V
V_{CCH_GXBRn} (3)	Transmitter output buffer power (right side)				

Notes to Table 1–7:

(1) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

(2) $V_{CCA\_L/R}$ must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(3) n = 0, 1, 2, or 3.

(4) $V_{CCH\_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

Table 1–8 lists the recommended operating conditions for the Stratix IV GT transceiver power supply.

Table 1–8. Transceiver Power Supply Operating Conditions for Stratix IV GT Devices (Part 1 of 2) (1), (2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	3.17	3.3	3.43	V
V_{CCA_R}	Transceiver high voltage power (right side)	3.17	3.3	3.43	V
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.92	0.95	0.98	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	0.92	0.95	0.98	V
V_{CCR_L}	Receiver power (left side)	1.15	1.2	1.25	V

Table 1–8. Transceiver Power Supply Operating Conditions for Stratix IV GT Devices (Part 2 of 2) (1), (2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCR_R}	Receiver power (right side)	1.15	1.2	1.25	V
V_{CCT_L}	Transmitter power (left side)	1.15	1.2	1.25	V
V_{CCT_R}	Transmitter power (right side)	1.15	1.2	1.25	V
V_{CCL_GXBLn} (3)	Transceiver clock power (left side)	1.15	1.2	1.25	V
V_{CCL_GXBRn} (3)	Transceiver clock power (right side)	1.15	1.2	1.25	V
V_{CCH_GXBLn} (3)	Transmitter output buffer power (left side)	1.33	1.4	1.47	V
V_{CCH_GXBRn} (3)	Transmitter output buffer power (right side)	1.33	1.4	1.47	V

Notes to Table 1–8:

(1) For the recommended operating conditions for Stratix IV GT engineering sample (ES1) devices, contact your local Altera sales representative.

(2) Transceiver power supplies do not have power-on-reset circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

(3) n = 0, 1, 2, or 3.

DC Characteristics

This section lists the supply current, I/O pin leakage current, bus hold, on-chip termination (OCT) tolerance, input pin capacitance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 1–9 lists the Stratix IV I/O pin leakage current specifications.

Table 1–9. I/O Pin Leakage Current for Stratix IV Devices (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0V to $V_{CCIOMAX}$	-20	—	20	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0V to $V_{CCIOMAX}$	-20	—	20	µA

Note to Table 1–9:

(1) V_{REF} current refers to the input pin leakage current.

Table 1–14. Pin Capacitance for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Value	Unit
C_{OUTFB}	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Hot Socketing

Table 1–15 lists the hot socketing specifications for Stratix IV devices.

Table 1–15. Hot Socketing Specifications for Stratix IV Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 1–16 lists the weak pull-up resistor values for Stratix IV devices.

Table 1–16. Internal Weak Pull-Up Resistor for Stratix IV Devices (1), (3)

Symbol	Description	Conditions (V)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.0 ±5% (2)	25	kΩ
		V_{CCIO} = 2.5 ±5% (2)	25	kΩ
		V_{CCIO} = 1.8 ±5% (2)	25	kΩ
		V_{CCIO} = 1.5 ±5% (2)	25	kΩ
		V_{CCIO} = 1.2 ±5% (2)	25	kΩ

Notes to Table 1–16:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

(4) These specifications are valid with ±10% tolerances to cover changes over PVT.

Table 1–19. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.57	V_{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.76	V_{TT} + 0.76	16.2	-16.2
SSTL-18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	V_{TT} - 0.475	V_{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	-13.4
SSTL-15 Class I	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	-8
SSTL-15 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	-16
HSTL-18 Class I	—	V_{REF} -0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-18 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-15 Class I	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-15 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	-8
HSTL-12 Class II	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	-16

Table 1–20. Differential SSTL I/O Standards

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.15	—	$V_{CCIO}/2$ + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.125	—	$V_{CCIO}/2$ + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	$V_{CCIO}/2$	—	0.35	—	—	$V_{CCIO}/2$	—

Table 1–22. Differential I/O Standard Specifications (1), (2) (Part 2 of 2)

I/O Standard	V_{CCIO} (V) (3)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (4)			V_{OCM} (V) (4)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
BLVDS (8)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–22:

(1) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.

(2) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–16.

(3) Differential clock inputs in column I/O are powered by V_{CC_CLKIN} which requires 2.5 V. Differential inputs that are not on clock pins in column I/O are powered by V_{CCPD} which requires 2.5 V. All differential inputs in row I/O banks are powered by V_{CCPD} which requires 2.5V.

(4) RL range: $90 \leq RL \leq 110\ \Omega$.

(5) The receiver voltage input range for the data rate when $D_{MAX} > 700$ Mbps is $1.0\ V \leq V_{IN} \leq 1.6$ V.
The receiver voltage input range for the data rate when $D_{MAX} \leq 700$ Mbps is zero $V \leq V_{IN} \leq 1.85$ V.

(6) The receiver voltage input range for the data rate when $D_{MAX} > 700$ Mbps is $0.85\ V \leq V_{IN} \leq 1.75$ V.
The receiver voltage input range for the data rate when $D_{MAX} \leq 700$ Mbps is $0.45\ V \leq V_{IN} \leq 1.95$ V.

(7) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins.

(8) For more information about BLVDS interface support in Altera devices, refer to *AN522: Implementing Bus LVDS Interfaces in Supported Altera Device Families*.

Power Consumption

Altera offers two ways to estimate power consumption for a design the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Stratix IV core and periphery blocks for commercial, industrial, and military grade devices.

The final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 4 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, Serial RapidIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant									—
Programmable PPM detector (8)	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000									ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (18)	—	—	—	16	—	—	16	—	—	16	dB
t_{LTR} (9)	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR\_LTD\_Manual}$ (10)	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD_Manual} (11)	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} (12)	—	4000	—	—	4000	—	—	4000	—	—	ns
Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode	PCIe Gen1	20 - 35									MHz
	PCIe Gen2	40 - 65									MHz
	(OIF) CEI PHY at 6.375 Gbps	20 - 35									MHz
	XAUI	10 - 18									MHz
	Serial RapidIO 1.25 Gbps	10 - 18									MHz
	Serial RapidIO 2.5 Gbps	10 - 18									MHz
	Serial RapidIO 3.125 Gbps	6 - 10									MHz
	GIGE	6 - 10									MHz
	SONET OC12	3 - 6									MHz
	SONET OC48	14 - 19									MHz
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	18500	—	—	18500	—	—	18500	reconfig_clk cycles

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 9 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is two parallel clock cycles									—

Notes to Table 1–23:

(1) The –2× speed grade is the fastest speed grade offered in the following Stratix IV GX devices: EP4SGX70DF29, EP4SGX110DF29, EP4SGX110FF35, EP4SGX230DF29, EP4SGX110FF35, EP4SGX180DF29, EP4SGX230FF35, EP4SGX290FF35, EP4SGX180FF35, EP4SGX290FH29, EP4SGX360FF35, and EPSGX360FH29.

(2) Stratix IV GX devices in military speed grade only support selected transceiver configuration up to 3125 Mbps. For more information, contact Altera sales representative.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(5) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS.

(8) The rate matcher supports only up to ± 300 parts per million (ppm).

(9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–2 on page 1–33.

(10) Time for which the CDR must be kept in lock-to-reference (LTR) mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–2 on page 1–33.

(11) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–2 on page 1–33.

(12) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–3 on page 1–33.

(13) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the "Left/Right PLL Requirements in Basic (PMA Direct) Mode" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

(14) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(15) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of the device by configuring them in Basic (PMA Direct) xN mode. For more information about clocking requirements in this mode, refer to the "Basic (PMA Direct) Mode Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

(16) The Quartus II software automatically selects the appropriate /L divider depending on the configured data.

(17) The maximum transceiver-FPGA fabric interface speed of 265.625 MHz is allowed only in Basic low-latency PCS mode with a 32-bit interface width. For more information, refer to the "Basic Double-Width Mode Configurations" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

(18) Figure 1–1 shows the AC gain curves for each of the 16 available equalization settings.

(19) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(20) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with **Receiver Equalization** enabled.

(21) The rise and fall time transition is specified from 20% to 80%.

(22) Stratix IV GX devices in -4 speed grade support Basic mode and deterministic latency mode transceiver configurations up to 6375 Mbps. These configurations are shown in the figures 1-90, 1-92, 1-94, 1-96, and 1-101 in the *Transceiver Architecture in Stratix IV Devices* chapter.

(23) To support data rates lower than 600-Mbps specification through oversampling, use the CDR in LTR mode only.

Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part 6 of 8)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential and common mode return loss	PCIe Gen1 and Gen2 (TX V_{OD}=4), XAUI (TX V_{OD}=6), HiGig+ (TX V_{OD}=6), CEI SR/LR (TX V_{OD}=8), Serial RapidIO SR (V_{OD}=6), Serial RapidIO LR (V_{OD}=8), CPRI LV (V_{OD}=6), CPRI HV (V_{OD}=2), OBSAI (V_{OD}=6), SATA (V_{OD}=4),	Compliant									—
Rise time (13)	—	50	—	200	50	—	200	50	—	200	ps
Fall time (13)	—	50	—	200	50	—	200	50	—	200	ps
XAUI rise time	—	60	—	130	60	—	130	60	—	130	ps
XAUI fall time	—	60	—	130	60	—	130	60	—	130	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe, ×4, Basic ×4	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8	—	—	500	—	—	500	—	—	500	ps

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 4 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military (3) and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance (9)											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation (10)											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance (10)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	—	—	—	UI
	Jitter Frequency = 1.875MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
(OIF) CEI Transmitter Jitter Generation (11)											
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance (11)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.675			> 0.675			—	—	>0.675	UI

Table 1–37. Configuration Mode Specifications for Stratix IV Devices

Programming Mode	DCLK F_{MAX}			Unit
	Min	Typ	Max	
Fast active serial	17	26	40	MHz

Note to Table 1–37:

(1) This denotes the maximum frequency supported in the FPP configuration scheme. The frequency supported for each device may vary depending on device density. For more information, refer to the *Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices* chapter.

Table 1–38 lists the JTAG timing parameters and values for Stratix IV devices.

Table 1–38. JTAG Timing Parameters and Values for Stratix IV Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Note to Table 1–38:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Temperature Sensing Diode Specifications

Table 1–39 lists the specifications for the Stratix IV temperature sensing diode.

Table 1–39. External Temperature Sensing Diode Specifications for Stratix IV Devices

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	500	µA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 5	Ω
Diode ideality factor	1.026	1.028	1.030	—

Table 1–40 lists the specifications for the Stratix IV internal temperature sensing diode.

Table 1–40. Internal Temperature Sensing Diode Specifications for Stratix IV Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with No Missing Codes
–40 to 100 °C	±8 °C	No	Frequency: 500 kHz, 1 MHz	< 100 ms	8 bits	8 bits

Chip-Wide Reset (Dev_CLRn) Specifications

Table 1–41 lists the specifications for the Stratix IV chip-wide reset (Dev_CLRn). This specifications denote the minimum pulse width of the Dev_CLRn signal required to clear all the device registers.

Table 1–41. Chip-Wide Reset (DEV_CLRn) Specifications

Description	Min	Typ	Max	Unit
Dev_CLRn	500	—	—	µs

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-LVTTL/LVCMOS are capable of typical 167 MHz and 1.2 LVCMOS at 100 MHz interfacing frequency with 10 pF load.

For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specification, refer to the –3 speed grade column, unless otherwise specified.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1–42 lists the high-speed I/O timing for Stratix IV devices.

Table 1–42. High-Speed I/O Specifications (1), (2) (Part 1 of 3)

Symbol	Conditions	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (3)	5	—	800 (4)	5	—	717	5	—	717	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (12)	Clock boost factor W = 1 to 40 (3)	5	—	800	5	—	717	5	—	717	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (13)	Clock boost factor W = 1 to 40 (3)	5	—	520	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	800 (9)	5	—	717 (9)	5	—	717 (9)	MHz

Table 1–42. High-Speed I/O Specifications (1), (2) (Part 2 of 3)

Symbol	Conditions	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (10), (11)	(5)	—	1600	(5)	—	1250	(5)	—	1250	Mbps
	SERDES factor J = 2, Uses DDR Registers	(5)	—	(6)	(5)	—	(6)	(5)	—	(6)	Mbps
	SERDES factor J = 1, Uses an SDR Register	(5)	—	(6)	(5)	—	(6)	(5)	—	(6)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (7)	SERDES factor J = 4 to 10	(5)	—	1250	(5)	—	1152	(5)	—	800	Mbps
Emulated Differential I/O Standards with One External Output Resistor - f_{HSDR} (data rate)		(5)	—	311	(5)	—	200	(5)	—	200	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.25	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.125	—	—	0.15	—	—	0.15	UI
t_{DUTY}	Tx output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor	—	—	460	—	—	500	—	—	500	ps

Table 1–42. High-Speed I/O Specifications (1), (2) (Part 3 of 3)

Symbol	Conditions	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TCCS	True Differential I/O Standards	—	—	100	—	—	100	—	—	100	ps
	Emulated Differential I/o Standards	—	—	250	—	—	250	—	—	250	ps
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (11)	150	—	1600	150	—	1250	150	—	1250	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(5)	—	(8)	(5)	—	(8)	(5)	—	(8)	Mbps
	SERDES factor J = 2, Uses DDR Registers	(5)	—	(6)	(5)	—	(6)	(5)	—	(6)	Mbps
	SERDES factor J = 1, Uses an SDR Register	(5)	—	(6)	(5)	—	(6)	(5)	—	(6)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	± PPM
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 1–42:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) For 820, 530, 360, and 290 density devices, the frequency is 762 MHz.

(5) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(6) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

(7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.

(9) This is achieved by using the LVDS and DPA clock network.

(10) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(11) The f_{MAX} specification is based on the fast clock used for serial data. The interface f_{MAX} also depends on the parallel clock domain, which is design dependent and requires timing analysis.

(12) This only applies to DPA and soft-CDR modes.

(13) This only applies to LVDS source synchronous mode.

Programmable IOE Delay

Table 1–52 lists the Stratix IV IOE programmable delay settings.

Table 1–52. IOE Programmable Delay for Stratix IV Devices

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model					
			Industrial/ Military	Commercial (3)	C2 (3)	C3	C4	I3/M3	I4	Unit
D1	16	0	0.462	0.505	0.732	0.795	0.857	0.801	0.864	ns
D2	8	0	0.234	0.232	0.337	0.372	0.407	0.371	0.405	ns
D3	8	0	1.700	1.769	2.695	2.927	3.157	2.948	3.178	ns
D4	16	0	0.508	0.554	0.813	0.882	0.952	0.889	0.959	ns
D5	16	0	0.472	0.500	0.747	0.799	0.875	0.817	0.882	ns
D6	7	0	0.186	0.195	0.294	0.319	0.345	0.321	0.347	ns

Notes to Table 1–52:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
(2) Minimum offset does not include the intrinsic delay.
(3) For the EP4SGX530 device density, the IOE programmable delays have an additional 5% maximum offset.

Programmable Output Buffer Delay

Table 1–53 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 1–53. Programmable Output Buffer Delay (1)

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Note to Table 1–53:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Table 1–54. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block: Clock Boost Factor
X, Y, Z	—	—

Document Revision History

Table 1–55 lists the revision history for this chapter.

Table 1–55. Document Revision History (Part 1 of 3)

Date	Version	Changes
September 2014	5.9	■ Removed the Remote Update only in fast AS mode programming mode from the "Configuration Mode Specifications for Stratix IV Devices" table.
March 2014	5.8	■ Added note to Table 1–49. ■ Updated D6 row in Table 1–52.
January 2014	5.7	■ Updated Table 1–42.
December 2013	5.6	■ Updated Table 1–23 and Table 1–24.
November 2013	5.5	■ Updated Table 1–23 and Table 1–24.
November 2013	5.4	■ Updated Table 1–42, Table 1–23, and Table 1–24.
July 2012	5.3	■ Added Table 1–5 and Table 1–40. ■ Updated Table 1–15, Table 1–22, Table 1–23, Table 1–30, Table 1–33, Table 1–35, Table 1–36, Table 1–39, Table 1–42 and Table 1–51. ■ Removed "Schmitt Trigger Input" section.

Table 1–55. Document Revision History (Part 3 of 3)

Date	Version	Changes
November 2009	4.0	■ Added Table 1–9, Table 1–15, Table 1–38, and Table 1–39. ■ Added Figure 1–5 and Figure 1–6. ■ Added the "Transceiver Datapath PCS Latency" section. ■ Updated the "Electrical Characteristics", "Operating Conditions", and "I/O Timing" sections. ■ All tables updated except Table 1–16, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–33, Table 1–34, and Table 1–45. ■ Updated Figure 1–2 and Figure 1–3. ■ Updated Equation 1–1. ■ Deleted Table 1-28, Table 1-29, Table 1-30, Table 1-42, Table 1-43, and Table 1-44. ■ Minor text edits.
June 2009	3.1	■ Added "Preliminary Specifications" to the footer of each page. ■ Updated Table 1–1, Table 1–2, Table 1–7, Table 1–10, Table 1–11, Table 1–12, Table 1–21, Table 1–22, Table 1–23, Table 1–25, Table 1–37, Table 1–38, Table 1–39, Table 1–40, and Table 1–44. ■ Minor text edits.
March 2009	3.0	■ Replaced Table 1–31 and Table 1–37. ■ Updated Table 1–1, Table 1–2, Table 1–5, Table 1–19, Table 1–41, Table 1–44, Table 1–45, Table 1–49, and Table 1–51. ■ Added Table 1–21, Table 1–46, and Table 1–47 ■ Added Figure 1–3. ■ Removed "Timing Model", "Preliminary and Final Timing", "I/O Timing Measurement Methodology", "I/O Default Capacitive Loading", and "Referenced Documents" sections.
December 2008	2.1	Minor changes.
November 2008	2.0	■ Minor text edits. ■ Updated Table 1–19, Table 1–32, Table 1–34 - Table 1–39. ■ Minor text edits.
August 2008	1.1	■ Updated Table 1–1, Table 1–2, Table 1–4, Table 1–5, and Table 1–26. ■ Removed figures from "Transceiver Performance Specifications" on page 1–10 that are repeated in the glossary. ■ Minor text edits and an additional note to Table 1–26.
May 2008	1.0	Initial release.