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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	21248
Number of Logic Elements/Cells	531200
Total RAM Bits	28033024
Number of I/O	654
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-HBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4s100g5h40i2n

Chapter Revision Dates

The chapters in this document, Stratix IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. DC and Switching Characteristics for Stratix IV Devices
Revised: *September 2014*
Part Number: *SIV54001-5.9*

Chapter 2. Addendum to the Stratix IV Device Handbook
Revised: *February 2011*
Part Number: *SIV54002-1.5*

CAUTION

Conditions other than those listed in Table 1–1, Table 1–2, and Table 1–3 may cause permanent damage to the device. Addition ally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Stratix IV Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	-0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V_{CCPGM}	Configuration pins power supply	-0.5	3.75	V
V_{CCAUX}	Auxiliary supply for the programmable power technology	-0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_{CCPD}	I/O pre-driver power supply	-0.5	3.75	V
V_{CCIO}	I/O power supply	-0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply	-0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	-0.5	1.35	V
V_{CCA_PLL}	PLL analog power supply	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
I_{OUT}	DC output current per pin	-25	40	mA
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (No bias)	-65	150	°C

Table 1–2. Transceiver Power Supply Absolute Maximum Ratings for Stratix IV GX Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	-0.5	3.75	V
V_{CCA_R}	Transceiver high voltage power (right side)	-0.5	3.75	V
V_{CCHIP_L}	Transceiver HIP digital power (left side)	-0.5	1.35	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	-0.5	1.35	V
V_{CCR_L}	Receiver power (left side)	-0.5	1.35	V
V_{CCR_R}	Receiver power (right side)	-0.5	1.35	V
V_{CCT_L}	Transmitter power (left side)	-0.5	1.35	V
V_{CCT_R}	Transmitter power (right side)	-0.5	1.35	V
V_{CCL_GXBLn} (1)	Transceiver clock power (left side)	-0.5	1.35	V
V_{CCL_GXBRn} (1)	Transceiver clock power (right side)	-0.5	1.35	V
V_{CCH_GXBLn} (1)	Transmitter output buffer power (left side)	-0.5	1.8	V
V_{CCH_GXBRn} (1)	Transmitter output buffer power (right side)	-0.5	1.8	V

Note to Table 1–2:

(1) n = 0, 1, 2, or 3.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–4 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–4 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half of a year.

Table 1–4. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	4.0	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%

Temperature Overshoot Above Maximum Allowed Temperature

The maximum allowed operating temperature for Stratix IV industrial grade devices is 100 °C. It is recommended that the operating temperature of the device is maintained below 100 °C at all times. The temperature excursions over 100 °C due to internal heating of the device should not exceed the number of cycles as specified in the Table 1–5. Exceeding the recommended number of cycles may cause solder interconnect failures. Altera® recommends using the Stratix IV military grade devices if the application requires operating temperatures over 100 °C.

Table 1–5. Temperature Overshoot Above Maximum Allowed Temperature

Description	Operating Temperature (°C)	Number of Cycles Over 100 °C
Device operating temperature (°C)	100	3200
	105	768
	110	640
	115	480
	120	320
	125	160

Table 1–11. OCT Calibration Accuracy Specifications for Stratix IV Devices (Part 2 of 2) *(1)*

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3, M3	C4,I4	
25-Ω $R_{S\_left\_shift}$ 3.0, 2.5, 1.8, 1.5, 1.2	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%

Notes to Table 1–11:

(1) OCT calibration accuracy is valid at the time of calibration only.
(2) 25-Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.
(3) 20-Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change. Table 1–12 lists the Stratix IV OCT without calibration resistance tolerance to PVT changes.

Table 1–12. OCT Without Calibration Resistance Tolerance Specifications for Stratix IV Devices

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3,I3, M3	C4,I4	
25-Ω R_S 3.0 and 2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	± 30	± 40	± 40	%
25-Ω R_S 1.8 and 1.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	± 30	± 40	± 40	%
25-Ω R_S 1.2	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	± 35	± 50	± 50	%
50-Ω R_S 3.0 and 2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	± 30	± 40	± 40	%
50-Ω R_S 1.8 and 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	± 30	± 40	± 40	%
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	± 35	± 50	± 50	%
100-Ω R_D 2.5	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5 V	± 25	± 25	± 25	%

Table 1–14. Pin Capacitance for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Value	Unit
C_{OUTFB}	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Hot Socketing

Table 1–15lists the hot socketing specifications for Stratix IV devices.

Table 1–15. Hot Socketing Specifications for Stratix IV Devices

Symbol	Description	Maximum
$I_{IOPIN (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR-TX (DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVR-RX (DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $I_{IOPIN} = C$ dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 1–16lists the weak pull-up resistor values for Stratix IV devices.

Table 1–16. Internal Weak Pull-Up Resistor for Stratix IV Devices (1), (3)

Symbol	Description	Conditions (V)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.0 ±5% (2)	25	kΩ
		V_{CCIO} = 2.5 ±5% (2)	25	kΩ
		V_{CCIO} = 1.8 ±5% (2)	25	kΩ
		V_{CCIO} = 1.5 ±5% (2)	25	kΩ
		V_{CCIO} = 1.2 ±5% (2)	25	kΩ

Notes to Table 1–16:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(4) These specifications are valid with ±10% tolerances to cover changes over PVT.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 1–23lists the Stratix IV GX transceiver specifications.

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 1 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.4 V PCML 1.5 V PCML, 2.5 V PCML, Differential LVPECL, LVDS, HCSL (4)										
Input frequency from REFCLK input pins	—	50	—	697	50	—	697	50	—	637.5	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	425	50	—	325	50	—	325	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a REFCLK pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Rise/fall time (21)	—	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	1100 ± 10%			1100 ± 10%			1100 ± 10%			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 5 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 3	—	9	—	—	9	—	—	9	—	dB
	DC Gain Setting = 4	—	12	—	—	12	—	—	12	—	dB
EyeQ Data Rate	—	600	—	3250	600	—	3250	600	—	3250	Mbps
AEQ Data Rate	min V_{ID} (diff p-p) outer envelope = 600 mV 8B/10B encoded data	2500	—	6500	2500	—	6500	—	—	—	Mbps
Decision Feedback Equalizer (DFE) Data Rate	min V_{ID} (diff p-p) outer envelope = 500 mV	3125	—	6500	3125	—	6500	—	—	—	Mbps
Transmitter											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML										
Data rate (Single width, non-PMA Direct)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	8500	1000	—	6500	1000	—	6375 (22)	Mbps
Data rate (Single width, PMA Direct)	—	600	—	3250	600	—	3250	600	—	3250	Mbps
Data rate (Double width, PMA Direct) (13)	—	1000	—	6500	1000	—	6500	1000	—	6375	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85–Ω setting	85 ± 15%			85 ± 15%			85 ± 15%			Ω
	100–Ω setting	100 ± 15%			100 ± 15%			100 ± 15%			Ω
	120–Ω setting	120 ± 15%			120 ± 15%			120 ± 15%			Ω
	150-Ω setting	150 ± 15%			150 ± 15%			150 ± 15%			Ω

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 7 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade (1)			–3 Military (2) and –4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block skew in Basic (PMA Direct) ×N mode (15)	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	—	—	400	—	—	400	ps
	N≥ 18 channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks	—	—	650	—	—	650	—	—	650	ps
CMU0 PLL and CMU1 PLL											
Supported Data Range	—	600	—	8500	600	—	6500	600	—	6375	Mbps
`pll_powerdown` minimum pulse width (`tpll_powerdown`)	—	1									µs
CMU PLL lock time from `pll_powerdown` de-assertion	—	—	—	100	—	—	100	—	—	100	µs

Table 1–25through Table 1–28lists the typical differential V_{OD} termination settings for Stratix IV GX and GT devices.

Table 1–25. Typical V_{OD} Setting, TX Term = 85 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	170 ± 20%	340 ± 20%	510 ± 20%	595 ± 20%	680 ± 20%	765 ± 20%	850 ± 20%	1020 ± 20%

Table 1–26. Typical V_{OD} Setting, TX Term = 100 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	200 ± 20%	400 ± 20%	600 ± 20%	700 ± 20%	800 ± 20%	900 ± 20%	1000 ± 20%	1200 ± 20%

Table 1–27. Typical V_{OD} Setting, TX Term = 120 Ω

Symbol	V_{OD} Setting (mV)						
	0	1	2	3	4	5	6
V_{OD} differential peak-to-peak Typical (mV)	240 ± 20%	480 ± 20%	720 ± 20%	840 ± 20%	960 ± 20%	1080 ± 20%	1200 ± 20%

Table 1–28. Typical V_{OD} Setting, TX Term = 150 Ω

Symbol	V_{OD} Setting (mV)					
	0	1	2	3	4	5
V_{OD} differential peak-to-peak Typical (mV)	300 ± 20%	600 ± 20%	900 ± 20%	1050 ± 20%	1200 ± 20%	1350 ± 20%

Table 1–29lists typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed inTable 1–29are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Stratix IV HSSI HSPICE models.

Table 1–29. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 1 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0

Table 1–29. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 3 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military (3) and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter at 5 Gbps (Gen2)	Compliance pattern		Compliant			Compliant			—		UI
PCIe (Gen 1) Electrical Idle Detect Threshold											
$V_{RX-IDLE-DETDIFFp-p}$ (16)	Compliance pattern	65	—	175	65	—	175	65	—	175	UI
Serial RapidIO Transmit Jitter Generation (8)											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Serial RapidIO Receiver Jitter Tolerance (8)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation (9)											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices [1], [2] (Part 9 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military [3] and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter tolerance at 3072 Mbps	Jitter Frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI

Notes to Table 1–30:

(1) Dedicated refclk pins were used to drive the input reference clocks.
(2) The Jitter numbers are valid for the stated conditions only.
(3) Stratix IV GX devices in military speed grade only support select transceiver configuration up to 3125 Mbps. For more information, contact Altera sales representative.
(4) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(5) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(6) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(7) The jitter numbers for PCI Express (PIPE) (PCIe) are compliant to the PCIe Base Specification 2.0.
(8) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(9) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(10) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(11) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(13) The fibre channel transmitter jitter generation numbers are compliant to the specification at 8.5 Gbps interoperability point.
(14) The fibre channel receiver jitter tolerance numbers are compliant to the specification at 8.5 Gbps interoperability point.
(15) You must use the ATX PLL adjacent to the transceiver channels to meet the transmitter jitter generation compliance in PCIe Gen2 ×8 modes.
(16) Stratix IV PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50mV.
(17) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
(18) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
(19) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

PLL Specifications

Table 1–34lists the Stratix IV PLL specifications when operating in the commercial (0° to 85°C), industrial (–40° to 100°C), and military (–55°C to 125°C) junction temperature ranges.

Table 1–34. PLL Specifications for Stratix IV Devices (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–2/–2x speed grade)		5	—	800 (3) MHz
	Input clock frequency (–3 speed grade)		5	—	717 (3) MHz
	Input clock frequency (–4 speed grade)		5	—	717 (3) MHz
f_{INPFD}	Input frequency to the PFD		5	—	325 MHz
f_{VCO} (2)	PLL VCO operating range (–2 speed grade)		600	—	1600 MHz
	PLL VCO operating range (–3 speed grade)		600	—	1300 MHz
	PLL VCO operating range (–4 speed grade)		600	—	1300 MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle		40	—	60 %
f_{OUT}	Output frequency for internal global or regional clock (–2/–2x speed grade)	—	—	800 (3)	MHz
	Output frequency for internal global or regional clock (–3 speed grade)	—	—	717 (3)	MHz
	Output frequency for internal global or regional clock (–4 speed grade)	—	—	717 (3)	MHz
f_{OUT_EXT}	Output frequency for external clock output (–2 speed grade)		—	— (3)	800 MHz
	Output frequency for external clock output (–3 speed grade)		—	— (3)	717 MHz
	Output frequency for external clock output (–4 speed grade)		—	— (3)	717 MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)		45	50	55 %
t_{FCOMP}	External feedback clock compensation time		—	—	10 ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain		—	3.5	— scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift		—	1	— scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth		—	0.3	— MHz
	PLL closed-loop medium bandwidth		—	1.5	— MHz
	PLL closed-loop high bandwidth (9)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift		—	—	±50 ps
t_{ARESET}	Minimum pulse width on the areset signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle to cycle jitter ($F_{REF} \geq$ 100 MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter (F_{REF} < 100 MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} (6)	Period Jitter for dedicated clock output ($F_{OUT} \geq$ 100 MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output (F_{OUT} < 100 MHz)	—	—	17.5	mUI (p-p)

Table 1–34. PLL Specifications for Stratix IV Devices (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{OUTCCJ_DC} (6)	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq$ 100 MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output (F_{OUT} < 100 MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (6), (9)	Period Jitter for clock output on regular I/O ($F_{OUT} \geq$ 100 MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O (F_{OUT} < 100 MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (6), (9)	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq$ 100 MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O (F_{OUT} < 100 MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ (6), (7)	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq$100MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs (F_{OUT}< 100MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 us	—	—	±10	%

Notes to Table 1–34:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(3) This specification is limited by the lower of the two: I/O_{MAX} or F_{OUT} of the PLL.

(4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.

(5) F_{REF} is fIN/N when N = 1.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–51 on page 1–62

(7) The cascaded PLL specification is applicable with the following condition:
A. Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
B. Downstream PLL: Downstream PLL BW > 2 MHz

(8) High bandwidth PLL settings are not supported in external feedback mode.

(9) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–49 on page 1–61