Intel - EPM3064ATC44-10NAF Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	34
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm3064atc44-10naf

...and More Features

- PCI compatible
- Bus–friendly architecture including programmable slew–rate control
- Open–drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power–saving mode for a power reduction of over 50% in each macrocell
- Configurable expander product–term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - 6 or 10 pin– or logic–driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Programmable output slew–rate control
- Software design support and automatic place–and–route provided by Altera's development systems for Windows–based PCs and Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from third–party manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with the Altera master programming unit (MPU), MasterBlaster™ communications cable, ByteBlasterMV™ parallel port download cable, BitBlaster™ serial download cable as well as programming hardware from third–party manufacturers and any in–circuit tester that supports Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**), Jam STAPL Byte-Code Files (**.jbc**), or Serial Vector Format Files (**.svf**)

General Description

MAX 3000A devices are low–cost, high–performance devices based on the Altera MAX architecture. Fabricated with advanced CMOS technology, the EEPROM–based MAX 3000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 3000A devices in the –4, –5, –6, –7, and –10 speed grades are compatible with the timing requirements of the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 2.

MAX 3000A devices contain 32 to 512 macrocells, combined into groups of 16 macrocells called logic array blocks (LABs). Each macrocell has a programmable–AND / fixed–OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander and high–speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 3000A devices provide programmable speed / power optimization. Speed–critical portions of a design can run at high speed / full power, while the remaining portions run at reduced speed / low power. This speed / power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 3000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non–speed–critical signals are switching. The output drivers of all MAX 3000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5–V, 3.3–V, and 5.0-V tolerant, allowing MAX 3000A devices to be used in mixed–voltage systems.

MAX 3000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry–standard PC– and UNIX–workstation–based EDA tools. The software runs on Windows–based PCs, as well as Sun SPARCstation, and HP 9000 Series 700 / 800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 3000A architecture includes the following elements:

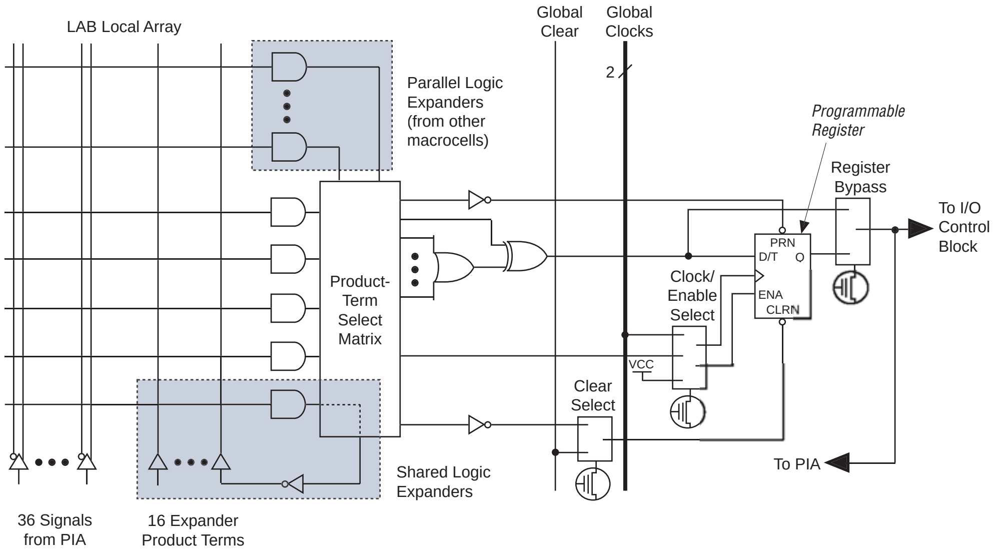
- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array (PIA)
- I / O control blocks

The MAX 3000A architecture includes four dedicated inputs that can be used as general–purpose inputs or as high–speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I / O pin. Figure 1 shows the architecture of MAX 3000A devices.

Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product–term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

Figure 2. MAX 3000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product–term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

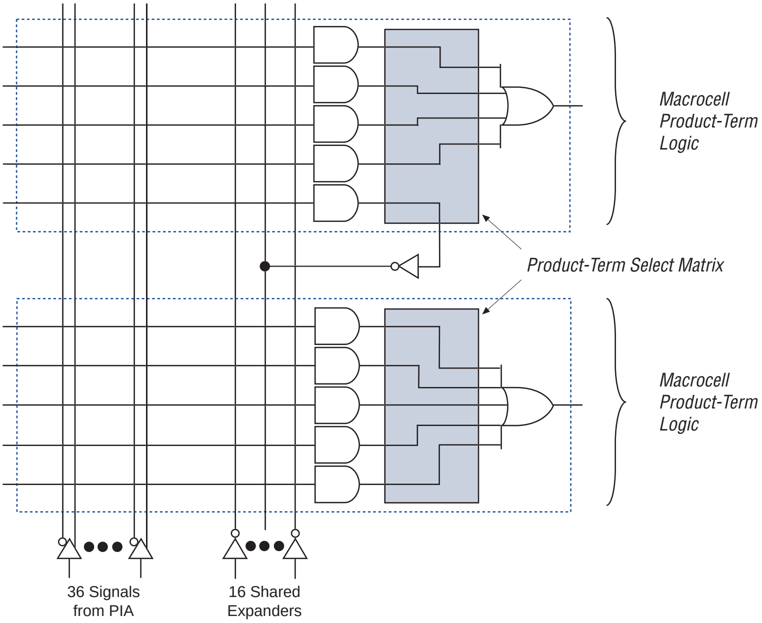
The Altera development system automatically optimizes product–term allocation according to the logic requirements of the design.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders incur a small delay (t_{SEXP}). Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 3000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



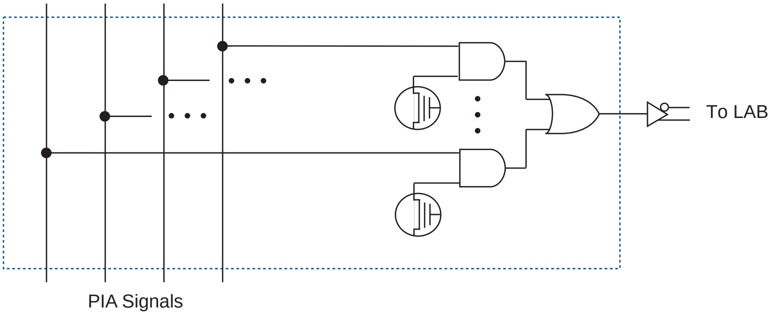
Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 3000A PIA Routing



While the routing delays of channel–based routing schemes in masked or FPGAs are cumulative, variable, and path–dependent, the MAX 3000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri–state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 3000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

In–System Programmability

MAX 3000A devices can be programmed in–system via an industry–standard four–pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in–system programming with only a single 3.3–V power supply. During in–system programming, the I/O pins are tri–stated and weakly pulled–up to eliminate board conflicts. The pull–up value is nominally 50 kΩ.

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an `ISP_Done` bit that ensures safe operation when in–system programming is interrupted. This `ISP_Done` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick–and–place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in–circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high–pin–count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in–circuit testers, PCs, or embedded processors.

For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*, *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code)*.

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

The programming times described in Tables 4 through 6 are associated with the worst-case method using the enhanced ISP algorithm.

Table 4. MAX 3000A t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM3032A	2.00	55,000	0.002	18,000
EPM3064A	2.00	105,000	0.002	35,000
EPM3128A	2.00	205,000	0.002	68,000
EPM3256A	2.00	447,000	0.002	149,000
EPM3512A	2.00	890,000	0.002	297,000

Tables 5 and 6 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 5. MAX 3000A In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM3032A	2.01	2.01	2.03	2.06	2.11	2.28	2.55	3.10	s
EPM3064A	2.01	2.02	2.05	2.11	2.21	2.53	3.05	4.10	s
EPM3128A	2.02	2.04	2.10	2.21	2.41	3.03	4.05	6.10	s
EPM3256A	2.05	2.09	2.23	2.45	2.90	4.24	6.47	10.94	s
EPM3512A	2.09	2.18	2.45	2.89	3.78	6.45	10.90	19.80	s

Table 6. MAX 3000A Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM3032A	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EPM3064A	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EPM3128A	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	s
EPM3256A	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	s
EPM3512A	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	s

Programming with External Hardware

MAX 3000A devices can be programmed on Windows–based PCs with an Altera Logic Programmer card, MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text– or waveform–format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary–Scan Support

MAX 3000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1–1990. Table 7 describes the JTAG instructions supported by MAX 3000A devices. The pin-out tables found on the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 7. MAX 3000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board–level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1–bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`
USERCODE	Selects the 32–bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`
ISP Instructions	These instructions are used when programming MAX 3000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster cable, or when using a Jam STAPL file, JBC file, or SVF file via an embedded processor or test equipment

Programmable Speed/Power Control

MAX 3000A devices offer a power–saving mode that supports low-power operation across user–defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 3000A device for either high–speed or low–power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, t_{CPPW} and t_{SEXP} parameters.

Output Configuration

MAX 3000A device outputs can be programmed to meet a variety of system–level requirements.

MultiVolt I/O Interface

The MAX 3000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 3000A devices to connect to systems with differing supply voltages. MAX 3000A devices in all packages can be set for 2.5–V, 3.3–V, or 5.0–V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCIO` pins can be connected to either a 3.3–V or 2.5–V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 2.5–V power supply, the output levels are compatible with 2.5–V systems. When the `VCCIO` pins are connected to a 3.3–V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0–V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5–V, 3.3–V, or 5.0–V signals.

Table 11 summarizes the MAX 3000A MultiVolt I/O support.

Table 11. MAX 3000A MultiVolt I/O Support

V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓	✓	✓	✓

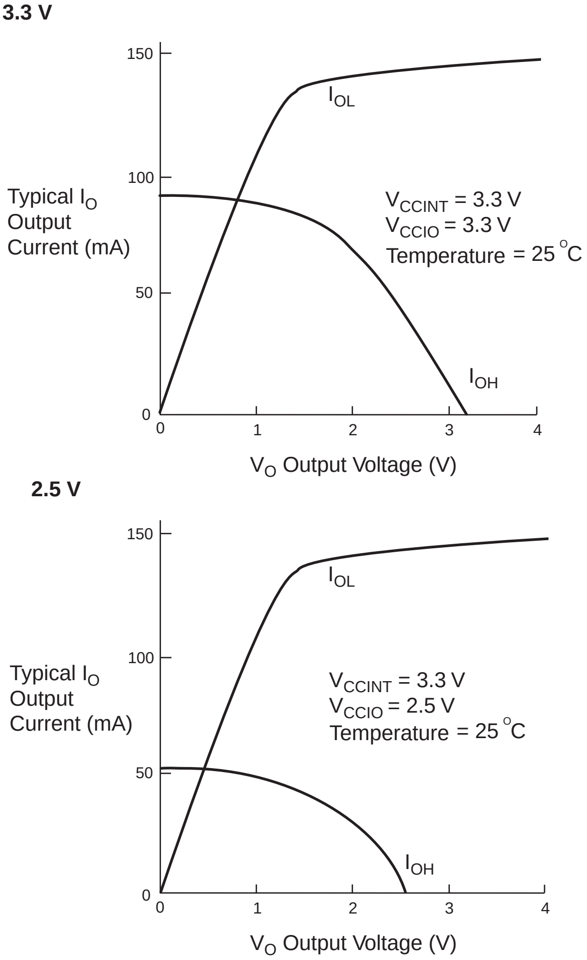
Table 13. MAX 3000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(10)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3–V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5–V operation		2.3	2.7	V
V_{CCISP}	Supply voltage during ISP		3.0	3.6	V
V_I	Input voltage	*(3)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	Commercial range	0	70	° C
		Industrial range	–40	85	° C
T_J	Junction temperature	Commercial range	0	90	° C
		Industrial range *(11)*	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 14. MAX 3000A Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High–level input voltage		1.7	5.75	V
V_{IL}	Low–level input voltage		–0.5	0.8	V
V_{OH}	3.3–V high–level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(5)*	2.4		V
	3.3–V high–level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(5)*	V_{CCIO} – 0.2		V
	2.5–V high–level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V *(5)*	2.1		V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(5)*	2.0		V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(5)*	1.7		V
V_{OL}	3.3–V low–level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(6)*		0.4	V
	3.3–V low–level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(6)*		0.2	V
	2.5–V low–level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(6)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(6)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(6)*		0.7	V
I_I	Input leakage current	V_I = –0.5 to 5.5 V *(7)*	–10	10	µA
I_{OZ}	Tri–state output off–state current	V_I = –0.5 to 5.5 V *(7)*	–10	10	µA
R_{ISP}	Value of I/O pin pull–up resistor when programming in–system or during power–up	V_{CCIO} = 2.3 to 3.6 V *(8)*	20	74	kΩ

Figure 9. Output Drive Characteristics of MAX 3000A Devices



3.3 V

2.5 V

Power Sequencing & Hot–Socketing

Because MAX 3000A devices can be used in a mixed–voltage environment, they have been designed specifically to tolerate any possible power–up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 3000A devices before and during power-up without damaging the device. In addition, MAX 3000A devices do not drive out during power-up. Once operating conditions are reached, MAX 3000A devices operate as specified by the user.

Table 17. EPM3032A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–4		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.2		1.5	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.2		1.5	ns
t_{SEXP}	Shared expander delay			1.9		3.1		4.0	ns
t_{PEXP}	Parallel expander delay			0.5		0.8		1.0	ns
t_{LAD}	Logic array delay			1.5		2.5		3.3	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.8		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.7		1.2		1.5	ns
t_{COMB}	Combinatorial delay			0.6		1.0		1.3	ns
t_{IC}	Array clock delay			1.2		2.0		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			0.8		1.3		1.9	ns
t_{PRE}	Register preset time			1.2		1.9		2.6	ns
t_{CLR}	Register clear time			1.2		1.9		2.6	ns
t_{PIA}	PIA delay	*(2)*		0.9		1.5		2.1	ns

Table 20. EPM3128A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	192.3		129.9		98.0		MHz

Table 21. EPM3128A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.0		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.0		1.4	ns
t_{SEXP}	Shared expander delay			2.0		2.9		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.6		2.4		3.1	ns
t_{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns

Table 21. EPM3128A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{SU}	Register setup time		1.4		2.1		2.9		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.8		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.7		2.2	ns
t_{EN}	Register enable time			0.7		1.0		1.3	ns
t_{GLOB}	Global control delay			1.1		1.6		2.0	ns
t_{PRE}	Register preset time			1.4		2.0		2.7	ns
t_{CLR}	Register clear time			1.4		2.0		2.7	ns
t_{PIA}	PIA delay	*(2)*		1.4		2.0		2.6	ns
t_{LPA}	Low–power adder	*(5)*		4.0		4.0		5.0	ns

Table 22. EPM3256A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			–7		–10		
			Min	Max	Min	Max	
t_{PD1}	Input to non–registered output	C1 = 35 pF *(2)*		7.5		10	ns
t_{PD2}	I/O input to non–registered output	C1 = 35 pF *(2)*		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	5.2		6.9		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.8	1.0	6.4	ns
t_{CH}	Global clock high time		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.7		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	7.3	1.0	9.7	ns
t_{ACH}	Array clock high time		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		4.0		ns

Table 22. EPM3256A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			–7		–10		
			Min	Max	Min	Max	
t_{CNT}	Minimum global clock period	*(2)*		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	*(2)*		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	126.6		95.2		MHz

Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			–7		–10		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.9		1.2	ns
t_{SEXP}	Shared expander delay			2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.5		0.6	ns
t_{LAD}	Logic array delay			2.2		2.8	ns
t_{LAC}	Logic control array delay			1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		5.5	ns

Table 23. EPM3256A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			–7		–10		
			Min	Max	Min	Max	
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0	ns
t_{SU}	Register setup time		2.1		2.9		ns
t_H	Register hold time		0.9		1.2		ns
t_{RD}	Register delay			1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.8		1.2	ns
t_{IC}	Array clock delay			1.6		2.1	ns
t_{EN}	Register enable time			1.0		1.3	ns
t_{GLOB}	Global control delay			1.5		2.0	ns
t_{PRE}	Register preset time			2.3		3.0	ns
t_{CLR}	Register clear time			2.3		3.0	ns
t_{PIA}	PIA delay	*(2)*		2.4		3.2	ns
t_{LPA}	Low–power adder	*(5)*		4.0		5.0	ns

Table 24. EPM3512A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	5.6		7.6		ns
t_H	Global clock hold time	*(2)*	0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	ns
t_{CH}	Global clock high time		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.5		3.5		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		ns

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$I_{CCINT} =$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in the I_{CCINT} equation are:

MC_{TON} = Number of macrocells with the Turbo Bit^{TM} option turned on, as reported in the Quartus II or MAX+PLUS II Report File (**.rpt**)

MC_{DEV} = Number of macrocells in the device

MC_{USED} = Total number of macrocells in the design, as reported in the RPT File

$\mathbf{f_{MAX}}$ = Highest clock frequency to the device

$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)

A, B, C = Constants (shown in Table 26)

Table 26. MAX 3000A I_{CC} Equation Constants

Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The I_{CCINT} calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16–bit, loadable, enabled, up / down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

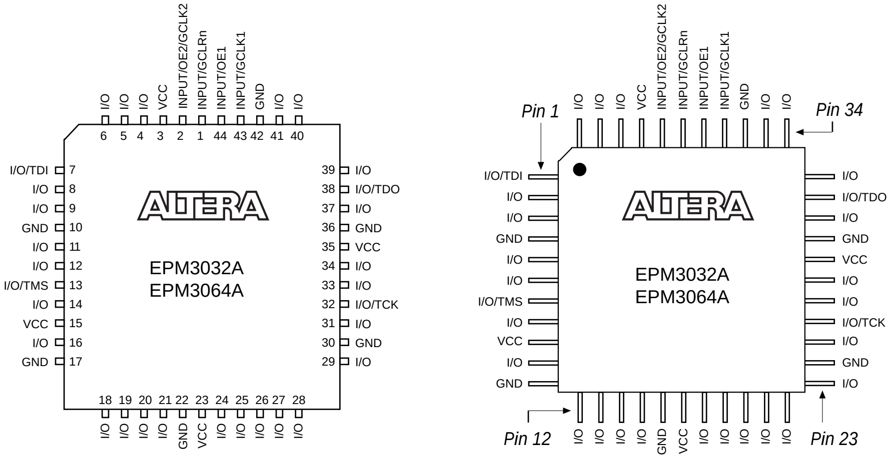
Device Pin–Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin–out information.

Figures 14 through 18 show the package pin–out diagrams for MAX 3000A devices.

Figure 14. 44–Pin PLCC/TQFP Package Pin–Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TQFP

Version 3.2

The following change were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.2:

- Updated the EPM3512 I_{CC} versus frequency graph in Figure 13.

Version 3.1

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.1:

- Updated timing information in Table 1 for the EPM3256A device.
- Updated *Note (10)* of Table 15.

Version 3.0

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.0:

- Added EPM3512A device.
- Updated Tables 2 and 3.

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