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# Understanding <u>Embedded - FPGAs (Field Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	185
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c12f256c7n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

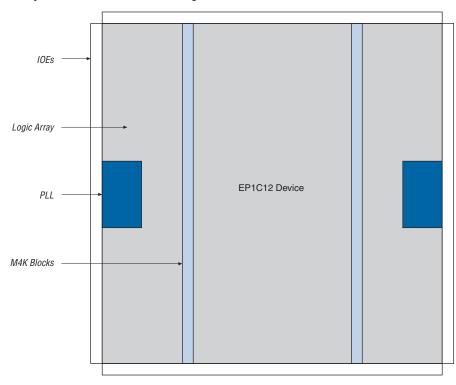


Figure 2-1. Cyclone EP1C12 Device Block Diagram

The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

Table 2–1. Cyclone Device Resources									
Davisa	M4K	PLLs	LAB Columns	LADD					
Device	Columns	Blocks	PLLS	LAD CUIUIIIIS	LAB Rows				
EP1C3	1	13	1	24	13				
EP1C4	1	17	2	26	17				
EP1C6	1	20	2	32	20				
EP1C12	2	52	2	48	26				
EP1C20	2	64	2	64	32				

# Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, look-up table (LUT) chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within a LAB. The Quartus® II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 details the Cyclone LAB.

Row Interconnect Column Interconnect Direct link interconnect from Direct link adjacent block interconnect from adjacent block Direct link Direct link interconnect to interconnect to adjacent block adjacent block LÄB Local Interconnect

Figure 2-2. Cyclone LAB Structure

#### LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, and M4K RAM blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack<sup>TM</sup> interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

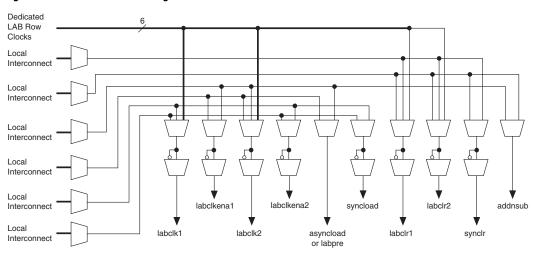


Figure 2-4. LAB-Wide Control Signals

# **Logic Elements**

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–2 shows the Cyclone device's routing scheme.

Table 2–2. Cyclone Device Routing Scheme											
					D	estinatio	on				
Source	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	C4 Interconnect	31	M4K RAM Block	PLL	Column 10E	Row 10E
LUT Chain	_	_	_	_	_	_	<b>✓</b>	_	_	_	_
Register Chain	_	_	_	_	_	_	<b>✓</b>	_	_	_	_
Local Interconnect	_	_	_	_	_	_	<b>✓</b>	~	<b>✓</b>	~	<b>✓</b>
Direct Link Interconnect	_	_	<b>✓</b>	_	_	_	_	_	_	_	_
R4 Interconnect	_	_	<b>✓</b>	_	<b>✓</b>	<b>✓</b>	_	_	_	_	_
C4 Interconnect	_	_	<b>✓</b>	_	<b>✓</b>	<b>✓</b>	_	_	_	_	_
LE	<b>✓</b>	<b>✓</b>	~	~	<b>✓</b>	<b>✓</b>	_	_	_	_	_
M4K RAM Block	_	_	<b>✓</b>	<b>✓</b>	<b>✓</b>	<b>✓</b>	_	_	_	_	_
PLL	_	_	_	<b>✓</b>	<b>✓</b>	<b>✓</b>	_	_	_	_	_
Column IOE	_	_	_	_	_	<b>✓</b>	_	_	_	_	_
Row IOE	_	_	_	<b>✓</b>	<b>✓</b>	<b>✓</b>	_	_	_	_	_

is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4	K KAM BI	OCK Conf	iguration	s (Simple	Duai-Port)				
Read Port	Write Port								
neau ruii	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	<b>✓</b>	<b>✓</b>	<b>✓</b>	~	<b>✓</b>	<b>✓</b>	_	_	_
2K × 2	<b>✓</b>	<b>✓</b>	<b>✓</b>	<b>✓</b>	<b>✓</b>	<b>✓</b>	_	_	_
1K × 4	~	<b>✓</b>	<b>✓</b>	~	<b>✓</b>	<b>✓</b>	_	_	_
512 × 8	<b>✓</b>	<b>✓</b>	<b>✓</b>	~	<b>✓</b>	<b>✓</b>	_	_	_
256 × 16	~	<b>✓</b>	<b>✓</b>	~	<b>✓</b>	<b>✓</b>	_	_	_
128 × 32	<b>✓</b>	<b>✓</b>	<b>✓</b>	~	<b>✓</b>	<b>✓</b>	_	_	_
512 × 9	_	_	_	_	_	_	✓	~	<b>✓</b>
256 × 18	_	_	_	_	_	_	<b>✓</b>	~	<b>✓</b>
128 × 36	<u> </u>	_	_	_	_	_	<b>✓</b>	<b>✓</b>	<b>✓</b>

Table 2–4. M4K RAM Block Configurations (True Dual-Port)										
Dovt A		Port B								
Port A	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18			
4K × 1	✓	<b>✓</b>	<b>✓</b>	<b>✓</b>	<b>✓</b>	_	_			
2K × 2	<b>✓</b>	<b>✓</b>	<b>✓</b>	<b>✓</b>	✓	_	_			
1K × 4	✓	✓	✓	✓	<b>✓</b>	_	_			
512 × 8	✓	✓	✓	✓	<b>✓</b>	_	_			
256 × 16	✓	✓	✓	✓	<b>✓</b>	_	_			
512 × 9	_	_	_	_	_	<b>✓</b>	<b>✓</b>			
256 × 18	_	_	_	_	_	✓	<b>✓</b>			

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits  $(w \times m \times n)$ .

### **Programmable Duty Cycle**

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

# **Control Signals**

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

The pllenable signal enables and disables PLLs. When the pllenable signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the pllenable signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the pllenable signal.

The areset signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When areset is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The pfdena signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the pfdena signal.



For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

# I/O Structure

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

Cyclone device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–27 shows the Cyclone IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. IOEs can be used as input, output, or bidirectional pins.

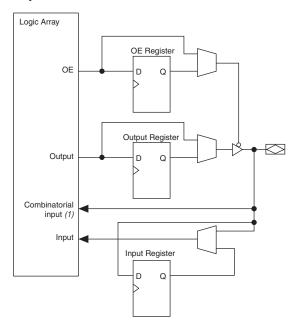


Figure 2-27. Cyclone IOE Structure

Note to Figure 2-27:

 There are two paths available for combinatorial inputs to the logic array. Each path contains a unique programmable delay chain.

The IOEs are located in I/O blocks around the periphery of the Cyclone device. There are up to three IOEs per row I/O block and up to three IOEs per column I/O block (column I/O blocks span two columns). The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–28 shows how a row I/O block connects to the logic array. Figure 2–29 shows how a column I/O block connects to the logic array.

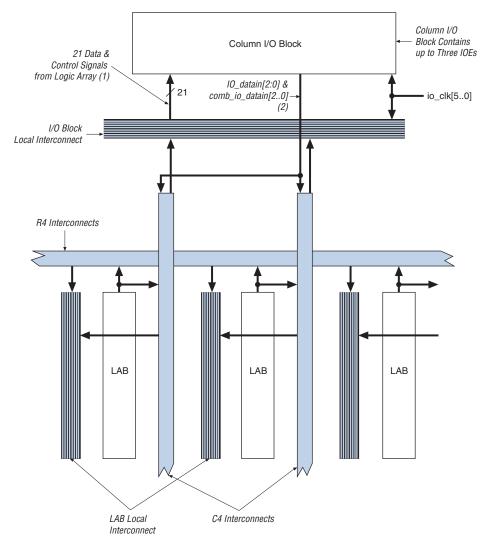


Figure 2-29. Column I/O Block Connection to the Interconnect

#### Notes to Figure 2-29:

- (1) The 21 data and control signals consist of three data out lines, io\_dataout[2..0], three output enables, io\_coe[2..0], three input clock enables, io\_cce\_in[2..0], three output clock enables, io\_cce\_out[2..0], three clocks, io\_cclk[2..0], three asynchronous clear signals, io\_caclr[2..0], and three synchronous clear signals, io\_csclr[2..0].
- (2) Each of the three IOEs in the column I/O block can have one io\_datain input (combinatorial or registered) and one comb io datain (combinatorial) input.

The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, io\_clk[5..0], provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see "Global Clock Network and Phase-Locked Loops" on page 2–29). Figure 2–30 illustrates the signal paths through the I/O block.

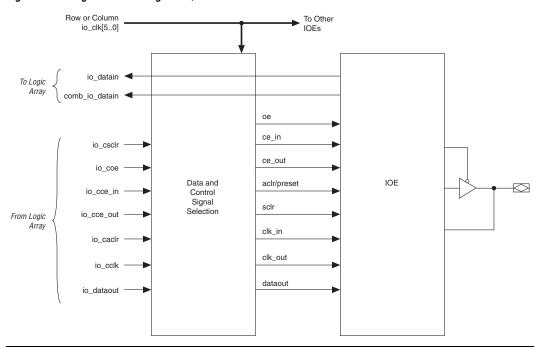


Figure 2-30. Signal Path through the I/O Block

Each IOE contains its own control signal selection for the following control signals: oe, ce\_in, ce\_out, aclr/preset, sclr/preset, clk\_in, and clk\_out. Figure 2–31 illustrates the control signal selection.

## Advanced I/O Standard Support

Cyclone device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- LVDS
- RSDS
- SSTL-2 class I and II
- SSTL-3 class I and II
- Differential SSTL-2 class II (on output clocks only)

Table 2–12 describes the I/O standards supported by Cyclone devices.

Table 2–12. Cyclone I/O Standards								
I/O Standard	Туре	Input Reference Voltage (V <sub>REF</sub> ) (V)	Output Supply Voltage (V <sub>CCIO</sub> ) (V)	Board Termination Voltage (V <sub>TT</sub> ) (V)				
3.3-V LVTTL/LVCMOS	Single-ended	N/A	3.3	N/A				
2.5-V LVTTL/LVCMOS	Single-ended	N/A	2.5	N/A				
1.8-V LVTTL/LVCMOS	Single-ended	N/A	1.8	N/A				
1.5-V LVCMOS	Single-ended	N/A	1.5	N/A				
3.3-V PCI (1)	Single-ended	N/A	3.3	N/A				
LVDS (2)	Differential	N/A	2.5	N/A				
RSDS (2)	Differential	N/A	2.5	N/A				
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25				
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5				
Differential SSTL-2 (3)	Differential	1.25	2.5	1.25				

#### Notes to Table 2-12:

- (1) There is no megafunction support for EP1C3 devices for the PCI compiler. However, EP1C3 devices support PCI by using the LVTTL 16-mA I/O standard and drive strength assignments in the Quartus II software. The device requires an external diode for PCI compliance.
- (2) EP1C3 devices in the 100-pin TQFP package do not support the LVDS and RSDS I/O standards.
- (3) This I/O standard is only available on output clock pins (PLL\_OUT pins). EP1C3 devices in the 100-pin package do not support this I/O standard as it does not have PLL\_OUT pins.

Cyclone devices contain four I/O banks, as shown in Figure 2–35. I/O banks 1 and 3 support all the I/O standards listed in Table 2–12. I/O banks 2 and 4 support all the I/O standards listed in Table 2–12 except the 3.3-V PCI standard. I/O banks 2 and 4 contain dual-purpose DQS, DQ,

Each I/O bank can support multiple standards with the same  $V_{CCIO}$  for input and output pins. For example, when  $V_{CCIO}$  is 3.3-V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

### LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100- termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

Table 2–13. Cyclone Device LVDS Channels					
Device	Pin Count	Number of LVDS Channels			
EP1C3	100	(1)			
	144	34			
EP1C4	324	103			
	400	129			
EP1C6	144	29			
	240	72			
	256	72			
EP1C12	240	66			
	256	72			
	324	103			
EP1C20	324	95			
	400	129			

*Note to Table 2–13:* 

### MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and four sets for I/O output drivers ( $V_{CCIO}$ ).

EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.