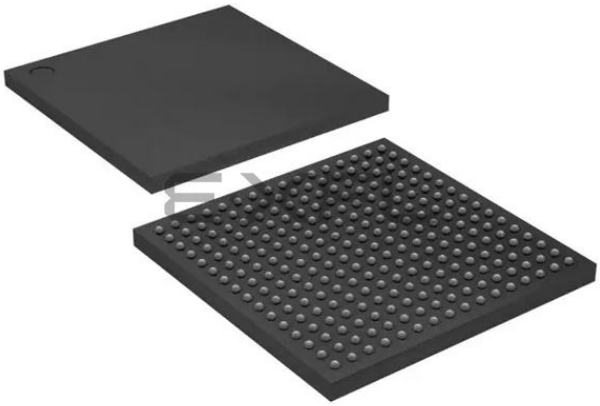

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	185
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c12f256c8

Table 1–1. Cyclone Device Features (Part 2 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Total RAM bits	59,904	78,336	92,160	239,616	294,912
PLLs	1	2	2	2	2
Maximum user I/O pins *(1)*	104	301	185	249	301

Note to Table 1–1:
(1) This parameter includes global clock pins.

Cyclone devices are available in quad flat pack (QFP) and space-saving FineLine® BGA packages (see Tables 1–2 through 1–3).

Table 1–2. Cyclone Package Options and I/O Pin Counts

Device	100-Pin TQFP *(1)*	144-Pin TQFP *(1), (2)*	240-Pin PQFP *(1)*	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
EP1C3	65	104	—	—	—	—
EP1C4	—	—	—	—	249	301
EP1C6	—	98	185	185	—	—
EP1C12	—	—	173	185	249	—
EP1C20	—	—	—	—	233	301

Notes to Table 1–2:
(1) TQFP: thin quad flat pack.
PQFP: plastic quad flat pack.
(2) Cyclone devices support vertical migration within the same package (i.e., designers can migrate between the EP1C3 device in the 144-pin TQFP package and the EP1C6 device in the same package).

Vertical migration means you can migrate a design from one device to another that has the same dedicated pins, JTAG pins, and power pins, and are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must use the layout for the largest planned density in a package to provide the necessary power pins for migration.

For I/O pin migration across densities, cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list. If one device has power or ground pins, but these same pins are user I/O on a different device that is in the migration path,the Quartus II software ensures the pins are not used as user I/O in the Quartus II software. Ensure that these pins are connected

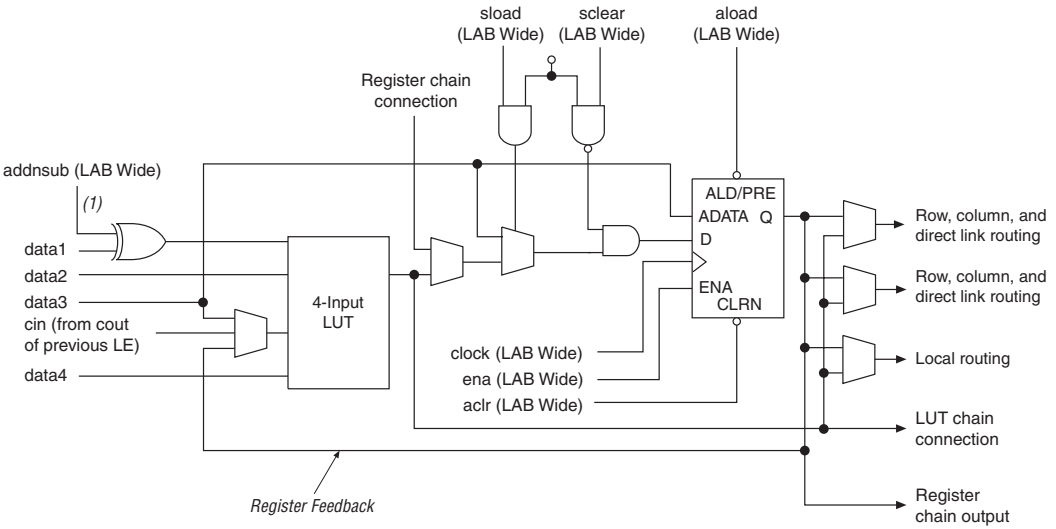
preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

Figure 2–6. LE in Normal Mode



Note to Figure 2–6:
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

Table 2–4. M4K RAM Block Configurations (True Dual-Port)

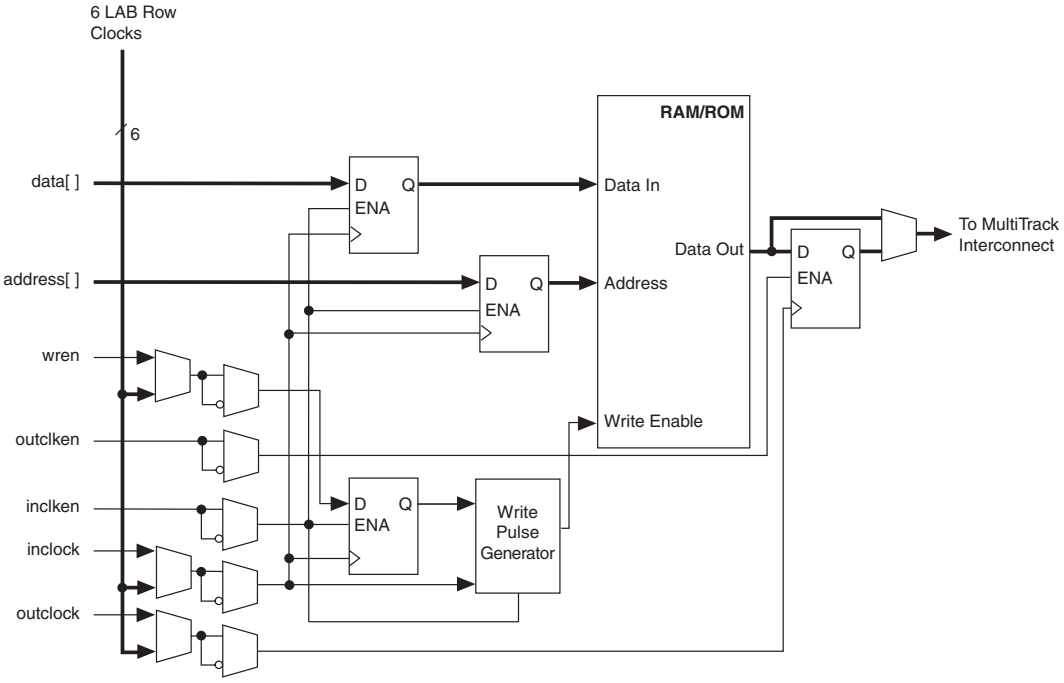
Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Single-Port Mode

The M4K memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–21. A single M4K memory block can support up to two single-port mode RAM blocks if each RAM block is less than or equal to 2K bits in size.

Figure 2–21. Single-Port Mode *Note (1)*



Note to Figure 2–21:

(1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Global Clock Network and Phase-Locked Loops

Cyclone devices provide a global clock network and up to two PLLs for a complete clock management solution.

Global Clock Network

There are four dedicated clock pins (`CLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network, as shown in Figure 2–22. PLL outputs, logic array, and dual-purpose clock (`DPCLK[7..0]`) pins can also drive the global clock network.

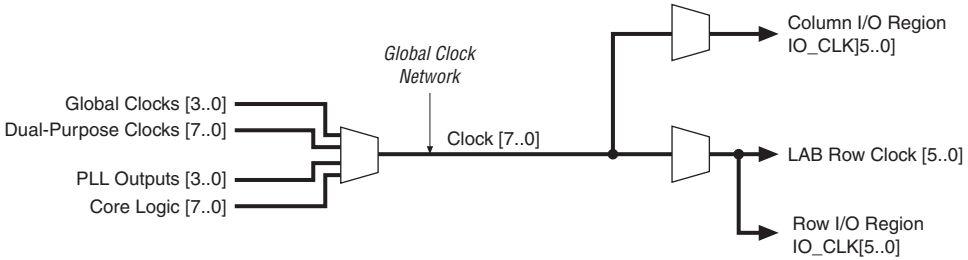
Dual-Purpose Clock Pins

Each Cyclone device except the EP1C3 device has eight dual-purpose clock pins, DPCLK[7..0] (two on each I/O bank). EP1C3 devices have five DPCLK pins in the 100-pin TQFP package. These dual-purpose pins can connect to the global clock network (see Figure 2–22) for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables, or protocol control signals such as TRDY and IRDY for PCI, or DQS signals for external memory interfaces.

Combined Resources

Each Cyclone device contains eight distinct dedicated clocking resources. The device uses multiplexers with these clocks to form six-bit buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. See Figure 2–23. Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

Figure 2–23. Global Clock Network Multiplexers



IOE clocks have row and column block regions. Six of the eight global clock resources feed to these row and column regions. Figure 2–24 shows the I/O clock regions.

Table 2–7. Global Clock Network Sources (Part 2 of 2)

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
Dual-Purpose Clock Pins	DPCLK0 *(3)*	—	—	—	✓	—	—	—	—
	DPCLK1 *(3)*	—	—	✓	—	—	—	—	—
	DPCLK2	✓	—	—	—	—	—	—	—
	DPCLK3	—	—	—	—	✓	—	—	—
	DPCLK4	—	—	—	—	—	—	✓	—
	DPCLK5 *(3)*	—	—	—	—	—	—	—	✓
	DPCLK6	—	—	—	—	—	✓	—	—
	DPCLK7	—	✓	—	—	—	—	—	—

Notes to Table 2–7:
(1) EP1C3 devices only have one PLL (PLL 1).
(2) EP1C3 devices in the 100-pin TQFP package do not have dedicated clock pins `CLK1` and `CLK3`.
(3) EP1C3 devices in the 100-pin TQFP package do not have the `DPCLK0`, `DPCLK1`, or `DPCLK5` pins.

Clock Multiplication and Division

Cyclone PLLs provide clock synthesis for PLL output ports using $m/(n \times$ post scale counter) scaling factors. The input clock is divided by a pre-scale divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter to divide down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least-common multiple in the VCO's range).

Each PLL has one pre-scale divider, n, that can range in value from 1 to 32. Each PLL also has one multiply divider, m, that can range in value from 2 to 32. Global clock outputs have two post scale G dividers for global clock outputs, and external clock outputs have an E divider for external clock output, both ranging from 1 to 32. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

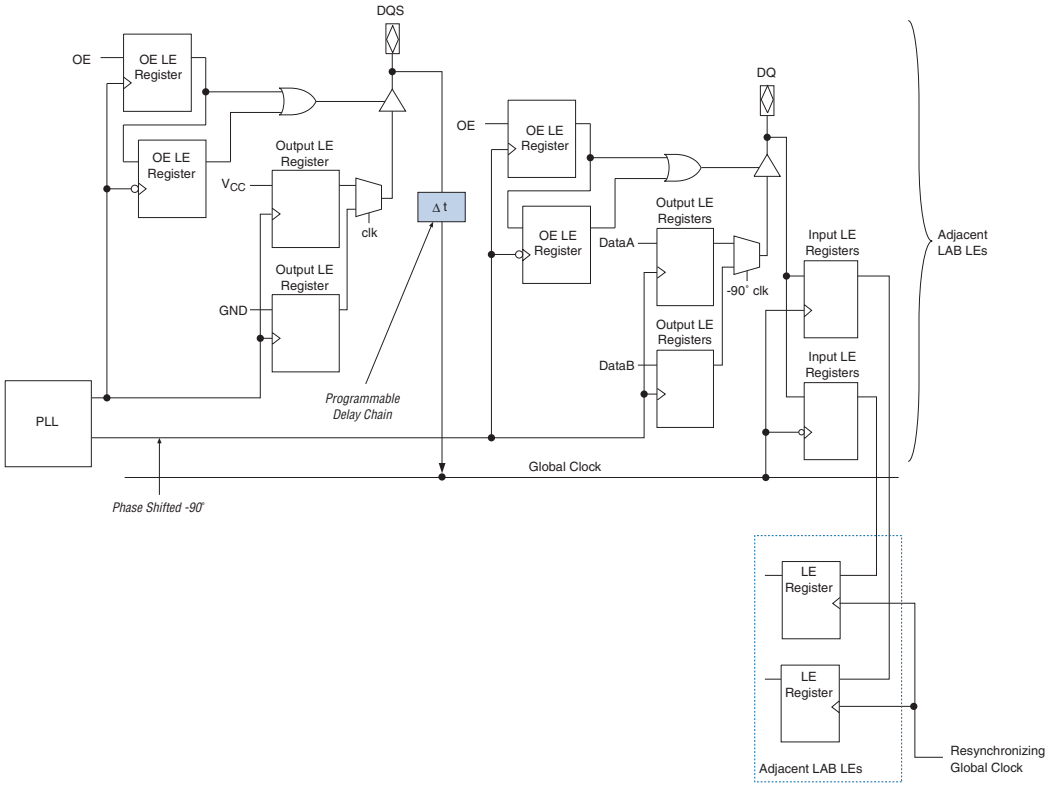
I/O Structure

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

Cyclone device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–27 shows the Cyclone IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. IOEs can be used as input, output, or bidirectional pins.

Figure 2–34. DDR SDRAM and FCRAM Interfacing



Programmable Drive Strength

The output buffer for each Cyclone device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standards have several levels of drive strength that the designer can control. SSTL-3 class I and II, and SSTL-2 class I and II support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL}

of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 2–11 shows the possible settings for the I/O standards with drive strength control.

Table 2–11. Programmable Drive Strength *Note (1)*

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
LVTTL (3.3 V)	4
	8
	12
	16
	24 *(2)*
LVCMOS (3.3 V)	2
	4
	8
	12 *(2)*
LVTTL (2.5 V)	2
	8
	12
	16 *(2)*
LVTTL (1.8 V)	2
	8
	12 *(2)*
LVCMOS (1.5 V)	2
	4
	8 *(2)*

Notes to Table 2–11:

(1) SSTL-3 class I and II, SSTL-2 class I and II, and 3.3-V PCI I/O Standards do not support programmable drive strength.

(2) This is the default current strength setting in the Quartus II software.

Open-Drain Output

Cyclone devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Multiple Cyclone devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 3–5. Data Sources for Configuration

Configuration Scheme	Data Source
Active serial	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster or ByteBlasterMV download cable, or serial data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file

Referenced Documents

This chapter references the following document:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

Document Revision History

Table 3–6 shows the revision history for this chapter.

Table 3–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added "Referenced Documents" section.	—
January 2007 v1.3	• Added document revision history. • Updated handpara note below Table 3–4.	—
August 2005 V1.2	Minor updates.	—
February 2005 V1.1	Updated JTAG chain limits. Added information concerning test vectors.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA	—	0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1	—	V
		I_{OH} = –1 mA	2.0	—	V
		I_{OH} = –2 to –16 mA *(11)*	1.7	—	V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	—	0.2	V
		I_{OH} = 1 mA	—	0.4	V
		I_{OH} = 2 to 16 mA *(11)*	—	0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.65	1.95	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(12)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(11)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(11)*	—	0.45	V

Table 4–13. SSTL-3 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{REF}	Reference voltage	—	1.3	1.5	1.7	V
V_{IH}	High-level input voltage	—	V_{REF} + 0.2	—	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(11)*	V_{TT} + 0.6	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(11)*	—	—	V_{TT} – 0.6	V

Table 4–14. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{TT}	Termination voltage	—	V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage	—	1.3	1.5	1.7	V
V_{IH}	High-level input voltage	—	V_{REF} + 0.2	—	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(11)*	V_{TT} + 0.8	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(11)*	—	—	V_{TT} – 0.8	V

Table 4–15. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	—	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	—	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}	—	—	—	200	—	300	—	500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}	—	—	—	–200	—	–300	—	–500	µA

Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in Table 4–19.

Table 4–19. Clock Tree Maximum Performance Specification

Parameter	Definition	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock tree f_{MAX}	Maximum frequency that the clock tree can support for clocking registered logic	—	—	405	—	—	320	—	—	275	MHz

Table 4–20 shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
LE	16-to-1 multiplexer	—	21	—	—	405.00	320.00	275.00
	32-to-1 multiplexer	—	44	—	—	317.36	284.98	260.15
	16-bit counter	—	16	—	—	405.00	320.00	275.00
	64-bit counter *(1)*	—	66	—	—	208.99	181.98	160.75

Table 4–22. IOE Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{SU}	IOE input and output register setup time before clock
t_{H}	IOE input and output register hold time after clock
t_{CO}	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–23. M4K Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width

Tables 4–32 through 4–33 show the external timing parameters on column and row pins for EP1C4 devices.

Table 4–32. EP1C4 Column Pin Global Clock External I/O Timing Parameters *Note (1)*

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.471	—	2.841	—	3.210	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.937	2.000	4.526	2.000	5.119	ns
$t_{INSUPLL}$	1.471	—	1.690	—	1.910	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	2.080	0.500	2.392	0.500	2.705	ns

Table 4–33. EP1C4 Row Pin Global Clock External I/O Timing Parameters *Note (1)*

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.600	—	2.990	—	3.379	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.991	2.000	4.388	2.000	5.189	ns
$t_{INSUPLL}$	1.300	—	1.494	—	1.689	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	2.234	0.500	2.569	0.500	2.905	ns

Note to Tables 4–32 and 4–33:
(1) Contact Altera Applications for EP1C4 device timing parameters.

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class II		–278	—	–320	—	–362	ps
LVDS		–261	—	–301	—	–340	ps

Table 4–41. Cyclone I/O Standard Row Pin Input Delay Adders

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS	—	0	—	0	—	0	ps
3.3-V LVTTL	—	0	—	0	—	0	ps
2.5-V LVTTL	—	27	—	31	—	35	ps
1.8-V LVTTL	—	182	—	209	—	236	ps
1.5-V LVTTL	—	278	—	319	—	361	ps
3.3-V PCI *(1)*	—	0	—	0	—	0	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps
SSTL-2 class II	—	–278	—	–320	—	–362	ps
LVDS	—	–261	—	–301	—	–340	ps

Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps

Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.8-V LVTTL	2 mA	—	1,290	—	1,483	—	1,677	ps
	8 mA	—	4	—	4	—	5	ps
	12 mA	—	–208	—	–240	—	–271	ps
1.5-V LVTTL	2 mA	—	2,288	—	2,631	—	2,974	ps
	4 mA	—	608	—	699	—	790	ps
	8 mA	—	292	—	335	—	379	ps
3.3-V PCI *(1)*		—	–877	—	–1,009	—	–1,141	ps
SSTL-3 class I		—	–410	—	–472	—	–533	ps
SSTL-3 class II		—	–811	—	–933	—	–1,055	ps
SSTL-2 class I		—	–485	—	–558	—	–631	ps
SSTL-2 class II		—	–758	—	–872	—	–986	ps
LVDS		—	–998	—	–1,148	—	–1,298	ps

Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	1,800	—	2,070	—	2,340	ps
	4 mA	—	1,311	—	1,507	—	1,704	ps
	8 mA	—	945	—	1,086	—	1,228	ps
	12 mA	—	807	—	928	—	1,049	ps
3.3-V LVTTL	4 mA	—	1,831	—	2,105	—	2,380	ps
	8 mA	—	1,484	—	1,705	—	1,928	ps
	12 mA	—	973	—	1,118	—	1,264	ps
	16 mA	—	1,012	—	1,163	—	1,315	ps
	24 mA	—	838	—	963	—	1,089	ps
2.5-V LVTTL	2 mA	—	2,747	—	3,158	—	3,570	ps
	8 mA	—	1,757	—	2,019	—	2,283	ps
	12 mA	—	1,763	—	2,026	—	2,291	ps
	16 mA	—	1,623	—	1,865	—	2,109	ps
1.8-V LVTTL	2 mA	—	5,506	—	6,331	—	7,157	ps
	8 mA	—	4,220	—	4,852	—	5,485	ps
	12 mA	—	4,008	—	4,608	—	5,209	ps

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-3 class I	—	1,390	—	1,598	—	1,807	ps
SSTL-3 class II	—	989	—	1,137	—	1,285	ps
SSTL-2 class I	—	1,965	—	2,259	—	2,554	ps
SSTL-2 class II	—	1,692	—	1,945	—	2,199	ps
LVDS	—	802	—	922	—	1,042	ps

Note to Tables 4–40 through 4–45:
(1) EP1C3 devices do not support the PCI I/O standard.

Tables 4–46 through 4–47 show the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

Table 4–46. Cyclone IOE Programmable Delays on Column Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	155	—	178	—	201	ps
	Small	—	2,122	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	155	—	178	—	201	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	552	—	634	—	717	ps

5. Reference and Ordering Information

C51005-1.4

Software

Cyclone® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analysis, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Cyclone devices are available on the Altera website (www.altera.com) and in the *Cyclone Device Handbook*.

Ordering Information

Figure 5–1 describes the ordering codes for Cyclone devices. For more information about a specific package, refer to the *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*.

February 2005 v1.1	Updated Figure 5-1.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—