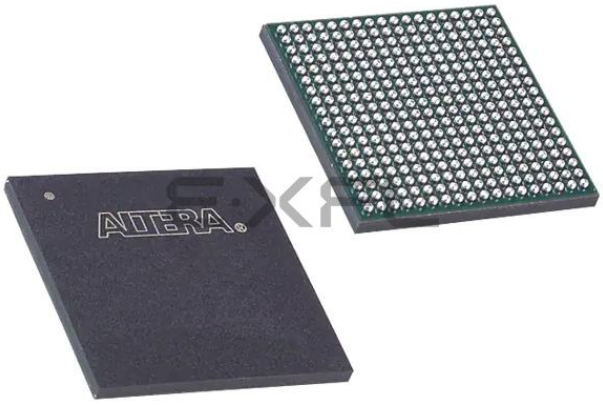


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	249
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c12f324c6

Table 1–1. Cyclone Device Features (Part 2 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Total RAM bits	59,904	78,336	92,160	239,616	294,912
PLLs	1	2	2	2	2
Maximum user I/O pins *(1)*	104	301	185	249	301

Note to Table 1–1:
(1) This parameter includes global clock pins.

Cyclone devices are available in quad flat pack (QFP) and space-saving FineLine® BGA packages (see Tables 1–2 through 1–3).

Table 1–2. Cyclone Package Options and I/O Pin Counts

Device	100-Pin TQFP *(1)*	144-Pin TQFP *(1), (2)*	240-Pin PQFP *(1)*	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
EP1C3	65	104	—	—	—	—
EP1C4	—	—	—	—	249	301
EP1C6	—	98	185	185	—	—
EP1C12	—	—	173	185	249	—
EP1C20	—	—	—	—	233	301

Notes to Table 1–2:
(1) TQFP: thin quad flat pack.
PQFP: plastic quad flat pack.
(2) Cyclone devices support vertical migration within the same package (i.e., designers can migrate between the EP1C3 device in the 144-pin TQFP package and the EP1C6 device in the same package).

Vertical migration means you can migrate a design from one device to another that has the same dedicated pins, JTAG pins, and power pins, and are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must use the layout for the largest planned density in a package to provide the necessary power pins for migration.

For I/O pin migration across densities, cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list. If one device has power or ground pins, but these same pins are user I/O on a different device that is in the migration path,the Quartus II software ensures the pins are not used as user I/O in the Quartus II software. Ensure that these pins are connected

to the appropriate plane on the board. The Quartus II software reserves I/O pins as power pins as necessary for layout with the larger densities in the same package having more power pins.

Table 1–3. Cyclone QFP and FineLine BGA Package Sizes

Dimension	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0.5	0.5	0.5	1.0	1.0	1.0
Area (mm^2)	256	484	1,024	289	361	441
Length × width (mm × mm)	16×16	22×22	34.6×34.6	17×17	19×19	21×21

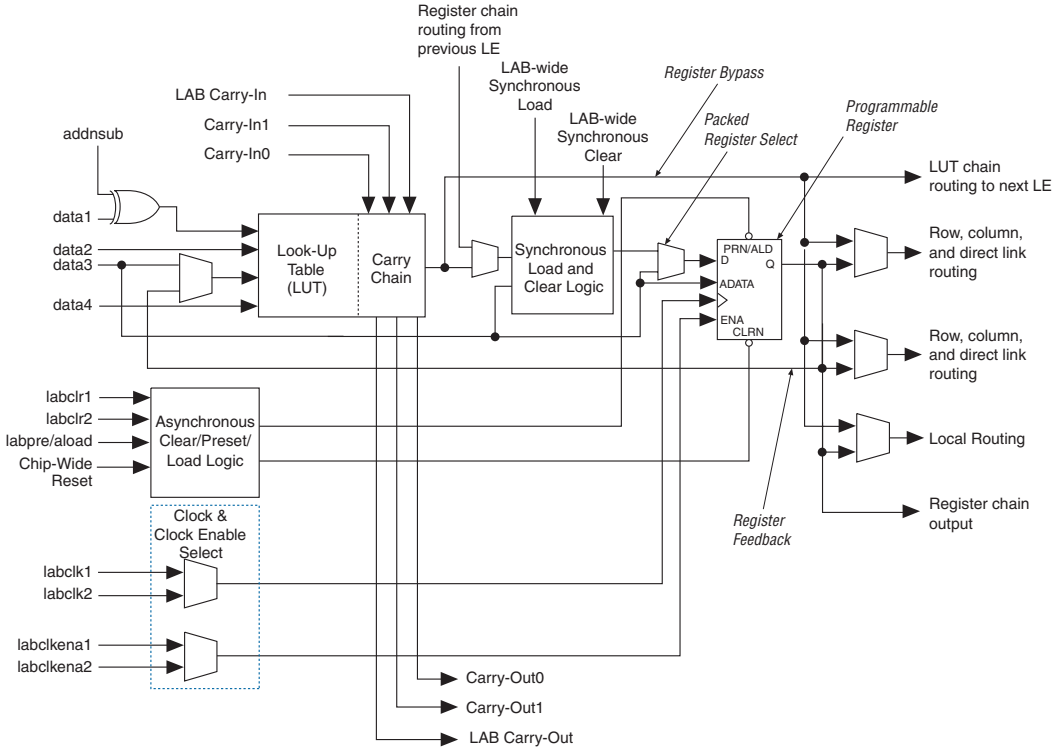
Document Revision History

Table 1–4 shows the revision history for this document.

Table 1–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.5	Minor textual and style changes.	—
January 2007 v1.4	Added document revision history.	—
August 2005 v1.3	Minor updates.	—
October 2003 v1.2	Added 64-bit PCI support information.	—
September 2003 v1.1	• Updated LVDS data rates to 640 Mbps from 311 Mbps. • Updated RSDS feature information.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Figure 2–5. Cyclone LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated

is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

Table 2–4. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Byte Enables

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2–5 summarizes the byte selection.

Table 2–5. Byte Enable for M4K Blocks *Notes (1), (2)*

byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	—	[26..18]
[3] = 1	—	[35..27]

Notes to Table 2–5:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

Control Signals and M4K Interface

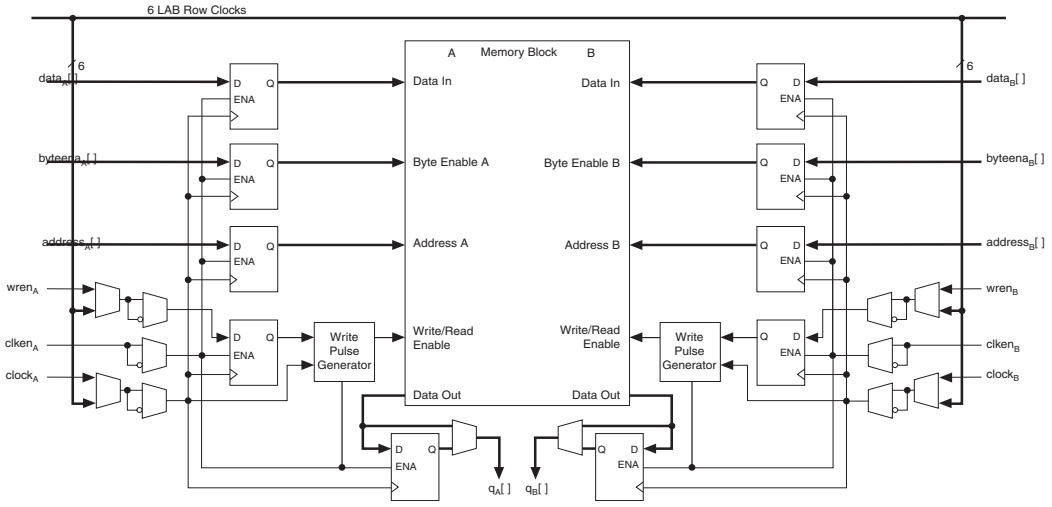
The M4K blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–15.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2–16 shows the M4K block to logic array interface.

Independent Clock Mode

The M4K memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–17 shows an M4K memory block in independent clock mode.

Figure 2–17. Independent Clock Mode *Notes (1), (2)*



Notes to Figure 2–17:

(1) All registers shown have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–18 and 2–19 show the memory block in input/output clock mode.

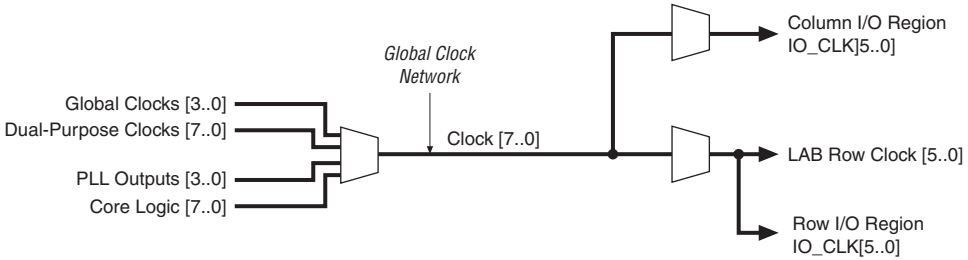
Dual-Purpose Clock Pins

Each Cyclone device except the EP1C3 device has eight dual-purpose clock pins, DPCLK[7..0] (two on each I/O bank). EP1C3 devices have five DPCLK pins in the 100-pin TQFP package. These dual-purpose pins can connect to the global clock network (see Figure 2–22) for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables, or protocol control signals such as TRDY and IRDY for PCI, or DQS signals for external memory interfaces.

Combined Resources

Each Cyclone device contains eight distinct dedicated clocking resources. The device uses multiplexers with these clocks to form six-bit buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. See Figure 2–23. Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

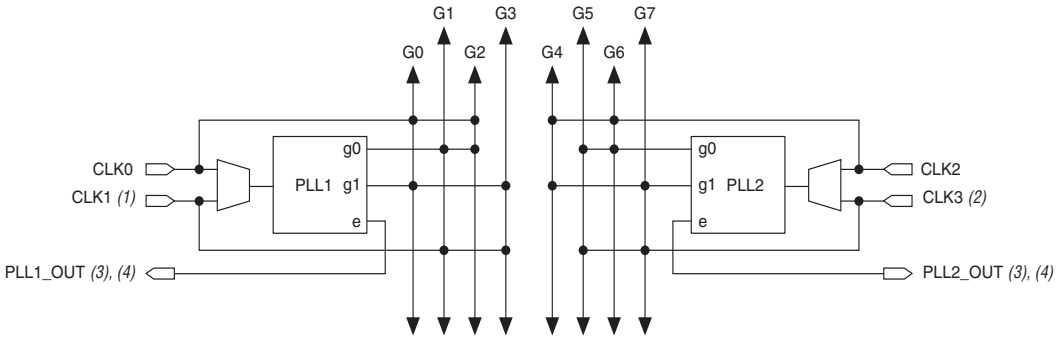
Figure 2–23. Global Clock Network Multiplexers



IOE clocks have row and column block regions. Six of the eight global clock resources feed to these row and column regions. Figure 2–24 shows the I/O clock regions.

Figure 2–26 shows the PLL global clock connections.

Figure 2–26. Cyclone PLL Global Clock Connections



Notes to Figure 2–26:

(1) PLL 1 supports one single-ended or LVDS input via pins CLK0 and CLK1.

(2) PLL2 supports one single-ended or LVDS input via pins CLK2 and CLK3.

(3) PLL1_OUT and PLL2_OUT support single-ended or LVDS output. If external output is not required, these pins are available as regular user I/O pins.

(4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Table 2–7 shows the global clock network sources available in Cyclone devices.

Table 2–7. Global Clock Network Sources (Part 1 of 2)

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
PLL Counter Output	PLL1 G0	—	✓	✓	—	—	—	—	—
	PLL1 G1	✓	—	—	✓	—	—	—	—
	PLL2 G0 *(1)*	—	—	—	—	—	✓	✓	—
	PLL2 G1 *(1)*	—	—	—	—	✓	—	—	✓
Dedicated Clock Input Pins	CLK0	✓	—	✓	—	—	—	—	—
	CLK1 *(2)*	—	✓	—	✓	—	—	—	—
	CLK2	—	—	—	—	✓	—	✓	—
	CLK3 *(2)*	—	—	—	—	—	✓	—	✓

External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (CLK[3..0]) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See Figure 2–25.

Table 2–8 shows the I/O standards supported by PLL input and output pins.

Table 2–8. PLL I/O Standards

I/O Standard	CLK Input	EXTCLK Output
3.3-V LVTTL/LVCMOS	✓	✓
2.5-V LVTTL/LVCMOS	✓	✓
1.8-V LVTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

For more information on LVDS I/O support, refer to "LVDS I/O Pins" on page 2–54.

External Clock Outputs

Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these PLL_OUT pins, the pins are available for use as general-purpose I/O pins. The PLL_OUT pins support all I/O standards shown in Table 2–8.

The external clock outputs do not have their own V_{CC} and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

I/O Structure

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

Cyclone device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–27 shows the Cyclone IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. IOEs can be used as input, output, or bidirectional pins.

Slew-Rate Control

The output buffer for each Cyclone device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Bus Hold

Each Cyclone device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 kΩ to pull the signal level to the last-driven state. Table 4–15 on page 4–6 gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Cyclone device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) holds the output to the V_{CCIO} level of the output pin's bank. Dedicated clock pins do not have the optional programmable pull-up resistor.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

Table 2–13. Cyclone Device LVDS Channels

Device	Pin Count	Number of LVDS Channels
EP1C3	100	*(1)*
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

Note to Table 2–13:

(1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and four sets for I/O output drivers (V_{CCIO}).

The Cyclone V_{CCINT} pins must always be connected to a 1.5-V power supply. If the V_{CCINT} level is 1.5 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The V_{CCIO} pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when V_{CCIO} pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V or 5.0-V systems. Table 2–14 summarizes Cyclone MultiVolt I/O support.

Table 2–14. Cyclone MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ (2)	✓ (2)	—	✓	—	—	—	—
1.8	✓	✓	✓ (2)	✓ (2)	—	✓ (3)	✓	—	—	—
2.5	—	—	✓	✓	—	✓ (5)	✓ (5)	✓	—	—
3.3	—	—	✓ (4)	✓	✓ (6)	✓ (7)	✓ (7)	✓ (7)	✓	✓ (8)

Notes to Table 2–14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2) When V_{CCIO} = 1.5-V or 1.8-V and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected. Turn on **Allow voltage overdrive for LVTTL / LVCMOS input pins** in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combinations.
(3) When V_{CCIO} = 1.8-V, a Cyclone device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected.
(5) When V_{CCIO} = 2.5-V, a Cyclone device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(6) Cyclone devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.
(7) When V_{CCIO} = 3.3-V, a Cyclone device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
(8) When V_{CCIO} = 3.3-V, a Cyclone device can drive a device with 5.0-V LVTTL inputs but not 5.0-V LVCMOS inputs.

Power Sequencing and Hot Socketing

Because Cyclone devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into Cyclone devices before and during power up without damaging the device. In addition, Cyclone devices do not drive out during power up. Once operating conditions are reached and the device is configured, Cyclone devices operate as specified by the user.

Operating Modes

The Cyclone architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Cyclone devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the V_{CCIO} of the bank where the pins reside. The bank V_{CCIO} selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Configuration Schemes

Designers can load the configuration data for a Cyclone device with one of three configuration schemes (see Table 3–5), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone device. A low-cost configuration device can automatically configure a Cyclone device at system power-up.

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA	—	0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1	—	V
		I_{OH} = –1 mA	2.0	—	V
		I_{OH} = –2 to –16 mA *(11)*	1.7	—	V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	—	0.2	V
		I_{OH} = 1 mA	—	0.4	V
		I_{OH} = 2 to 16 mA *(11)*	—	0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.65	1.95	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(12)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(11)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(11)*	—	0.45	V

Table 4–27. M4K Block Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{M4KRC}	—	4,379		5,035		5,691	ps
t_{M4KWC}	—	2,910		3,346		3,783	ps
$t_{M4KWERESU}$	72	—	82	—	93	—	ps
$t_{M4KWEREH}$	43	—	49	—	55	—	ps
$t_{M4KBESU}$	72	—	82	—	93	—	ps
t_{M4KBEH}	43	—	49	—	55	—	ps
$t_{M4KDATAASU}$	72	—	82	—	93	—	ps
$t_{M4KDATAAH}$	43	—	49	—	55	—	ps
$t_{M4KADDRASU}$	72	—	82	—	93	—	ps
$t_{M4KADDRAH}$	43	—	49	—	55	—	ps
$t_{M4KDATABSU}$	72	—	82	—	93	—	ps
$t_{M4KDATABH}$	43	—	49	—	55	—	ps
$t_{M4KADDRBSU}$	72	—	82	—	93	—	ps
$t_{M4KADDRBH}$	43	—	49	—	55	—	ps
$t_{M4KDATACO1}$	—	621	—	714	—	807	ps
$t_{M4KDATACO2}$	—	4,351	—	5,003	—	5,656	ps
$t_{M4KCLKHL}$	1,234	—	1,562	—	1,818	—	ps
t_{M4KCLR}	286	—	328	—	371	—	ps

Table 4–28. Routing Delay Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{R4}	—	261	—	300	—	339	ps
t_{C4}	—	338	—	388	—	439	ps
t_{LOCAL}	—	244	—	281	—	318	ps

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–2 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Table 4–49. Cyclone Maximum Input Clock Rate for Row Pins				
I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVCMOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
3.3-V PCI *(1)*	464	428	387	MHz
LVDS	567	549	531	MHz

Note to Tables 4–48 through 4–49:
(1) EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

Tables 4–50 and 4–51 show the maximum output clock rate for column and row pins in Cyclone devices.

Table 4–50. Cyclone Maximum Output Clock Rate for Column Pins				
I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	304	304	304	MHz
2.5 V	220	220	220	MHz
1.8 V	213	213	213	MHz
1.5 V	166	166	166	MHz
LVCMOS	304	304	304	MHz
SSTL-3 class I	100	100	100	MHz
SSTL-3 class II	100	100	100	MHz
SSTL-2 class I	134	134	134	MHz
SSTL-2 class II	134	134	134	MHz
LVDS	320	320	275	MHz

Note to Table 4–50:
(1) EP1C3 devices do not support the PCI I/O standard.

Referenced Document

This chapter references the following documents:

- *Cyclone Architecture* chapter in the *Cyclone Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*

Document Revision History

Table 4–53 shows the revision history for this chapter.

Table 4–53. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.7	Minor textual and style changes. Added "Referenced Document" section.	—
January 2007 v1.6	• Added document revision history. • Added new row for V_{CCA} details in Table 4–1. • Updated R_{CONF} information in Table 4–3. • Added new *Note (12)* on voltage overdrive information to Table 4–7 and Table 4–8. • Updated *Note (9)* on R_{CONF} information to Table 4–3. • Updated information in "External I/O Delay Parameters" section. • Updated speed grade information in Table 4–46 and Table 4–47. • Updated LVDS information in Table 4–51.	—
August 2005 v1.5	Minor updates.	—
February 2005 v1.4	• Updated information on Undershoot voltage. Updated Table 4-2. • Updated Table 4-3. • Updated the undershoot voltage from 0.5 V to 2.0 V in Note 3 of Table 4-16. • Updated Table 4-17.	—
January 2004 v.1.3	• Added extended-temperature grade device information. Updated Table 4-2. • Updated I_{CC0} information in Table 4-3.	—
October 2003 v.1.2	• Added clock tree information in Table 4-19. • Finalized timing information for EP1C3 and EP1C12 devices. Updated timing information in Tables 4-25 through 4-26 and Tables 4-30 through 4-51. • Updated PLL specifications in Table 4-52.	—

July 2003 v1.1	Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—