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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	249
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c12f324c6n">https://www.e-xfl.com/product-detail/intel/ep1c12f324c6n</a>

to the appropriate plane on the board. The Quartus II software reserves I/O pins as power pins as necessary for layout with the larger densities in the same package having more power pins.

**Table 1–3. Cyclone QFP and FineLine BGA Package Sizes**

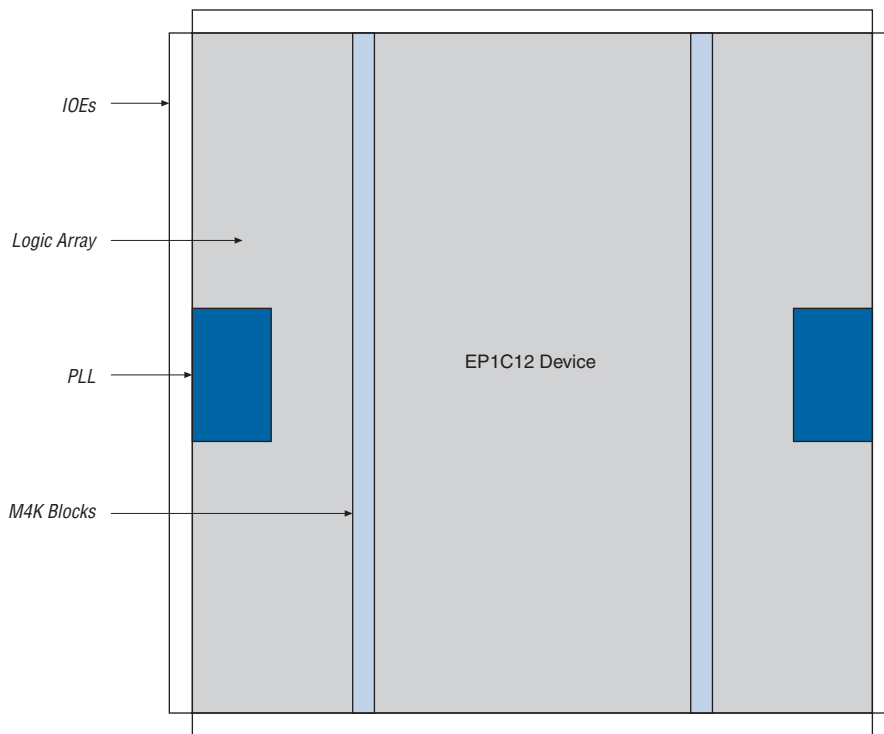
Dimension	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0.5	0.5	0.5	1.0	1.0	1.0
Area (mm <sup>2</sup> )	256	484	1,024	289	361	441
Length × width (mm × mm)	16×16	22×22	34.6×34.6	17×17	19×19	21×21

## Document Revision History

Table 1–4 shows the revision history for this document.

**Table 1–4. Document Revision History**

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.5	Minor textual and style changes.	—
January 2007 v1.4	Added document revision history.	—
August 2005 v1.3	Minor updates.	—
October 2003 v1.2	Added 64-bit PCI support information.	—
September 2003 v1.1	<ul style="list-style-type: none"> <li>Updated LVDS data rates to 640 Mbps from 311 Mbps.</li> <li>Updated RSDS feature information.</li> </ul>	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

**Figure 2–1. Cyclone EP1C12 Device Block Diagram**

The number of M4K RAM blocks, PLLs, rows, and columns vary per device. [Table 2–1](#) lists the resources available in each Cyclone device.

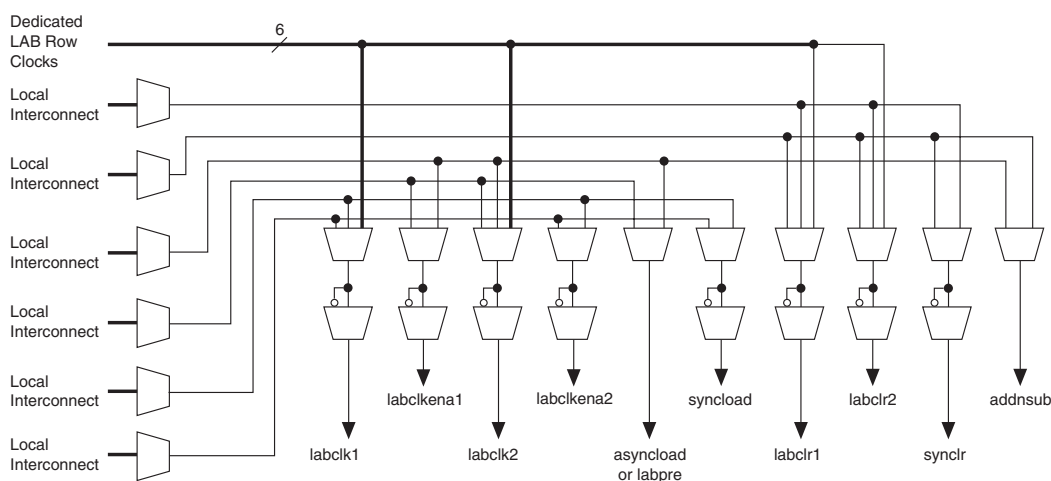
**Table 2–1. Cyclone Device Resources**

Device	M4K RAM		PLLs	LAB Columns	LAB Rows
	Columns	Blocks			
EP1C3	1	13	1	24	13
EP1C4	1	17	2	26	17
EP1C6	1	20	2	32	20
EP1C12	2	52	2	48	26
EP1C20	2	64	2	64	32

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [5 : 0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. [Figure 2-4](#) shows the LAB control signal generation circuit.

**Figure 2-4. LAB-Wide Control Signals**



## Logic Elements

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See [Figure 2-5](#).

### *Dynamic Arithmetic Mode*

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in [Figure 2-7](#), the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

$$\text{data1} + \text{data2} + \text{carry-in0}$$

or

$$\text{data1} + \text{data2} + \text{carry-in1}$$

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

## Embedded Memory

The Cyclone embedded memory consists of columns of M4K memory blocks. EP1C3 and EP1C6 devices have one column of M4K blocks, while EP1C12 and EP1C20 devices have two columns (refer to [Table 1–1 on page 1–1](#) for total RAM bits per density). Each M4K block can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. The M4K blocks support the following features:

- 4,608 RAM bits
- 250 MHz performance
- True dual-port memory
- Simple dual-port memory
- Single-port memory
- Byte enable
- Parity bits
- Shift register
- FIFO buffer
- ROM
- Mixed clock mode

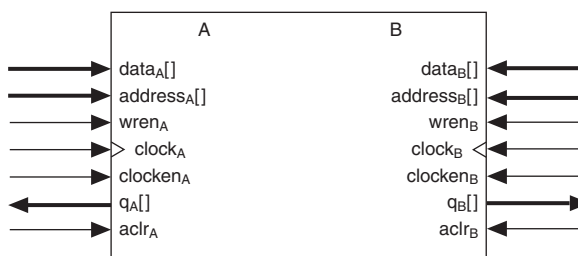


Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

### Memory Modes

The M4K memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. [Figure 2–12](#) shows true dual-port memory.

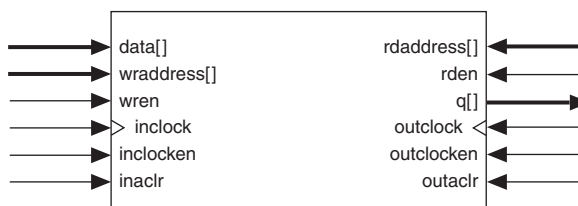
**Figure 2–12. True Dual-Port Memory Configuration**



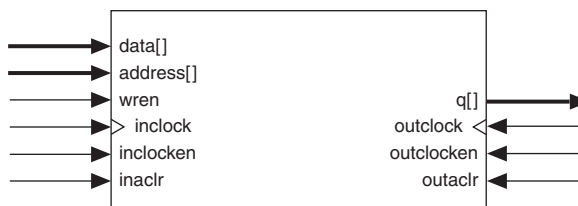
In addition to true dual-port memory, the M4K memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write. Single-port memory supports non-simultaneous reads and writes. Figure 2–13 shows these different M4K RAM memory port configurations.

**Figure 2–13. Simple Dual-Port and Single-Port Memory Configurations**

**Simple Dual-Port Memory**



**Single-Port Memory (1)**



**Note to Figure 2–13:**

- (1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in  $\times 1$  mode at port A and read out in  $\times 16$  mode from port B.

The Cyclone memory architecture can implement fully synchronous RAM by registering both the input and output signals to the M4K RAM block. All M4K memory block inputs are registered, providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`wren`) signal derived from a global clock. In contrast, a circuit using asynchronous RAM must generate the RAM `wren` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `wren`

signal. The output registers can be bypassed. Pseudo-asynchronous reading is possible in the simple dual-port mode of M4K blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple M4K memory blocks. For example, two 256×16-bit RAM blocks can be combined to form a 256×32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words allowed. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

## Parity Bit Support

The M4K blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. Byte enables are also available for data input masking during write operations.

## Shift Register Support

You can configure M4K memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a  $w \times m \times n$  shift register is determined by the input data width ( $w$ ), the length of the taps ( $m$ ), and the number of taps ( $n$ ). The size of a  $w \times m \times n$  shift register must be less than or equal to the maximum number of memory bits in the M4K block (4,608 bits). The total number of shift



## Byte Enables

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. [Table 2-5](#) summarizes the byte selection.

<b>Table 2-5. Byte Enable for M4K Blocks</b> <i>Notes (1), (2)</i>		
<b>byteena[3..0]</b>	<b>datain ×18</b>	<b>datain ×36</b>
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	—	[26..18]
[3] = 1	—	[35..27]

**Notes to [Table 2-5](#):**

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

## Control Signals and M4K Interface

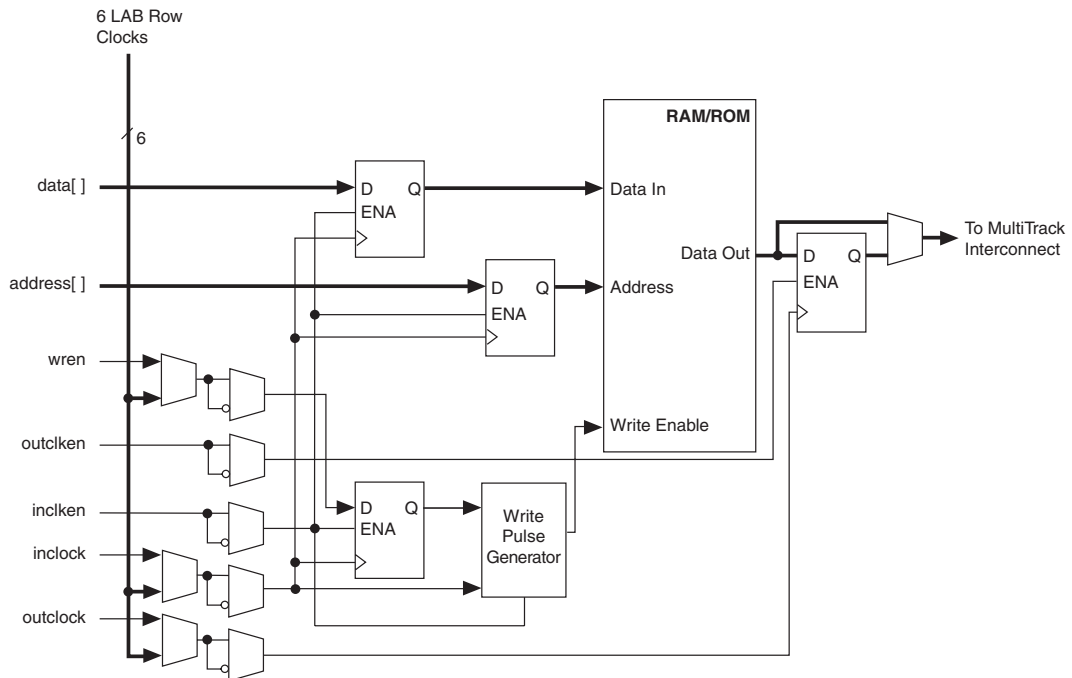
The M4K blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K block registers (*renwe*, *address*, *byte enable*, *datain*, and output registers). Only the output register can be bypassed. The six *labclk* signals or local interconnects can drive the control signals for the A and B ports of the M4K block. LEs can also control the *clock\_a*, *clock\_b*, *renwe\_a*, *renwe\_b*, *clr\_a*, *clr\_b*, *clocken\_a*, and *clocken\_b* signals, as shown in [Figure 2-15](#).

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through 10 direct link interconnects each. [Figure 2-16](#) shows the M4K block to logic array interface.

## Single-Port Mode

The M4K memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–21. A single M4K memory block can support up to two single-port mode RAM blocks if each RAM block is less than or equal to 2K bits in size.

**Figure 2–21. Single-Port Mode** *Note (1)*



**Note to Figure 2–21:**

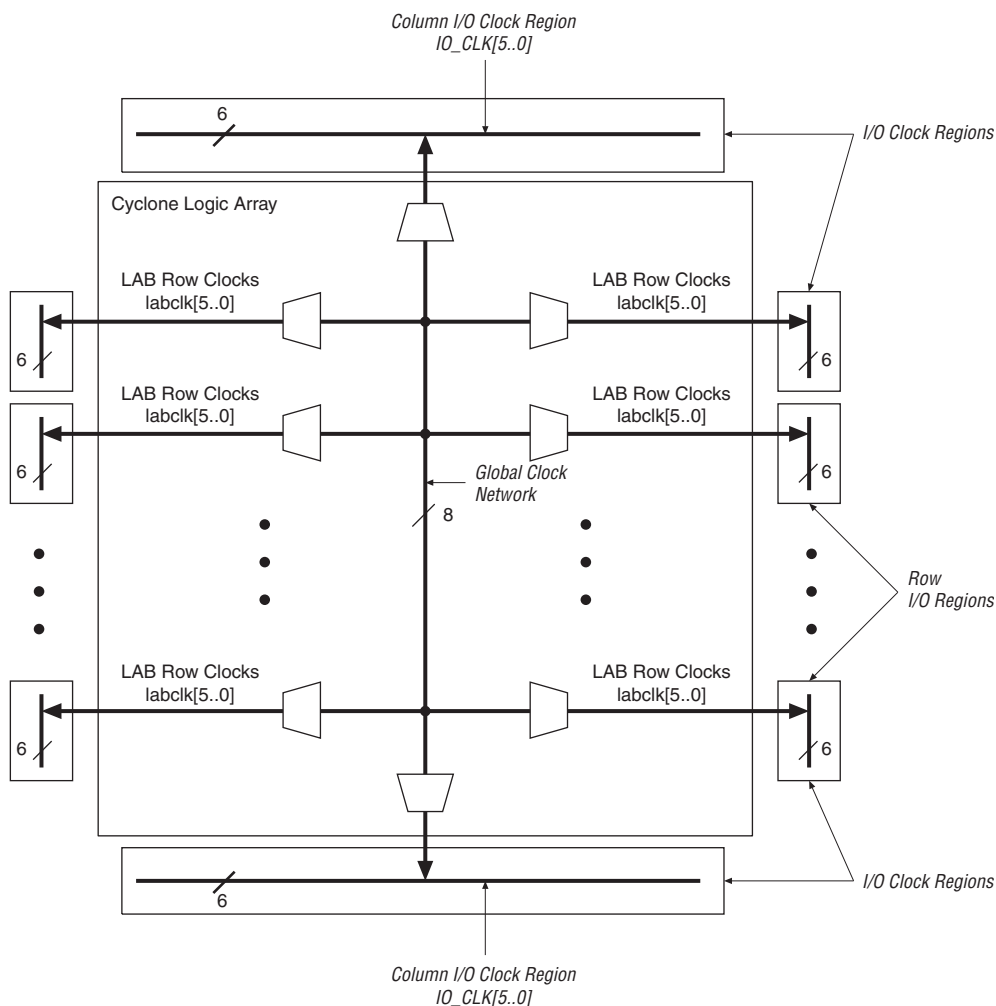
- (1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

## Global Clock Network and Phase-Locked Loops

Cyclone devices provide a global clock network and up to two PLLs for a complete clock management solution.

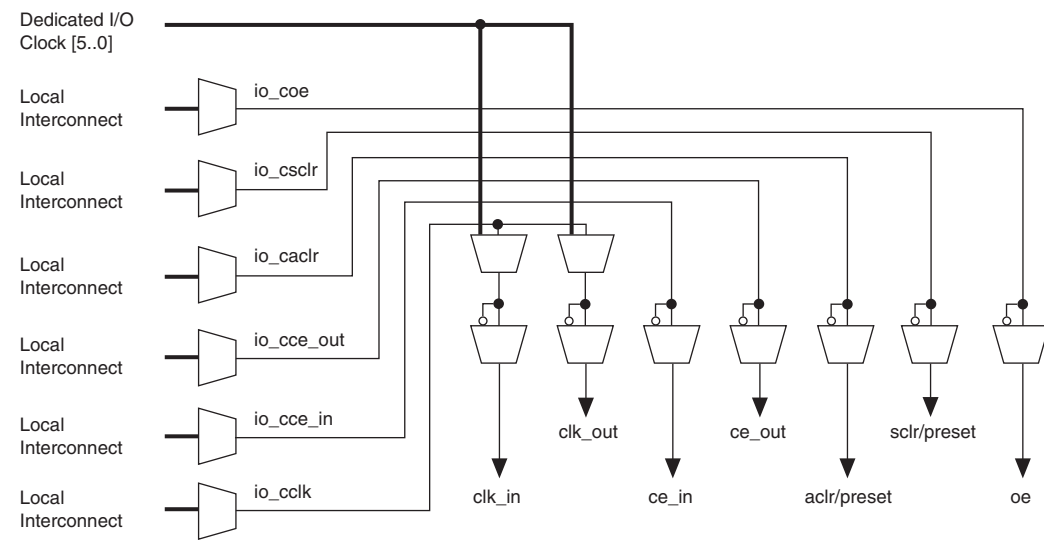
### Global Clock Network

There are four dedicated clock pins (CLK[3..0]), two pins on the left side and two pins on the right side) that drive the global clock network, as shown in Figure 2–22. PLL outputs, logic array, and dual-purpose clock (DPCLK[7..0]) pins can also drive the global clock network.

**Figure 2–24. I/O Clock Regions**

## PLLs

Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as outputs for differential I/O support. Cyclone devices contain two PLLs, except for the EP1C3 device, which contains one PLL.

**Figure 2–31. Control Signal Selection per IOE**

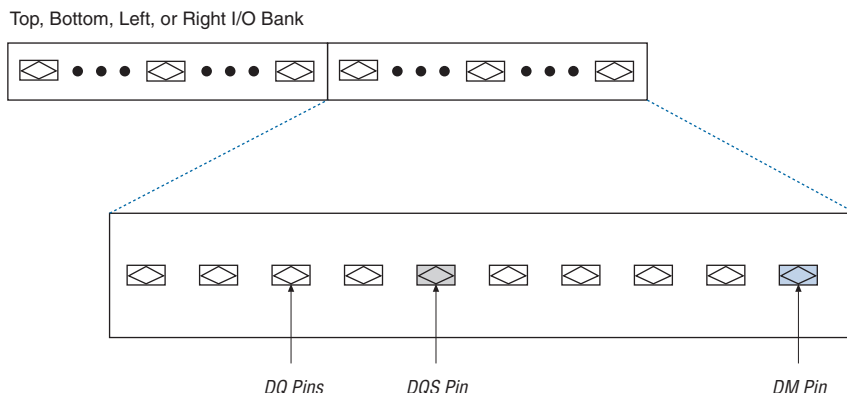
In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register is available for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from the local interconnect in the associated LAB, dedicated I/O clocks, or the column and row interconnects.

Figure 2–32 shows the IOE in bidirectional configuration.

output pins (`nSTATUS` and `CONF_DONE`) and all the JTAG pins in I/O bank 3 must operate at 2.5 V because the  $V_{CCIO}$  level of SSTL-2 is 2.5 V. I/O banks 1, 2, 3, and 4 support DQS signals with DQ bus modes of  $\times 8$ .

For  $\times 8$  mode, there are up to eight groups of programmable DQS and DQ pins, I/O banks 1, 2, 3, and 4 each have two groups in the 324-pin and 400-pin FineLine BGA packages. Each group consists of one DQS pin, a set of eight DQ pins, and one DM pin (see Figure 2–33). Each DQS pin drives the set of eight DQ pins within that group.

**Figure 2–33. Cyclone Device DQ and DQS Groups in  $\times 8$  Mode** *Note (1)*



**Note to Figure 2–33:**

- (1) Each DQ group consists of one DQS pin, eight DQ pins, and one DM pin.

Table 2–10 shows the number of DQ pin groups per device.

<b>Table 2–10. DQ Pin Groups (Part 1 of 2)</b>			
<b>Device</b>	<b>Package</b>	<b>Number of <math>\times 8</math> DQ Pin Groups</b>	<b>Total DQ Pin Count</b>
EP1C3	100-pin TQFP (1)	3	24
	144-pin TQFP	4	32
EP1C4	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

## Slew-Rate Control

The output buffer for each Cyclone device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

## Bus Hold

Each Cyclone device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than  $V_{CCIO}$  to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 k $\Omega$  to pull the signal level to the last-driven state. [Table 4-15 on page 4-6](#) gives the specific sustaining current for each  $V_{CCIO}$  voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

## Programmable Pull-Up Resistor

Each Cyclone device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor (typically 25 k $\Omega$ ) holds the output to the  $V_{CCIO}$  level of the output pin's bank. Dedicated clock pins do not have the optional programmable pull-up resistor.

The Cyclone device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone devices.

**Table 3–2. Cyclone Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EP1C3	339
EP1C4	930
EP1C6	582
EP1C12	774
EP1C20	930

**Table 3–3. 32-Bit Cyclone Device IDCODE**

Device	IDCODE (32 bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
EP1C3	0000	0010 0000 1000 0001	000 0110 1110	1
EP1C4	0000	0010 0000 1000 0101	000 0110 1110	1
EP1C6	0000	0010 0000 1000 0010	000 0110 1110	1
EP1C12	0000	0010 0000 1000 0011	000 0110 1110	1
EP1C20	0000	0010 0000 1000 0100	000 0110 1110	1

**Notes to Table 3–3:**

- (1) The most significant bit (MSB) is on the left.
- (2) The IDCODE's least significant bit (LSB) is always 1.

Multiple Cyclone devices can be configured in any of the three configuration schemes by connecting the configuration enable ( $nCE$ ) and configuration enable output ( $nCEO$ ) pins on each device.

**Table 3–5. Data Sources for Configuration**

Configuration Scheme	Data Source
Active serial	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster or ByteBlasterMV download cable, or serial data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file

## Referenced Documents

This chapter references the following document:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

## Document Revision History

Table 3–6 shows the revision history for this chapter.

**Table 3–6. Document Revision History**

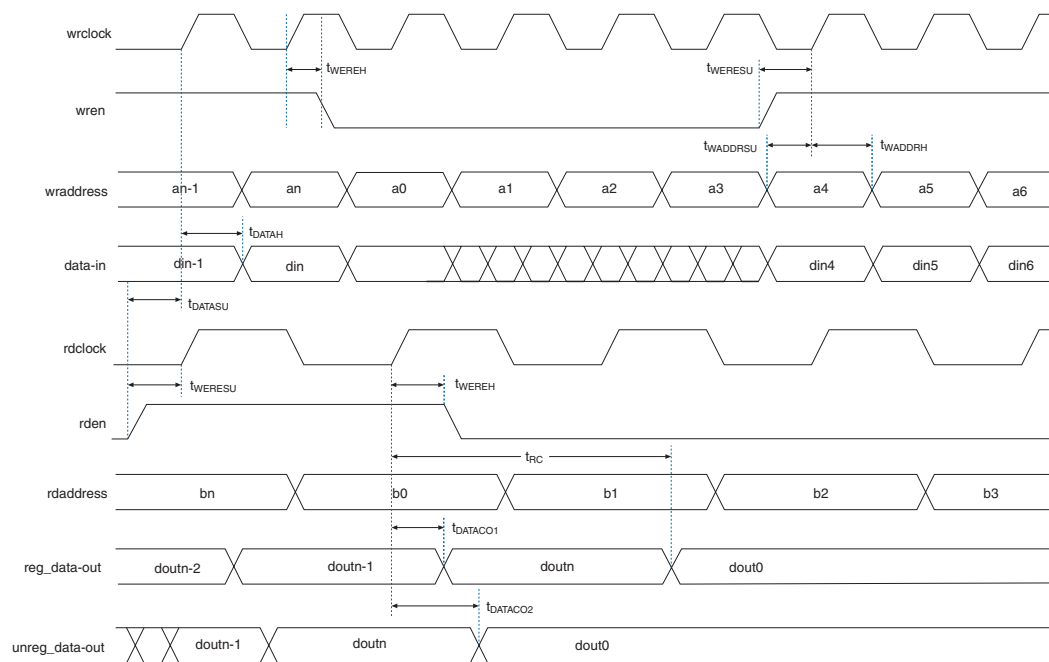
Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added “Referenced Documents” section.	—
January 2007 v1.3	<ul style="list-style-type: none"> <li>● Added document revision history.</li> <li>● Updated handpara note below Table 3–4.</li> </ul>	—
August 2005 V1.2	Minor updates.	—
February 2005 V1.1	Updated JTAG chain limits. Added information concerning test vectors.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

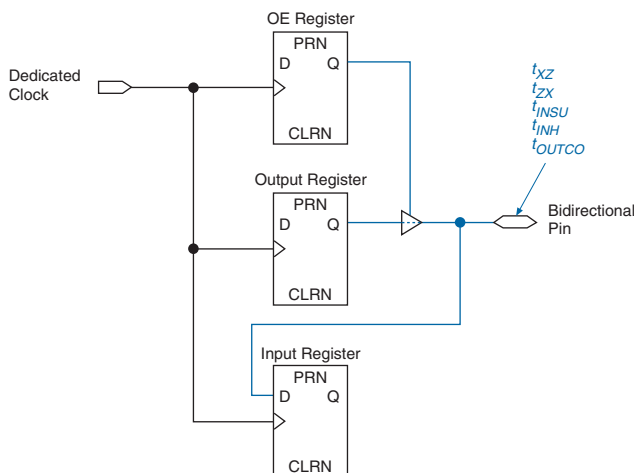


**Table 4–24. Routing Delay Internal Timing Microparameter Descriptions**

Symbol	Parameter
$t_{R4}$	Delay for an R4 line with average loading; covers a distance of four LAB columns
$t_{C4}$	Delay for an C4 line with average loading; covers a distance of four LAB rows
$t_{LOCAL}$	Local interconnect delay

Figure 4–1 shows the memory waveforms for the M4K timing parameters shown in Table 4–23.

**Figure 4–1. Dual-Port RAM Timing Microparameter Waveform**

**Figure 4–2. External Timing in Cyclone Devices**

All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in [Tables 4–40 through 4–44](#).

[Table 4–29](#) shows the external I/O timing parameters when using global clock networks.

<b>Table 4–29. Cyclone Global Clock External I/O Timing Parameters</b> <i>Notes (1), (2) (Part 1 of 2)</i>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{INSU}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by $CLK$ pin	—
$t_{INH}$	Hold time for input or bidirectional pin using IOE input register with global clock fed by $CLK$ pin	—
$t_{OUTCO}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by $CLK$ pin	$C_{LOAD} = 10 \text{ pF}$
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting	—
$t_{INHPLL}$	Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting	—

**Table 4–39. EP1C20 Row Pin Global Clock External I/O Timing Parameters**

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.417	—	2.779	—	3.140	—	ns
$t_{\text{INH}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCO}}$	2.000	3.724	2.000	4.282	2.000	4.843	ns
$t_{\text{XZ}}$	—	3.645	—	4.191	—	4.740	ns
$t_{\text{ZX}}$	—	3.645	—	4.191	—	4.740	ns
$t_{\text{INSUPLL}}$	1.417	—	1.629	—	1.840	—	ns
$t_{\text{INHPLL}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCOPLL}}$	0.500	1.667	0.500	1.917	0.500	2.169	ns
$t_{\text{XZPLL}}$	—	1.588	—	1.826	—	2.066	ns
$t_{\text{ZXPLL}}$	—	1.588	—	1.826	—	2.066	ns

## External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–40 through 4–45 show the adder delays associated with column and row I/O pins for all packages. If an I/O standard is selected other than LVTTTL 4 mA with a fast slew rate, add the selected delay to the external  $t_{\text{CO}}$  and  $t_{\text{SU}}$  I/O parameters shown in Tables 4–25 through 4–28.

**Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 1 of 2)**

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVC MOS	—	0	—	0	—	0	ps
3.3-V LVTTTL	—	0	—	0	—	0	ps
2.5-V LVTTTL	—	27	—	31	—	35	ps
1.8-V LVTTTL	—	182	—	209	—	236	ps
1.5-V LVTTTL	—	278	—	319	—	361	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps

**Table 4–52. Cyclone PLL Specifications (Part 2 of 2)**

Symbol	Parameter	Min	Max	Unit
$f_{OUT}$ (to global clock)	PLL output frequency (-6 speed grade)	15.625	405	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz
$t_{OUT}$ DUTY	Duty cycle for external clock output (when set to 50%)	45.00	55	%
$t_{JITTER}$ (1)	Period jitter for external clock output	—	$\pm 300$ (2)	ps
$t_{LOCK}$ (3)	Time required to lock from end of device configuration	10.00	100	$\mu$ s
$f_{VCO}$	PLL internal VCO operating range	500.00	1,000	MHz
-	Minimum areset time	10	—	ns
N, G0, G1, E	Counter values	1	32	integer

**Notes to Table 4–52:**

- (1) The  $t_{JITTER}$  specification for the PLL[2..1]\_OUT pins are dependent on the I/O pins in its  $V_{CCIO}$  bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength or slow slew rate.
- (2)  $f_{OUT} \geq 100$  MHz. When the PLL external clock output frequency ( $f_{OUT}$ ) is smaller than 100 MHz, the jitter specification is 60 mUI.
- (3)  $f_{IN/N}$  must be greater than 200 MHz to ensure correct lock detect circuit operation below  $-20^{\circ}\text{C}$ . Otherwise, the PLL operates with the specified parameters under the specified conditions.

## Document Revision History

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February 2005 v1.1	Updated Figure 5-1.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—