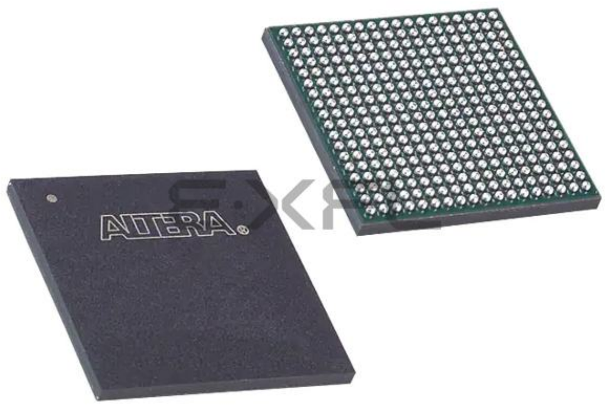


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1206 |
| Number of Logic Elements/Cells | 12060 |
| Total RAM Bits | 239616 |
| Number of I/O | 249 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 324-BGA |
| Supplier Device Package | 324-FBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1c12f324i7 |

# 1. Introduction

C51001-1.5

## Introduction

The Cyclone® field programmable gate array family is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 Kbits of RAM. With features like phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements, Cyclone devices are a cost-effective solution for data-path applications. Cyclone devices support various I/O standards, including LVDS at data rates up to 640 megabits per second (Mbps), and 66- and 33-MHz, 64- and 32-bit peripheral component interconnect (PCI), for interfacing with and supporting ASSP and ASIC devices. Altera also offers new low-cost serial configuration devices to configure Cyclone devices.

## Features

The Cyclone device family offers the following features:

- 2,910 to 20,060 LEs, see Table 1–1
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66- and 33-MHz, 64- and 32-bit PCI standard
- High-speed (640 Mbps) LVDS I/O support
- Low-speed (311 Mbps) LVDS I/O support
- 311-Mbps RSDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz), FCRAM, and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) cores, including Altera® MegaCore® functions and Altera Megafunctions Partners Program (AMPP℠) megafunctions.

*Table 1–1. Cyclone Device Features (Part 1 of 2)*

| Feature | EP1C3 | EP1C4 | EP1C6 | EP1C12 | EP1C20 |
|---|---|---|---|---|---|
| LEs | 2,910 | 4,000 | 5,980 | 12,060 | 20,060 |
| M4K RAM blocks (128 × 36 bits) | 13 | 17 | 20 | 52 | 64 |

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to M4K memory blocks. A carry chain can continue as far as a full column.

### *Clear and Preset Logic Control*

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Cyclone devices support simultaneous preset/ asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Cyclone devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

## MultiTrack Interconnect

In the Cyclone architecture, connections between LEs, M4K memory blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

*Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)*

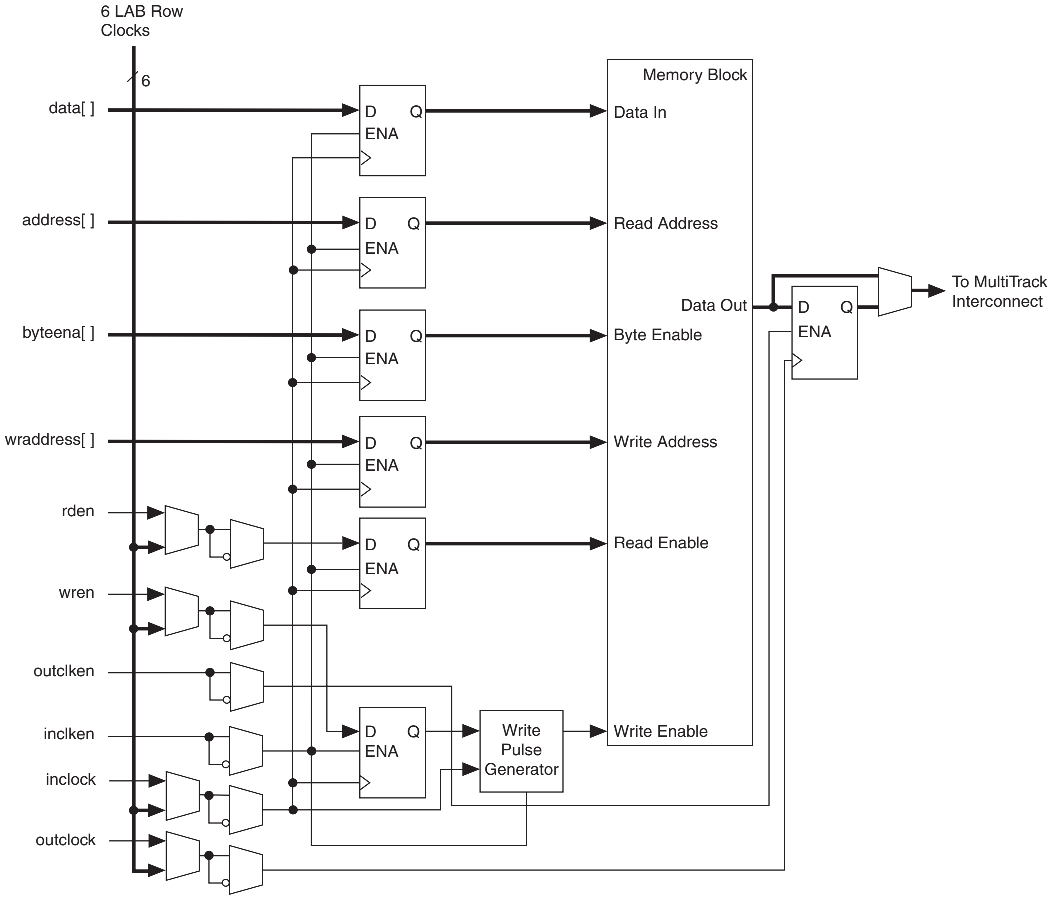
| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 4K × 1 | 2K × 2 | 1K × 4 | 512 × 8 | 256 × 16 | 128 × 32 | 512 × 9 | 256 × 18 | 128 × 36 |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 128 × 32 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 512 × 9 | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| 256 × 18 | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| 128 × 36 | — | — | — | — | — | — | ✓ | ✓ | ✓ |

*Table 2–4. M4K RAM Block Configurations (True Dual-Port)*

| Port A | Port B | | | | | | |
|---|---|---|---|---|---|---|---|
| | 4K × 1 | 2K × 2 | 1K × 4 | 512 × 8 | 256 × 16 | 512 × 9 | 256 × 18 |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 512 × 9 | — | — | — | — | — | ✓ | ✓ |
| 256 × 18 | — | — | — | — | — | ✓ | ✓ |

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

***Figure 2–19. Input/Output Clock Mode in Simple Dual-Port Mode*** *Notes (1), (2)*




*Notes to Figure 2–19:*

(1) All registers shown except the rden register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

*Table 2–7. Global Clock Network Sources (Part 2 of 2)*

| Source | | GCLK0 | GCLK1 | GCLK2 | GCLK3 | GCLK4 | GCLK5 | GCLK6 | GCLK7 |
|---|---|---|---|---|---|---|---|---|---|
| Dual-Purpose Clock Pins | DPCLK0 *(3)* | — | — | — | ✓ | — | — | — | — |
| | DPCLK1 *(3)* | — | — | ✓ | — | — | — | — | — |
| | DPCLK2 | ✓ | — | — | — | — | — | — | — |
| | DPCLK3 | — | — | — | — | ✓ | — | — | — |
| | DPCLK4 | — | — | — | — | — | — | ✓ | — |
| | DPCLK5 *(3)* | — | — | — | — | — | — | — | ✓ |
| | DPCLK6 | — | — | — | — | — | ✓ | — | — |
| | DPCLK7 | — | ✓ | — | — | — | — | — | — |

*Notes to Table 2–7:*
(1) EP1C3 devices only have one PLL (PLL 1).
(2) EP1C3 devices in the 100-pin TQFP package do not have dedicated clock pins `CLK1` and `CLK3`.
(3) EP1C3 devices in the 100-pin TQFP package do not have the `DPCLK0`, `DPCLK1`, or `DPCLK5` pins.

## Clock Multiplication and Division

Cyclone PLLs provide clock synthesis for PLL output ports using $m/(n \times$ post scale counter) scaling factors. The input clock is divided by a pre-scale divider, $n$, and is then multiplied by the $m$ feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter to divide down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least-common multiple in the VCO's range).

Each PLL has one pre-scale divider, $n$, that can range in value from 1 to 32. Each PLL also has one multiply divider, $m$, that can range in value from 2 to 32. Global clock outputs have two post scale G dividers for global clock outputs, and external clock outputs have an E divider for external clock output, both ranging from 1 to 32. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

## Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

## Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

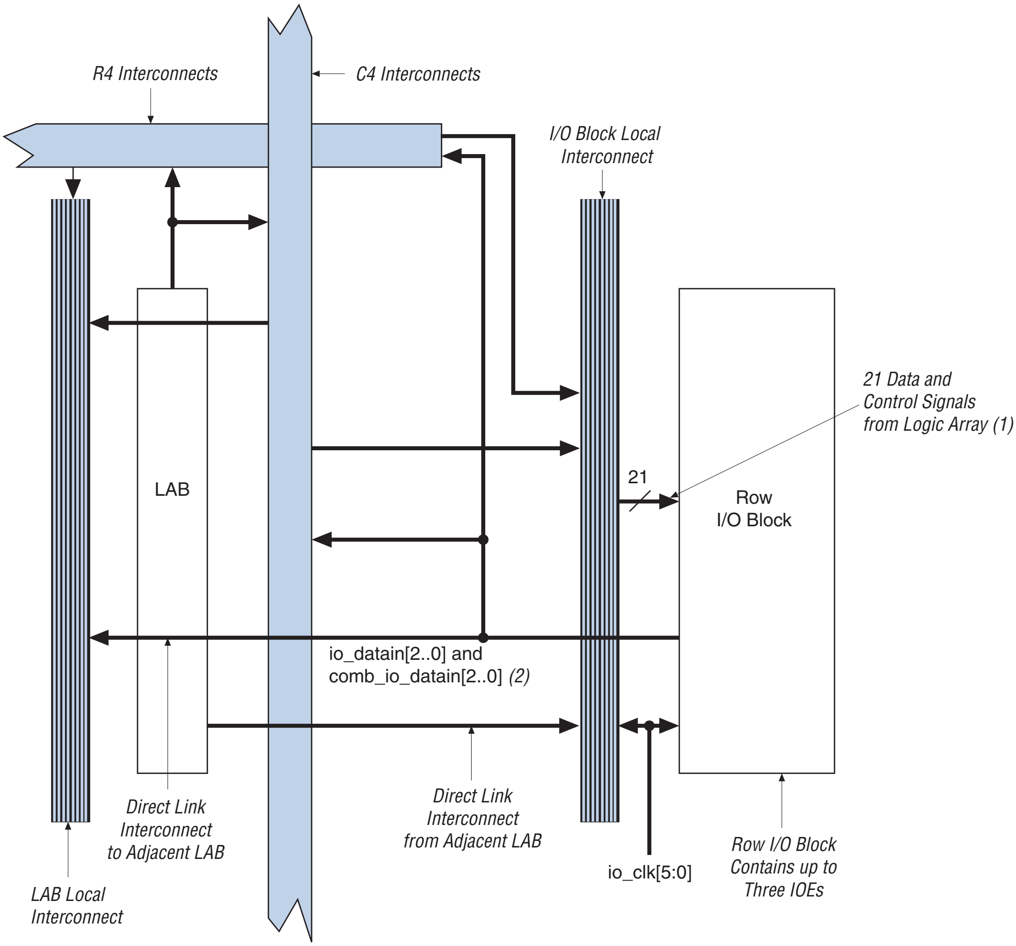
The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

*Figure 2–28. Row I/O Block Connection to the Interconnect*

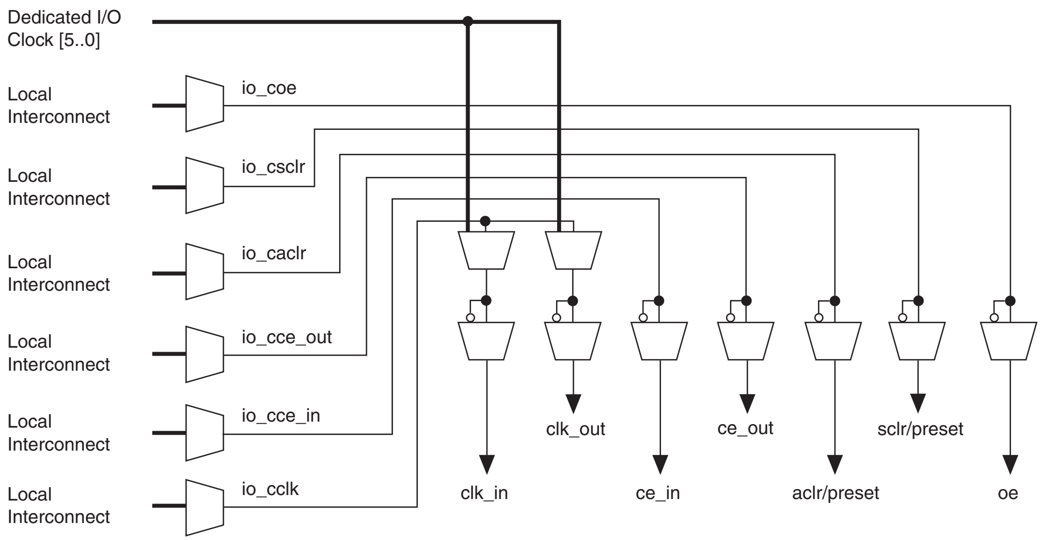



*Notes to Figure 2–28:*

(1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.

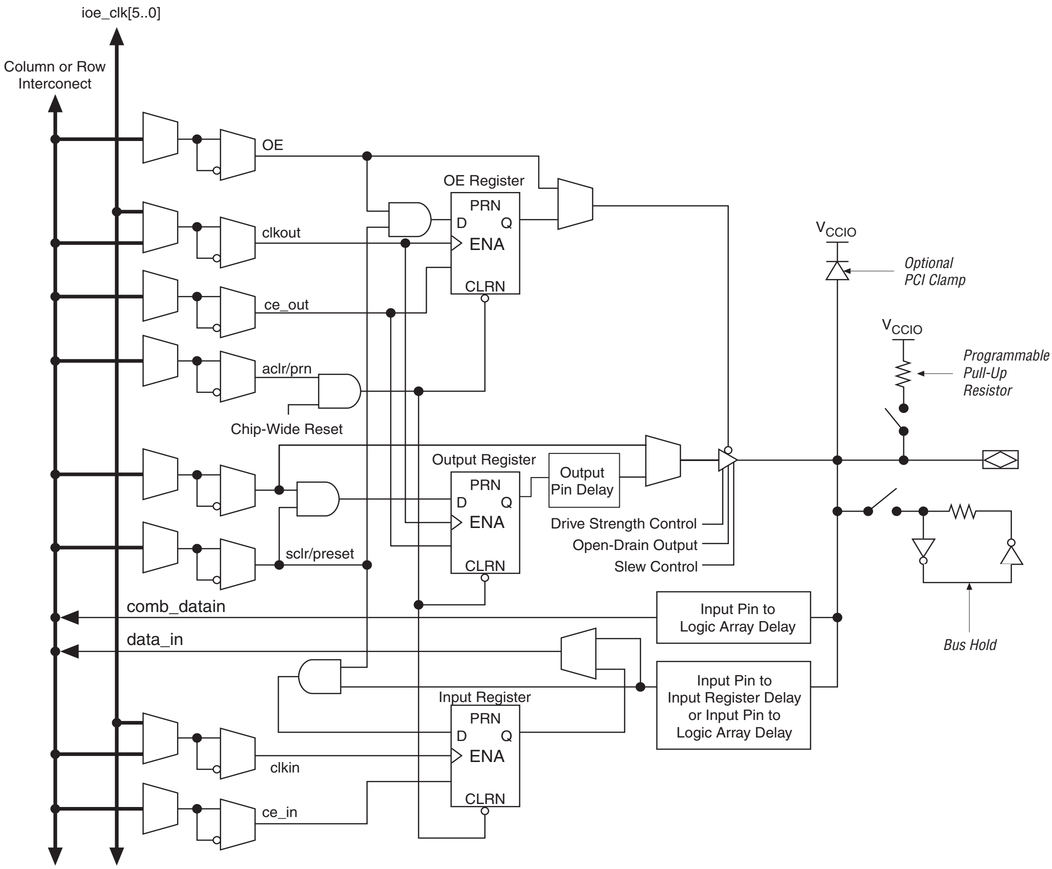
(2) Each of the three IOEs in the row I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

*Figure 2–31. Control Signal Selection per IOE*




In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register is available for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from the local interconnect in the associated LAB, dedicated I/O clocks, or the column and row interconnects. Figure 2–32 shows the IOE in bidirectional configuration.

*Figure 2–32. Cyclone IOE in Bidirectional I/O Configuration*




The Cyclone device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 2–11 shows the possible settings for the I/O standards with drive strength control.

*Table 2–11. Programmable Drive Strength Note (1)*

| I/O Standard | $I_{OH}/I_{OL}$ Current Strength Setting (mA) |
|---|---|
| LVTTL (3.3 V) | 4 |
| | 8 |
| | 12 |
| | 16 |
| | 24 *(2)* |
| LVCMOS (3.3 V) | 2 |
| | 4 |
| | 8 |
| | 12 *(2)* |
| LVTTL (2.5 V) | 2 |
| | 8 |
| | 12 |
| | 16 *(2)* |
| LVTTL (1.8 V) | 2 |
| | 8 |
| | 12 *(2)* |
| LVCMOS (1.5 V) | 2 |
| | 4 |
| | 8 *(2)* |

***Notes to Table 2–11:***

(1) SSTL-3 class I and II, SSTL-2 class I and II, and 3.3-V PCI I/O Standards do not support programmable drive strength.

(2) This is the default current strength setting in the Quartus II software.

## Open-Drain Output

Cyclone devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

## Advanced I/O Standard Support

Cyclone device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- LVDS
- RSDS
- SSTL-2 class I and II
- SSTL-3 class I and II
- Differential SSTL-2 class II (on output clocks only)

Table 2–12 describes the I/O standards supported by Cyclone devices.

***Table 2–12. Cyclone I/O Standards***

| I/O Standard | Type | Input Reference Voltage ($V_{REF}$) (V) | Output Supply Voltage ($V_{CCIO}$) (V) | Board Termination Voltage ($V_{TT}$) (V) |
|---|---|---|---|---|
| 3.3-V LVTTL/LVCMOS | Single-ended | N/A | 3.3 | N/A |
| 2.5-V LVTTL/LVCMOS | Single-ended | N/A | 2.5 | N/A |
| 1.8-V LVTTL/LVCMOS | Single-ended | N/A | 1.8 | N/A |
| 1.5-V LVCMOS | Single-ended | N/A | 1.5 | N/A |
| 3.3-V PCI *(1)* | Single-ended | N/A | 3.3 | N/A |
| LVDS *(2)* | Differential | N/A | 2.5 | N/A |
| RSDS *(2)* | Differential | N/A | 2.5 | N/A |
| SSTL-2 class I and II | Voltage-referenced | 1.25 | 2.5 | 1.25 |
| SSTL-3 class I and II | Voltage-referenced | 1.5 | 3.3 | 1.5 |
| Differential SSTL-2 *(3)* | Differential | 1.25 | 2.5 | 1.25 |

***Notes to Table 2–12:***

(1) There is no megafunction support for EP1C3 devices for the PCI compiler. However, EP1C3 devices support PCI by using the LVTTL 16-mA I/O standard and drive strength assignments in the Quartus II software. The device requires an external diode for PCI compliance.

(2) EP1C3 devices in the 100-pin TQFP package do not support the LVDS and RSDS I/O standards.

(3) This I/O standard is only available on output clock pins (`PLL_OUT` pins). EP1C3 devices in the 100-pin package do not support this I/O standard as it does not have `PLL_OUT` pins.

Cyclone devices contain four I/O banks, as shown in Figure 2–35. I/O banks 1 and 3 support all the I/O standards listed in Table 2–12. I/O banks 2 and 4 support all the I/O standards listed in Table 2–12 except the 3.3-V PCI standard. I/O banks 2 and 4 contain dual-purpose DQS, DQ,

*Table 3–1. Cyclone JTAG Instructions (Part 2 of 2)*

| JTAG Instruction | Instruction Code | Description |
|---|---|---|
| USERCODE | 00 0000 0111 | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | 00 0000 0110 | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| HIGHZ *(1)* | 00 0000 1011 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |
| CLAMP *(1)* | 00 0000 1010 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | — | Used when configuring a Cyclone device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor. |
| PULSE_NCONFIG | 00 0000 0001 | Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected. |
| CONFIG_IO | 00 0000 1101 | Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction will hold nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured. |
| SignalTap II instructions | — | Monitors internal device operation with the SignalTap II embedded logic analyzer. |

***Note to Table 3–1:***
(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

In the Quartus II software, there is an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. Choose Assignments > Device > Device and Pin Options > General. Turn on **Auto Usercode**.

Multiple Cyclone devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 3–5. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Active serial | Low-cost serial configuration device |
| Passive serial (PS) | Enhanced or EPC2 configuration device, MasterBlaster or ByteBlasterMV download cable, or serial data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file |

## Referenced Documents

This chapter references the following document:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

## Document Revision History

Table 3–6 shows the revision history for this chapter.

*Table 3–6. Document Revision History*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| May 2008 v1.4 | Minor textual and style changes. Added “Referenced Documents” section. | — |
| January 2007 v1.3 | • Added document revision history.<br>• Updated handpara note below Table 3–4. | — |
| August 2005 V1.2 | Minor updates. | — |
| February 2005 V1.1 | Updated JTAG chain limits. Added information concerning test vectors. | — |
| May 2003 v1.0 | Added document to Cyclone Device Handbook. | — |

# 4. DC and Switching Characteristics

C51004-1.7

## Operating Conditions

Cyclone® devices are offered in both commercial, industrial, and extended temperature grades. However, industrial-grade and extended-temperature-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Cyclone devices.

**Table 4–1. Cyclone Device Absolute Maximum Ratings** *Notes (1), (2)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(3)* | –0.5 | 2.4 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_{CCA}$ | Supply voltage | With respect to ground *(3)* | –0.5 | 2.4 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | °C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | °C |
| $T_J$ | Junction temperature | BGA packages under bias | — | 135 | °C |

**Table 4–2. Cyclone Device Recommended Operating Conditions (Part 1 of 2)**

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4)* | 1.425 | 1.575 | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4)* | 3.00 | 3.60 | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4)* | 2.375 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | *(4)* | 1.71 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | *(4)* | 1.4 | 1.6 | V |
| $V_I$ | Input voltage | *(3)*, *(5)* | –0.5 | 4.1 | V |

*Table 4–13. SSTL-3 Class I Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{REF}$ | Reference voltage | — | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | — | $V_{REF}$ + 0.2 | — | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | — | –0.3 | — | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(11)* | $V_{TT}$ + 0.6 | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(11)* | — | — | $V_{TT}$ – 0.6 | V |

*Table 4–14. SSTL-3 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | — | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | — | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | — | $V_{REF}$ + 0.2 | — | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | — | –0.3 | — | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16 mA *(11)* | $V_{TT}$ + 0.8 | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16 mA *(11)* | — | — | $V_{TT}$ – 0.8 | V |

*Table 4–15. Bus Hold Parameters*

| Parameter | Conditions | $V_{CCIO}$ Level | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.5 V | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $V_{IN} > V_{IL}$ (maximum) | — | — | 30 | — | 50 | — | 70 | — | µA |
| High sustaining current | $V_{IN} < V_{IH}$ (minimum) | — | — | –30 | — | –50 | — | –70 | — | µA |
| Low overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | — | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | — | — | –200 | — | –300 | — | –500 | µA |

## Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in Table 4–19.

*Table 4–19. Clock Tree Maximum Performance Specification*

| Parameter | Definition | -6 Speed Grade | | | -7 Speed Grade | | | -8 Speed Grade | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Clock tree $f_{MAX}$ | Maximum frequency that the clock tree can support for clocking registered logic | — | — | 405 | — | — | 320 | — | — | 275 | MHz |

Table 4–20 shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

*Table 4–20. Cyclone Device Performance*

| Resource Used | Design Size and Function | Mode | Resources Used | | | Performance | | |
|---|---|---|---|---|---|---|---|---|
| | | | LEs | M4K Memory Bits | M4K Memory Blocks | -6 Speed Grade (MHz) | -7 Speed Grade (MHz) | -8 Speed Grade (MHz) |
| LE | 16-to-1 multiplexer | — | 21 | — | — | 405.00 | 320.00 | 275.00 |
| | 32-to-1 multiplexer | — | 44 | — | — | 317.36 | 284.98 | 260.15 |
| | 16-bit counter | — | 16 | — | — | 405.00 | 320.00 | 275.00 |
| | 64-bit counter *(1)* | — | 66 | — | — | 208.99 | 181.98 | 160.75 |

*Table 4–24. Routing Delay Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{R4}$ | Delay for an R4 line with average loading; covers a distance of four LAB columns |
| $t_{C4}$ | Delay for an C4 line with average loading; covers a distance of four LAB rows |
| $t_{LOCAL}$ | Local interconnect delay |

Figure 4–1 shows the memory waveforms for the M4K timing parameters shown in Table 4–23.

*Figure 4–1. Dual-Port RAM Timing Microparameter Waveform*

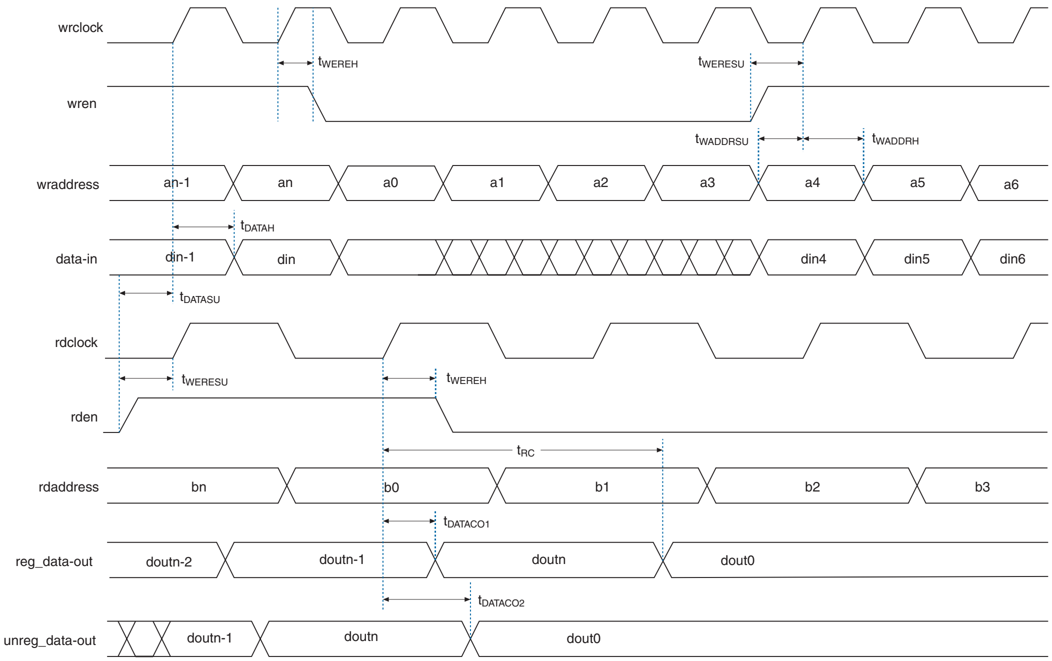


*Table 4–27. M4K Block Internal Timing Microparameters*

| Symbol | -6 | | -7 | | -8 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{M4KRC}$ | — | 4,379 | | 5,035 | | 5,691 | ps |
| $t_{M4KWC}$ | — | 2,910 | | 3,346 | | 3,783 | ps |
| $t_{M4KWERESU}$ | 72 | — | 82 | — | 93 | — | ps |
| $t_{M4KWEREH}$ | 43 | — | 49 | — | 55 | — | ps |
| $t_{M4KBESU}$ | 72 | — | 82 | — | 93 | — | ps |
| $t_{M4KBEH}$ | 43 | — | 49 | — | 55 | — | ps |
| $t_{M4KDATAASU}$ | 72 | — | 82 | — | 93 | — | ps |
| $t_{M4KDATAAH}$ | 43 | — | 49 | — | 55 | — | ps |
| $t_{M4KADDRASU}$ | 72 | — | 82 | — | 93 | — | ps |
| $t_{M4KADDRAH}$ | 43 | — | 49 | — | 55 | — | ps |
| $t_{M4KDATABSU}$ | 72 | — | 82 | — | 93 | — | ps |
| $t_{M4KDATABH}$ | 43 | — | 49 | — | 55 | — | ps |
| $t_{M4KADDRBSU}$ | 72 | — | 82 | — | 93 | — | ps |
| $t_{M4KADDRBH}$ | 43 | — | 49 | — | 55 | — | ps |
| $t_{M4KDATACO1}$ | — | 621 | — | 714 | — | 807 | ps |
| $t_{M4KDATACO2}$ | — | 4,351 | — | 5,003 | — | 5,656 | ps |
| $t_{M4KCLKHL}$ | 1,234 | — | 1,562 | — | 1,818 | — | ps |
| $t_{M4KCLR}$ | 286 | — | 328 | — | 371 | — | ps |

*Table 4–28. Routing Delay Internal Timing Microparameters*

| Symbol | -6 | | -7 | | -8 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{R4}$ | — | 261 | — | 300 | — | 339 | ps |
| $t_{C4}$ | — | 338 | — | 388 | — | 439 | ps |
| $t_{LOCAL}$ | — | 244 | — | 281 | — | 318 | ps |

## External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–2 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Tables 4–32 through 4–33 show the external timing parameters on column and row pins for EP1C4 devices.

**Table 4–32. EP1C4 Column Pin Global Clock External I/O Timing Parameters** *Note (1)*

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.471 | — | 2.841 | — | 3.210 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.937 | 2.000 | 4.526 | 2.000 | 5.119 | ns |
| $t_{INSUPLL}$ | 1.471 | — | 1.690 | — | 1.910 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.080 | 0.500 | 2.392 | 0.500 | 2.705 | ns |

**Table 4–33. EP1C4 Row Pin Global Clock External I/O Timing Parameters** *Note (1)*

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.600 | — | 2.990 | — | 3.379 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.991 | 2.000 | 4.388 | 2.000 | 5.189 | ns |
| $t_{INSUPLL}$ | 1.300 | — | 1.494 | — | 1.689 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.234 | 0.500 | 2.569 | 0.500 | 2.905 | ns |

***Note to Tables 4–32 and 4–33:***

(1) Contact Altera Applications for EP1C4 device timing parameters.

| | | |
|---|---|---|
| July 2003<br>v1.1 | Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section. | — |
| May 2003<br>v1.0 | Added document to Cyclone Device Handbook. | — |