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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	173
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c12q240c6">https://www.e-xfl.com/product-detail/intel/ep1c12q240c6</a>

to the appropriate plane on the board. The Quartus II software reserves I/O pins as power pins as necessary for layout with the larger densities in the same package having more power pins.

**Table 1–3. Cyclone QFP and FineLine BGA Package Sizes**

Dimension	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0.5	0.5	0.5	1.0	1.0	1.0
Area (mm <sup>2</sup> )	256	484	1,024	289	361	441
Length × width (mm × mm)	16×16	22×22	34.6×34.6	17×17	19×19	21×21

## Document Revision History

Table 1–4 shows the revision history for this document.

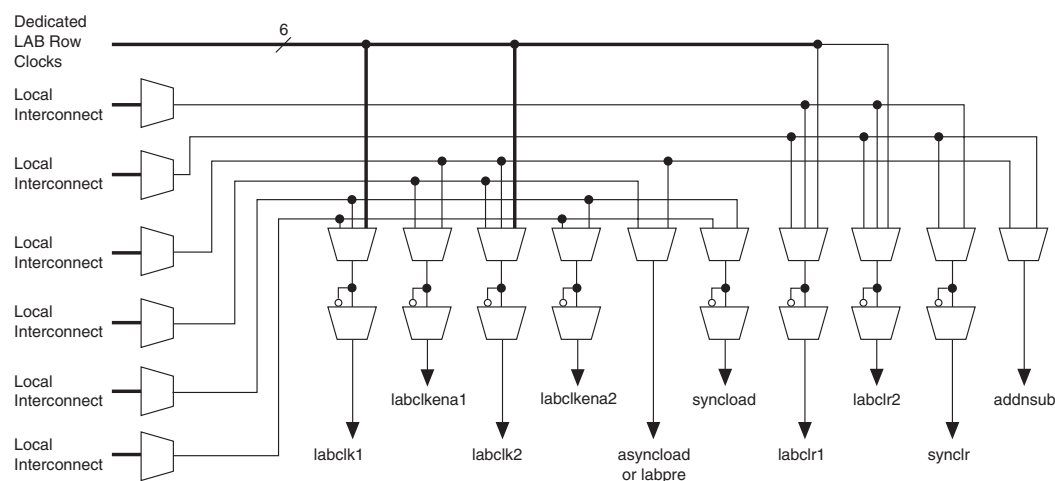
**Table 1–4. Document Revision History**

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.5	Minor textual and style changes.	—
January 2007 v1.4	Added document revision history.	—
August 2005 v1.3	Minor updates.	—
October 2003 v1.2	Added 64-bit PCI support information.	—
September 2003 v1.1	<ul style="list-style-type: none"> <li>Updated LVDS data rates to 640 Mbps from 311 Mbps.</li> <li>Updated RSDS feature information.</li> </ul>	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

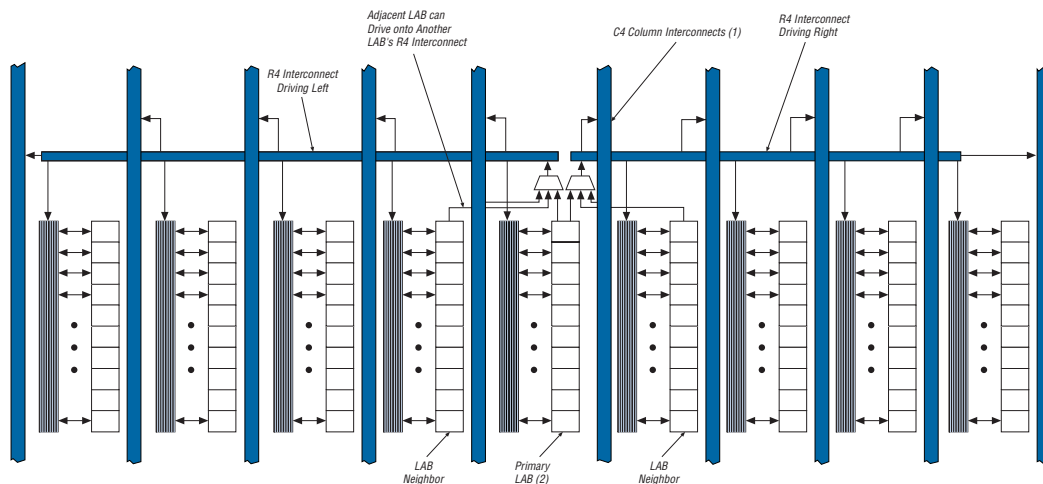
The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. [Figure 2-4](#) shows the LAB control signal generation circuit.

**Figure 2-4. LAB-Wide Control Signals**



## Logic Elements

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See [Figure 2-5](#).

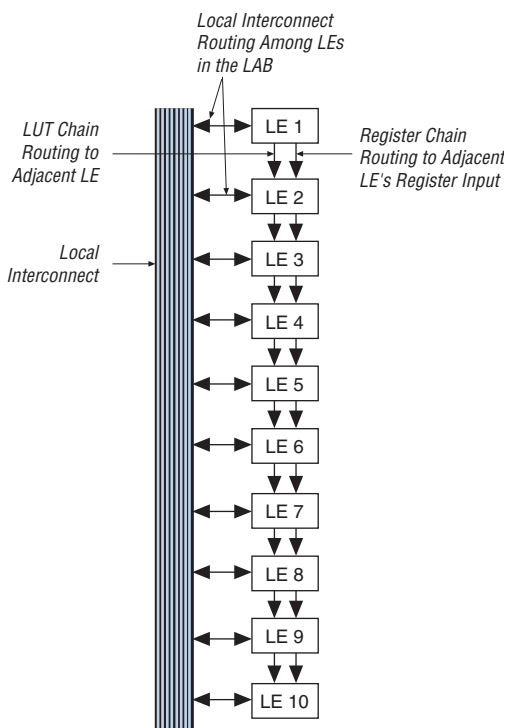
**Figure 2–9. R4 Interconnect Connections****Notes to Figure 2–9:**

- (1) C4 interconnects can drive R4 interconnects.
- (2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, M4K memory blocks, and row and column IOEs. These column resources include:

- LUT chain interconnects within a LAB
- Register chain interconnects within a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction

Cyclone devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

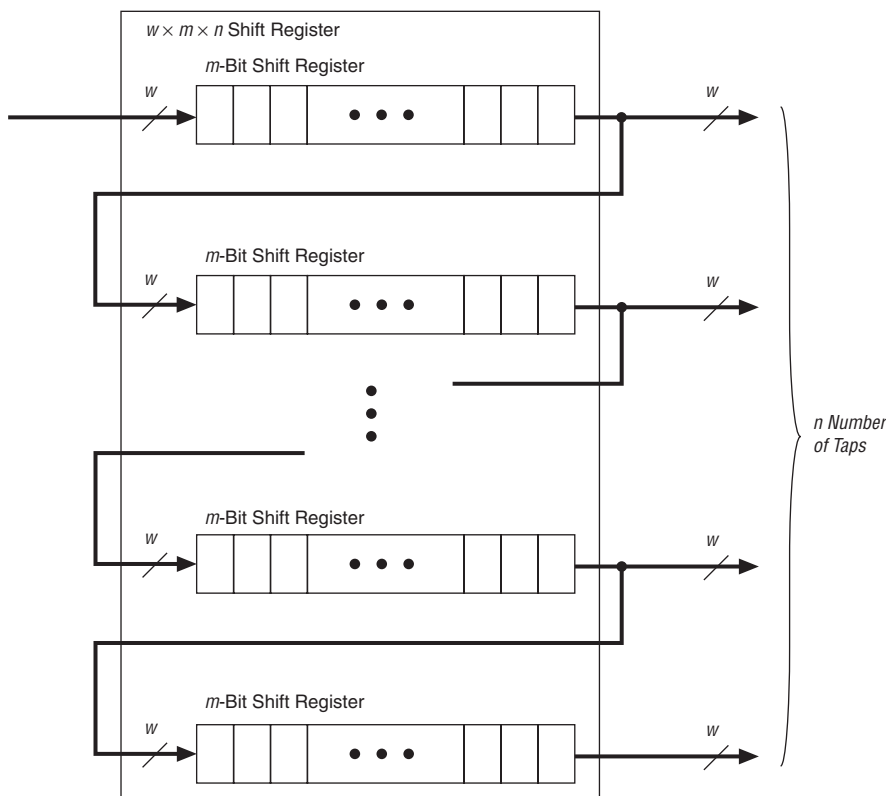
**Figure 2–10. LUT Chain and Register Chain Interconnects**

The C4 interconnects span four LABs or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. [Figure 2–11](#) shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including PLLs, M4K memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

register outputs (number of taps  $n \times$  width  $w$ ) must be less than the maximum data width of the M4K RAM block ( $\times 36$ ). To create larger shift registers, multiple memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 2-14 shows the M4K memory block in the shift register mode.

**Figure 2-14. Shift Register Memory Configuration**



## Memory Configuration Sizes

The memory address depths and output widths can be configured as  $4,096 \times 1$ ,  $2,048 \times 2$ ,  $1,024 \times 4$ ,  $512 \times 8$  (or  $512 \times 9$  bits),  $256 \times 16$  (or  $256 \times 18$  bits), and  $128 \times 32$  (or  $128 \times 36$  bits). The  $128 \times 32$ - or  $36$ -bit configuration

is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. [Tables 2-3](#) and [2-4](#) summarize the possible M4K RAM block configurations.

**Table 2-3. M4K RAM Block Configurations (Simple Dual-Port)**

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

**Table 2-4. M4K RAM Block Configurations (True Dual-Port)**

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ( $w \times m \times n$ ).

## Byte Enables

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2-5 summarizes the byte selection.

<b>Table 2-5. Byte Enable for M4K Blocks</b> <i>Notes (1), (2)</i>		
<b>byteena[3..0]</b>	<b>datain ×18</b>	<b>datain ×36</b>
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	—	[26..18]
[3] = 1	—	[35..27]

**Notes to Table 2-5:**

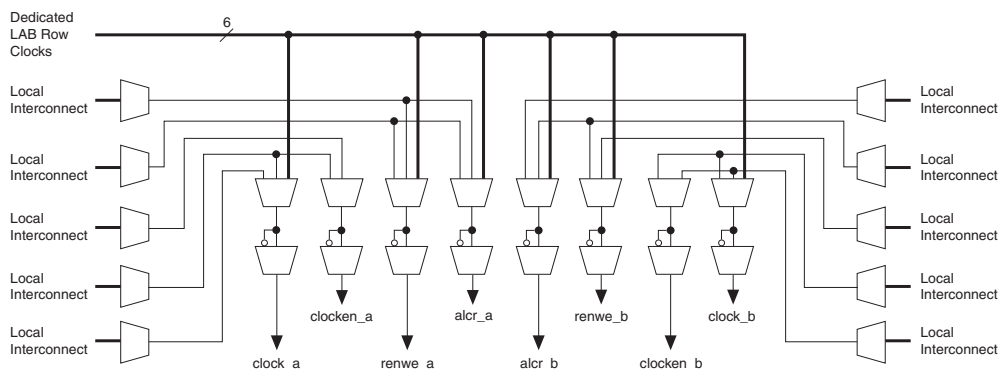
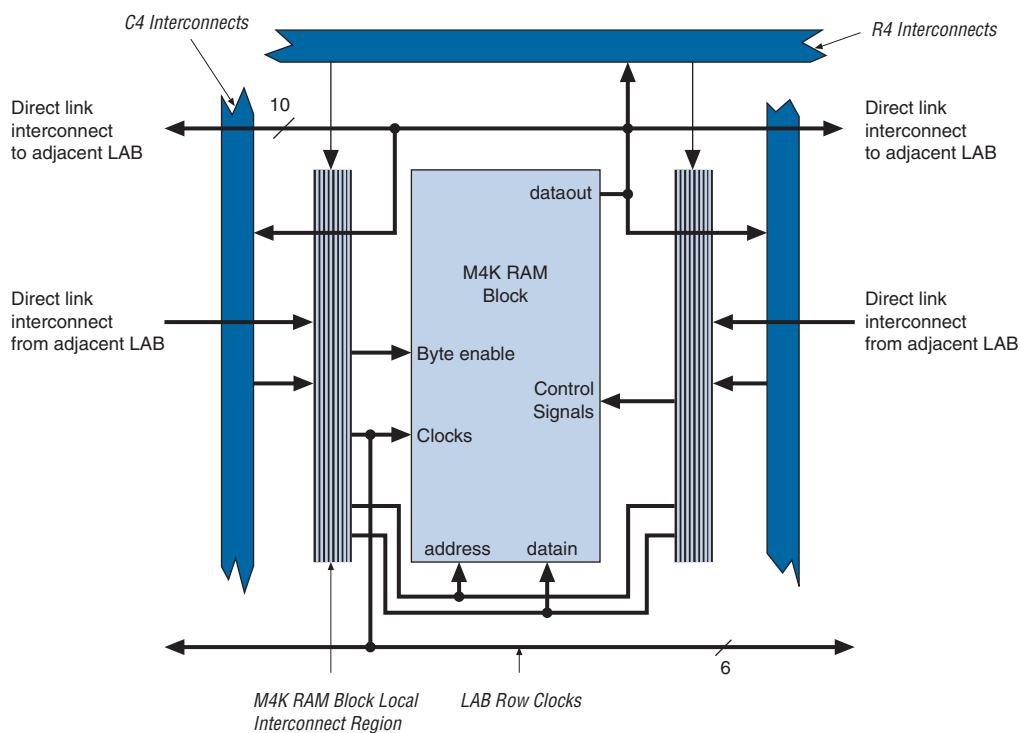
- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

## Control Signals and M4K Interface

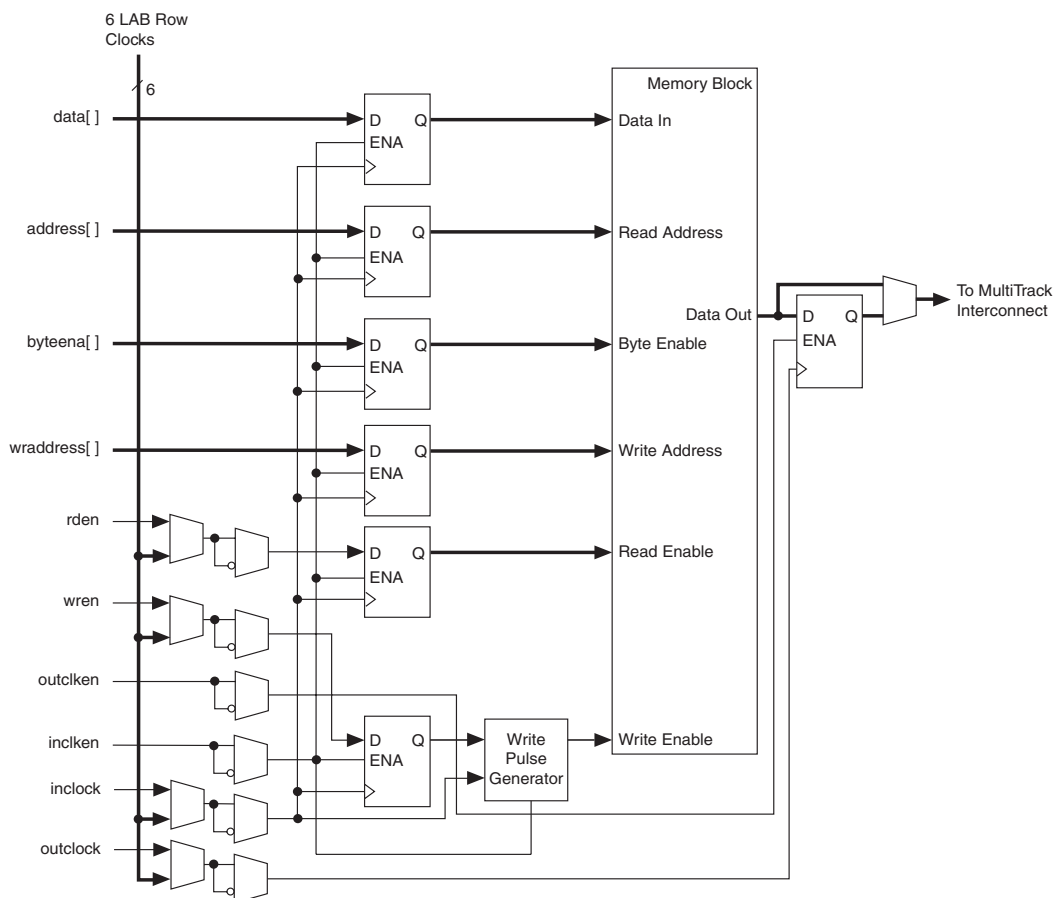
The M4K blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K block registers (*renwe*, *address*, *byte enable*, *datain*, and output registers). Only the output register can be bypassed. The six *labclk* signals or local interconnects can drive the control signals for the A and B ports of the M4K block. LEs can also control the *clock\_a*, *clock\_b*, *renwe\_a*, *renwe\_b*, *clr\_a*, *clr\_b*, *clocken\_a*, and *clocken\_b* signals, as shown in Figure 2-15.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2-16 shows the M4K block to logic array interface.



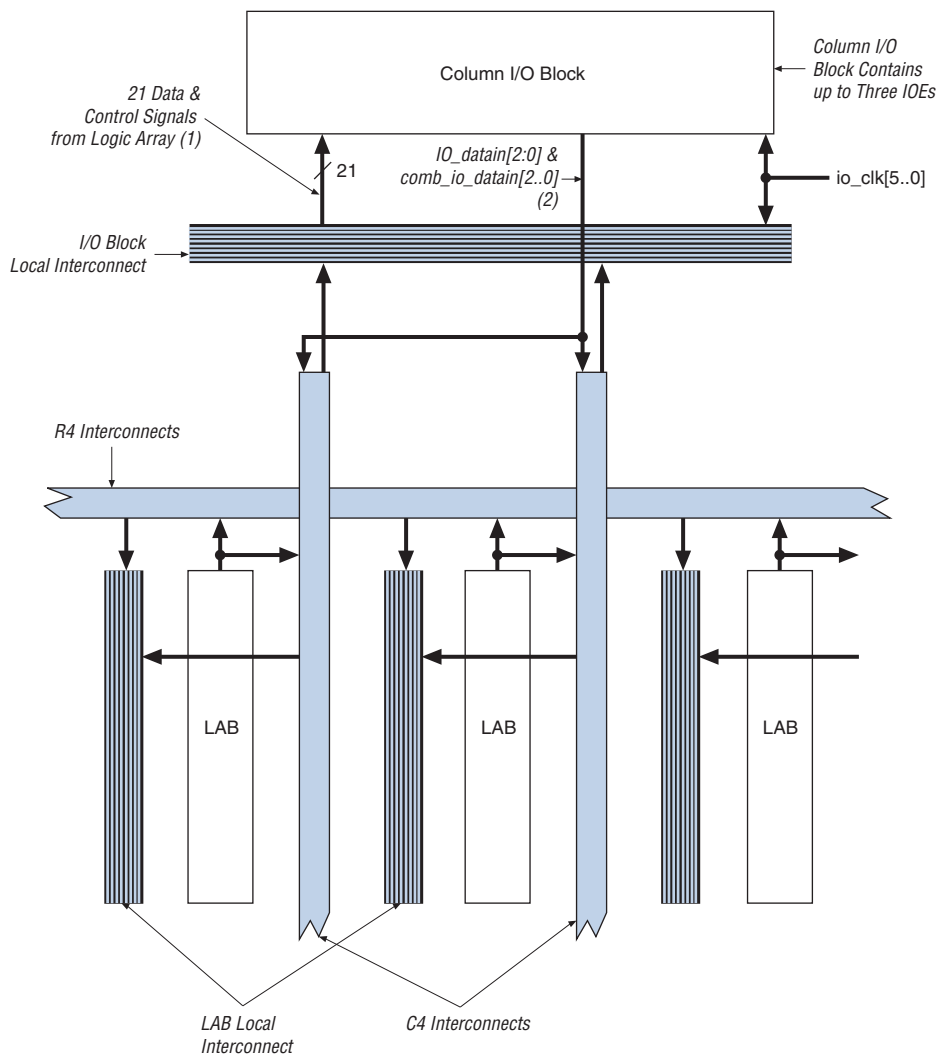
**Figure 2–15. M4K RAM Block Control Signals****Figure 2–16. M4K RAM Block LAB Row Interface**

**Figure 2–19. Input/Output Clock Mode in Simple Dual-Port Mode** *Notes (1), (2)*



**Notes to Figure 2–19:**

- (1) All registers shown except the rden register have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

**Figure 2–29. Column I/O Block Connection to the Interconnect****Notes to Figure 2–29:**

- (1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.
- (2) Each of the three IOEs in the column I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

Each I/O bank can support multiple standards with the same  $V_{CCIO}$  for input and output pins. For example, when  $V_{CCIO}$  is 3.3-V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

## LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100- $\Omega$  termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

<b>Table 2–13. Cyclone Device LVDS Channels</b>		
<b>Device</b>	<b>Pin Count</b>	<b>Number of LVDS Channels</b>
EP1C3	100	(1)
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

**Note to Table 2–13:**

- (1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

## MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and four sets for I/O output drivers ( $V_{CCIO}$ ).

The Cyclone  $V_{CCINT}$  pins must always be connected to a 1.5-V power supply. If the  $V_{CCINT}$  level is 1.5 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The  $V_{CCIO}$  pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when  $V_{CCIO}$  pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V or 5.0-V systems. Table 2–14 summarizes Cyclone MultiVolt I/O support.

**Table 2–14. Cyclone MultiVolt I/O Support** *Note (1)*

$V_{CCIO}$ (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ (2)	✓ (2)	—	✓	—	—	—	—
1.8	✓	✓	✓ (2)	✓ (2)	—	✓ (3)	✓	—	—	—
2.5	—	—	✓	✓	—	✓ (5)	✓ (5)	✓	—	—
3.3	—	—	✓ (4)	✓	✓ (6)	✓ (7)	✓ (7)	✓ (7)	✓	✓ (8)

**Notes to Table 2–14:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than  $V_{CCIO}$ .
- (2) When  $V_{CCIO} = 1.5\text{-V}$  or  $1.8\text{-V}$  and a  $2.5\text{-V}$  or  $3.3\text{-V}$  input signal feeds an input pin, higher pin leakage current is expected. Turn on **Allow voltage overdrive for LVTTL / LVCMOS input pins** in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combinations.
- (3) When  $V_{CCIO} = 1.8\text{-V}$ , a Cyclone device can drive a  $1.5\text{-V}$  device with  $1.8\text{-V}$  tolerant inputs.
- (4) When  $V_{CCIO} = 3.3\text{-V}$  and a  $2.5\text{-V}$  input signal feeds an input pin, the  $V_{CCIO}$  supply current will be slightly larger than expected.
- (5) When  $V_{CCIO} = 2.5\text{-V}$ , a Cyclone device can drive a  $1.5\text{-V}$  or  $1.8\text{-V}$  device with  $2.5\text{-V}$  tolerant inputs.
- (6) Cyclone devices can be  $5.0\text{-V}$  tolerant with the use of an external resistor and the internal PCI clamp diode.
- (7) When  $V_{CCIO} = 3.3\text{-V}$ , a Cyclone device can drive a  $1.5\text{-V}$ ,  $1.8\text{-V}$ , or  $2.5\text{-V}$  device with  $3.3\text{-V}$  tolerant inputs.
- (8) When  $V_{CCIO} = 3.3\text{-V}$ , a Cyclone device can drive a device with  $5.0\text{-V}$  LVTTL inputs but not  $5.0\text{-V}$  LVCMOS inputs.

## Power Sequencing and Hot Socketing

Because Cyclone devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the  $V_{CCIO}$  and  $V_{CCINT}$  power supplies may be powered in any order.

Signals can be driven into Cyclone devices before and during power up without damaging the device. In addition, Cyclone devices do not drive out during power up. Once operating conditions are reached and the device is configured, Cyclone devices operate as specified by the user.



Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4-25 through 4-28 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

**Table 4-25. LE Internal Timing Microparameters**

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	29	—	33	—	37	—	ps
$t_H$	12	—	13	—	15	—	ps
$t_{CO}$	—	173	—	198	—	224	ps
$t_{LUT}$	—	454	—	522	—	590	ps
$t_{CLR}$	129	—	148	—	167	—	ps
$t_{PRE}$	129	—	148	—	167	—	ps
$t_{CLKHL}$	1,234	—	1,562	—	1,818	—	ps

**Table 4-26. IOE Internal Timing Microparameters**

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	348	—	400	—	452	—	ps
$t_H$	0	—	0	—	0	—	ps
$t_{CO}$	—	511	—	587	—	664	ps
$t_{PIN2COMBOUT\_R}$	—	1,130	—	1,299	—	1,469	ps
$t_{PIN2COMBOUT\_C}$	—	1,135	—	1,305	—	1,475	ps
$t_{COMBIN2PIN\_R}$	—	2,627	—	3,021	—	3,415	ps
$t_{COMBIN2PIN\_C}$	—	2,615	—	3,007	—	3,399	ps
$t_{CLR}$	280	—	322	—	364	—	ps
$t_{PRE}$	280	—	322	—	364	—	ps
$t_{CLKHL}$	1,234	—	1,562	—	1,818	—	ps

Tables 4–34 through 4–35 show the external timing parameters on column and row pins for EP1C6 devices.

**Table 4–34. EP1C6 Column Pin Global Clock External I/O Timing Parameters**

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.691	—	3.094	—	3.496	—	ns
$t_{\text{INH}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCO}}$	2.000	3.917	2.000	4.503	2.000	5.093	ns
$t_{\text{INSUPLL}}$	1.513	—	1.739	—	1.964	—	ns
$t_{\text{INHPLL}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCOPLL}}$	0.500	2.038	0.500	2.343	0.500	2.651	ns

**Table 4–35. EP1C6 Row Pin Global Clock External I/O Timing Parameters**

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.774	—	3.190	—	3.605	—	ns
$t_{\text{INH}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCO}}$	2.000	3.817	2.000	4.388	2.000	4.963	ns
$t_{\text{INSUPLL}}$	1.596	—	1.835	—	2.073	—	ns
$t_{\text{INHPLL}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCOPLL}}$	0.500	1.938	0.500	2.228	0.500	2.521	ns

Tables 4–36 through 4–37 show the external timing parameters on column and row pins for EP1C12 devices.

**Table 4–36. EP1C12 Column Pin Global Clock External I/O Timing Parameters (Part 1 of 2)**

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.510	—	2.885	—	3.259	—	ns
$t_{\text{INH}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCO}}$	2.000	3.798	2.000	4.367	2.000	4.940	ns
$t_{\text{INSUPLL}}$	1.588	—	1.824	—	2.061	—	ns



**Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 2 of 2)**

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class II		–278	—	–320	—	–362	ps
LVDS		–261	—	–301	—	–340	ps

**Table 4–41. Cyclone I/O Standard Row Pin Input Delay Adders**

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVC MOS	—	0	—	0	—	0	ps
3.3-V LVTTTL	—	0	—	0	—	0	ps
2.5-V LVTTTL	—	27	—	31	—	35	ps
1.8-V LVTTTL	—	182	—	209	—	236	ps
1.5-V LVTTTL	—	278	—	319	—	361	ps
3.3-V PCI (1)	—	0	—	0	—	0	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps
SSTL-2 class II	—	–278	—	–320	—	–362	ps
LVDS	—	–261	—	–301	—	–340	ps

**Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps

**Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTTL	2 mA	—	329	—	378	—	427	ps
	8 mA	—	–661	—	–761	—	–860	ps
	12 mA	—	–655	—	–754	—	–852	ps
	16 mA	—	–795	—	–915	—	–1034	ps
1.8-V LVTTTL	2 mA	—	4	—	4	—	5	ps
	8 mA	—	–208	—	–240	—	–271	ps
	12 mA	—	–208	—	–240	—	–271	ps
1.5-V LVTTTL	2 mA	—	2,288	—	2,631	—	2,974	ps
	4 mA	—	608	—	699	—	790	ps
	8 mA	—	292	—	335	—	379	ps
SSTL-3 class I		—	–410	—	–472	—	–533	ps
SSTL-3 class II		—	–811	—	–933	—	–1,055	ps
SSTL-2 class I		—	–485	—	–558	—	–631	ps
SSTL-2 class II		—	–758	—	–872	—	–986	ps
LVDS		—	–998	—	–1,148	—	–1,298	ps

**Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps
2.5-V LVTTTL	2 mA	—	329	—	378	—	427	ps
	8 mA	—	–661	—	–761	—	–860	ps
	12 mA	—	–655	—	–754	—	–852	ps
	16 mA	—	–795	—	–915	—	–1,034	ps

July 2003 v1.1	Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

### Software

Cyclone® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analysis, and device configuration.



For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

### Device Pin-Outs

Device pin-outs for Cyclone devices are available on the Altera website ([www.altera.com](http://www.altera.com)) and in the *Cyclone Device Handbook*.

### Ordering Information

Figure 5–1 describes the ordering codes for Cyclone devices. For more information about a specific package, refer to the *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*.

