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## Understanding [Embedded - FPGAs (Field Programmable Gate Array)](https://www.e-xfl.com)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	173
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c12q240c6n

Figure 2–1. Cyclone EP1C12 Device Block Diagram
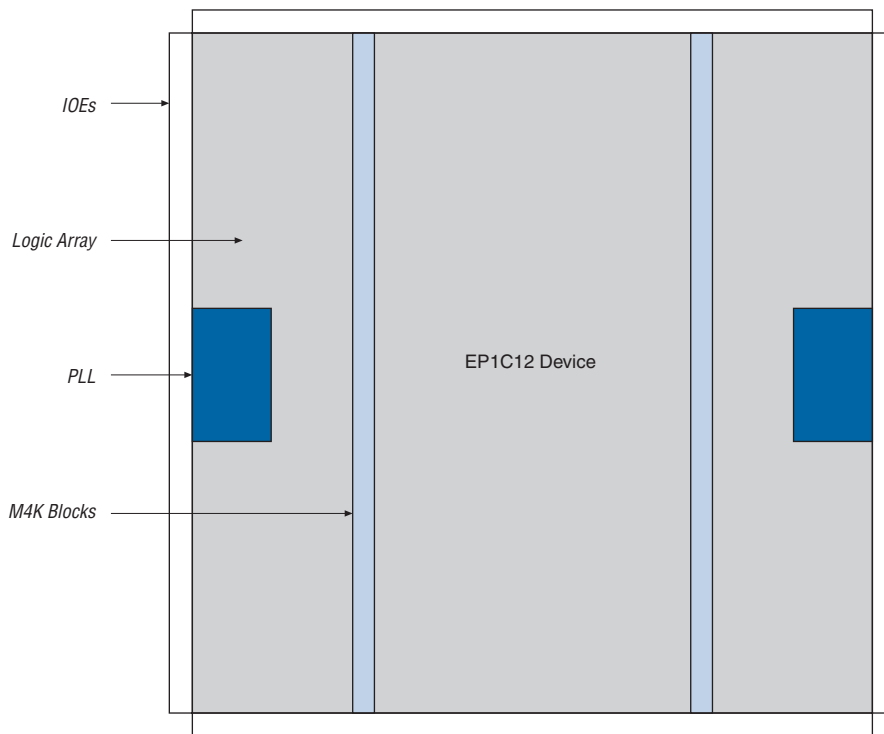
The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

| Table 2–1. Cyclone Device Resources					
Device	**M4K RAM**		**PLLs**	**LAB Columns**	**LAB Rows**
	Columns	**Blocks**			
EP1C3	1	13	1	24	13
EP1C4	1	17	2	26	17
EP1C6	1	20	2	32	20
EP1C12	2	52	2	48	26
EP1C20	2	64	2	64	32

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, look-up table (LUT) chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within a LAB. The Quartus® II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 details the Cyclone LAB.

Figure 2–2. Cyclone LAB Structure
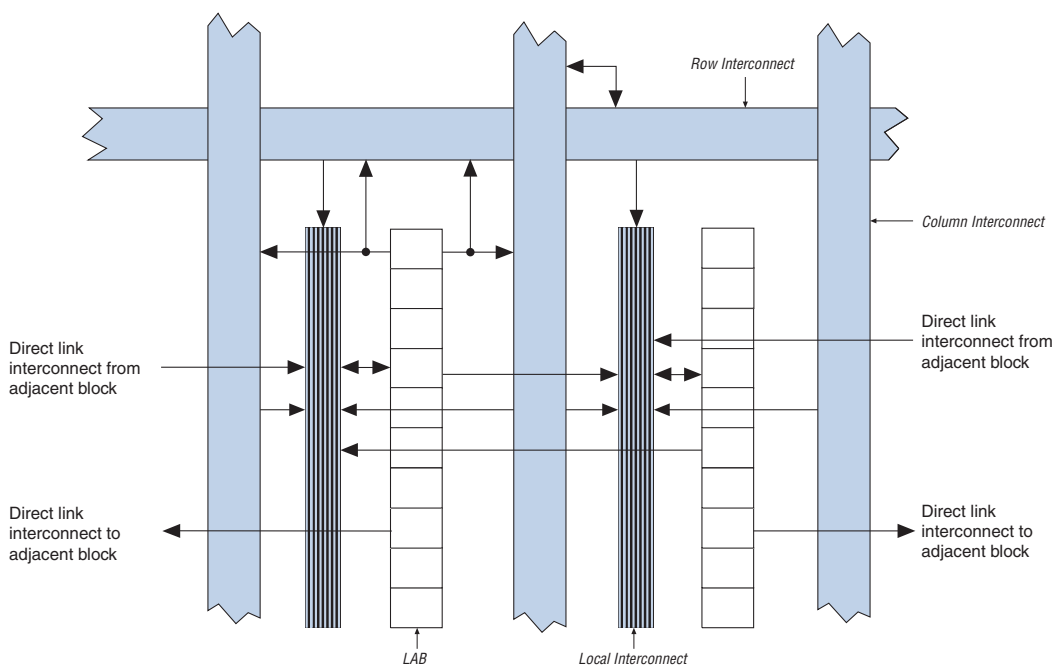
LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, and M4K RAM blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher

Figure 2–15. M4K RAM Block Control Signals
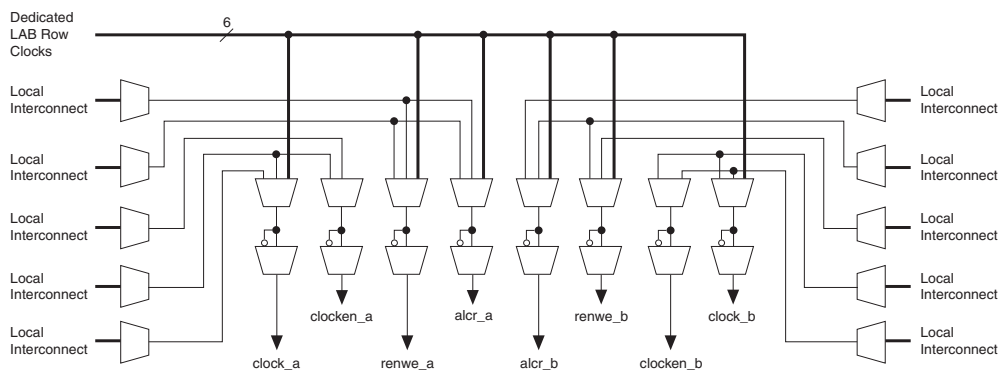
Figure 2–16. M4K RAM Block LAB Row Interface
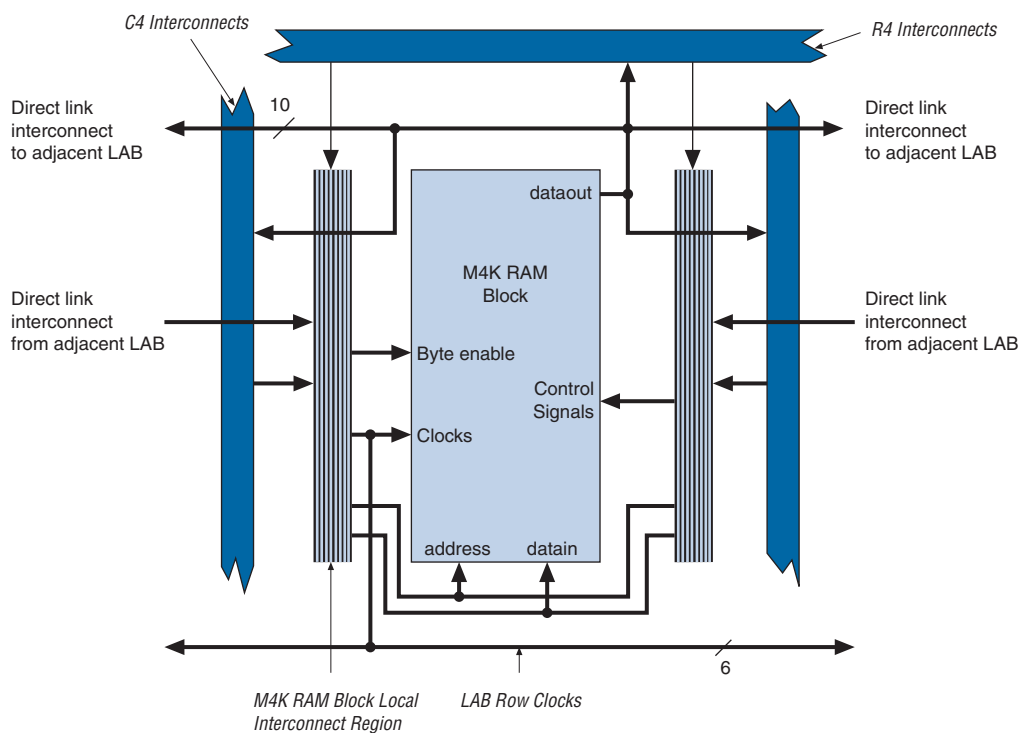
Read/Write Clock Mode

The M4K memory blocks implement read/write clock mode for simple dual-port memory. You can use up to two clocks in this mode. The write clock controls the block's data inputs, wraddress, and wren. The read clock controls the data output, rdaddress, and rden. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 2–20 shows a memory block in read/write clock mode.

*Figure 2–20. Read/Write Clock Mode in Simple Dual-Port Mode*   *Notes (1), (2)*
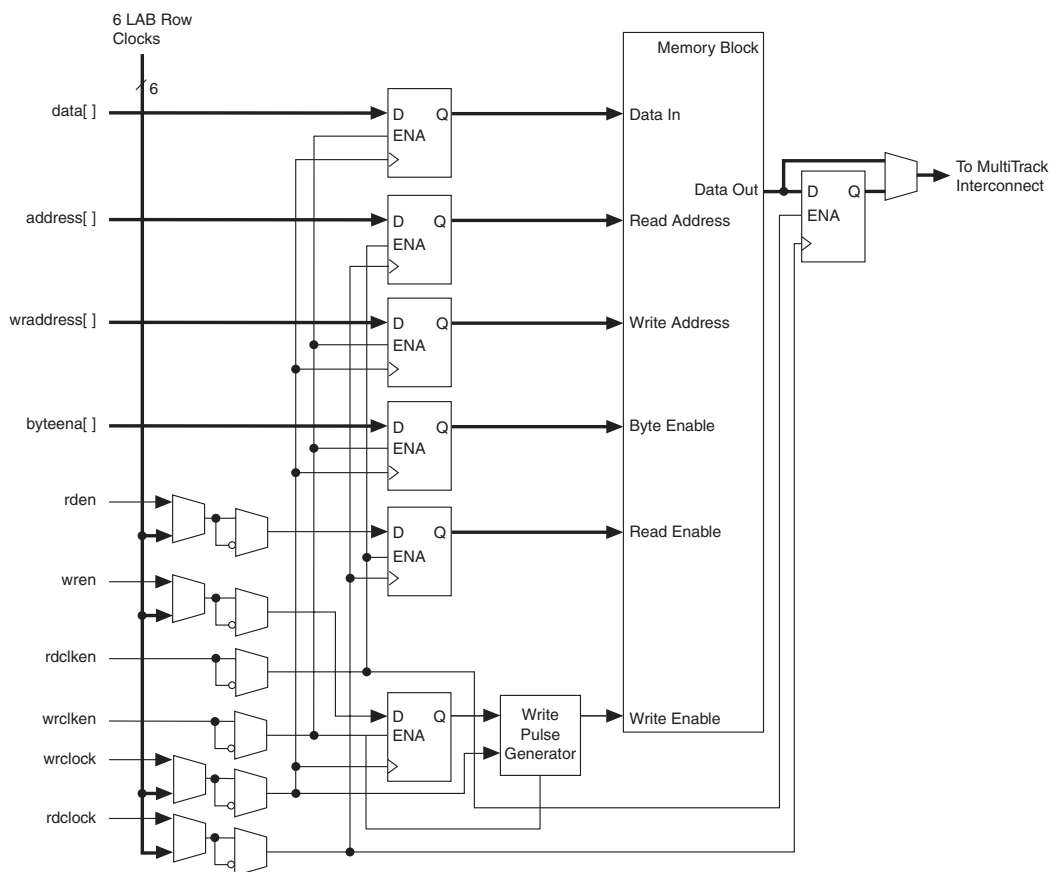
Notes to Figure 2–20:
(1)   All registers shown except the rden register have asynchronous clear ports.
(2)   Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, io_clk[5..0], provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see "Global Clock Network and Phase-Locked Loops" on page 2–29). Figure 2–30 illustrates the signal paths through the I/O block.

Figure 2–30. Signal Path through the I/O Block
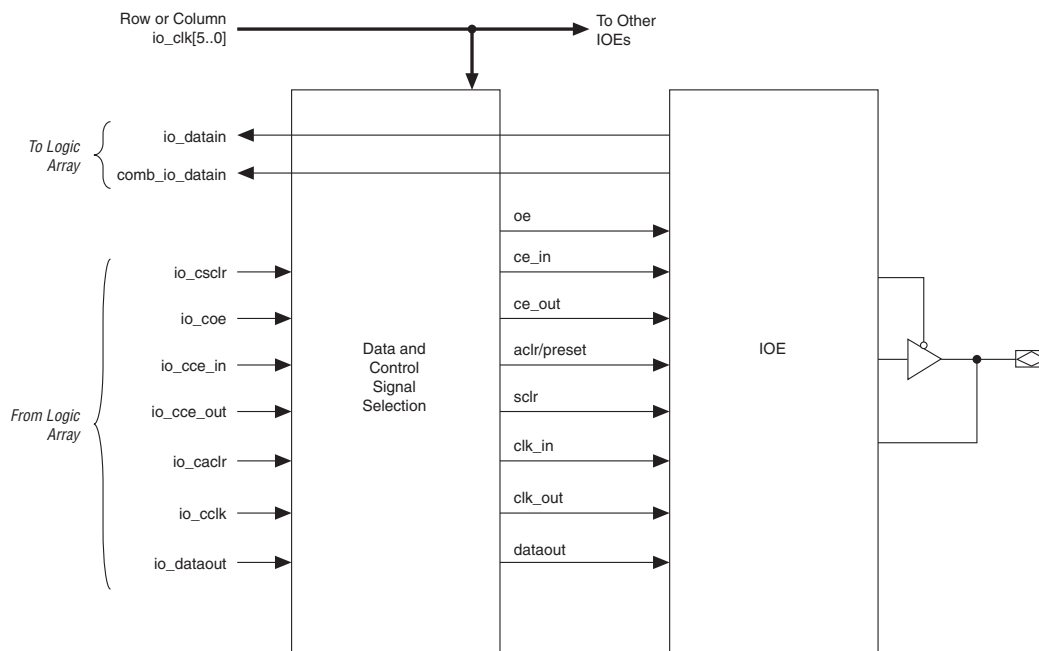
Each IOE contains its own control signal selection for the following control signals: oe, ce_in, ce_out, aclr/preset, sclr/preset, clk_in, and clk_out. Figure 2–31 illustrates the control signal selection.

Figure 2–32. Cyclone IOE in Bidirectional I/O Configuration
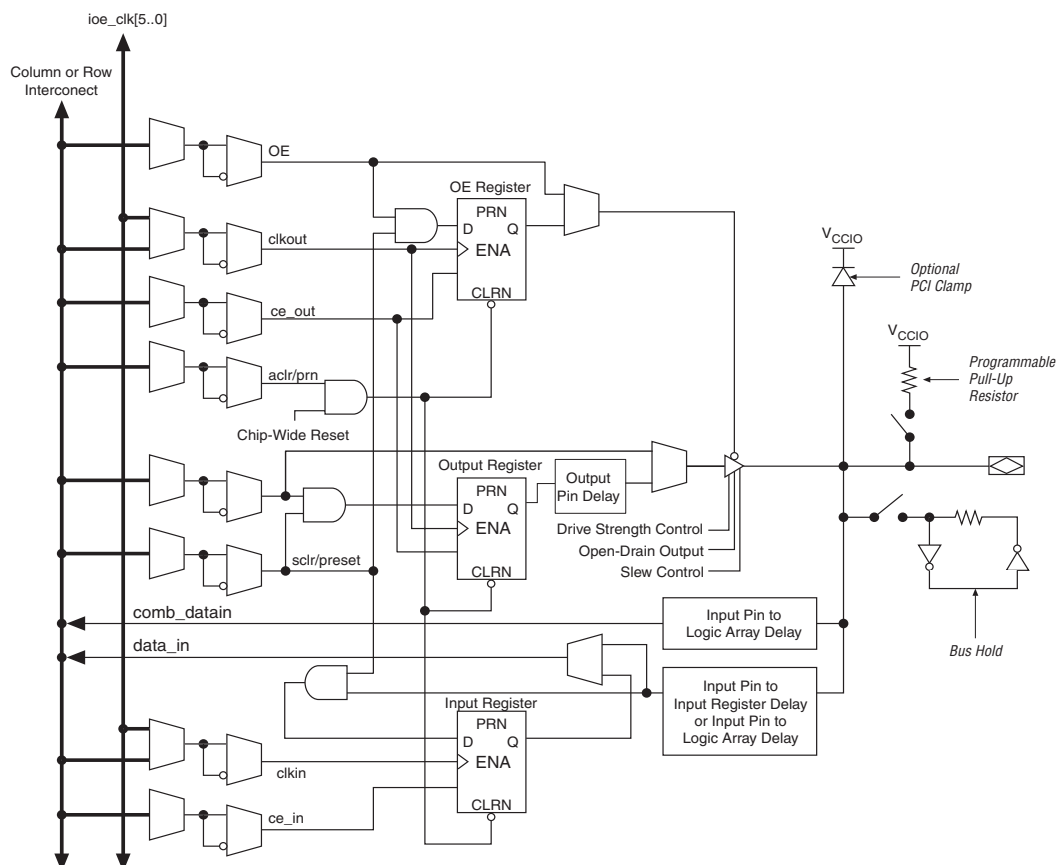
The Cyclone device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays

Table 2–10. DQ Pin Groups (Part 2 of 2)			
Device	Package	Number of ×8 DQ Pin Groups	Total DQ Pin Count
EP1C6	144-pin TQFP	4	32
	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
EP1C12	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
	324-pin FineLine BGA	8	64
EP1C20	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

Note to Table 2–10:
(1)   EP1C3 devices in the 100-pin TQFP package do not have any DQ pin groups in I/O bank 1.

A programmable delay chain on each DQS pin allows for either a 90° phase shift (for DDR SDRAM), or a 72° phase shift (for FCRAM) which automatically center-aligns input DQS synchronization signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal clocks DQ signals on internal LE registers.

These DQS delay elements combine with the PLL's clocking and phase shift ability to provide a complete hardware solution for interfacing to high-speed memory.

The clock phase shift allows the PLL to clock the DQ output enable and output paths. The designer should use the following guidelines to meet 133 MHz performance for DDR SDRAM and FCRAM interfaces:

■   The DQS signal must be in the middle of the DQ group it clocks
■   Resynchronize the incoming data to the logic array clock using successive LE registers or FIFO buffers
■   LE registers must be placed in the LAB adjacent to the DQ I/O pin column it is fed by

Figure 2–34 illustrates DDR SDRAM and FCRAM interfacing from the I/O through the dedicated circuitry to the logic array.

Advanced I/O Standard Support

Cyclone device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- LVDS
- RSDS
- SSTL-2 class I and II
- SSTL-3 class I and II
- Differential SSTL-2 class II (on output clocks only)

Table 2–12 describes the I/O standards supported by Cyclone devices.

Table 2–12. Cyclone I/O Standards				
I/O Standard	**Type**	**Input Reference Voltage (V_{REF}) (V)**	**Output Supply Voltage (V_{CCIO}) (V)**	**Board Termination Voltage (V_{TT}) (V)**
3.3-V LVTTL/LVCMOS	Single-ended	N/A	3.3	N/A
2.5-V LVTTL/LVCMOS	Single-ended	N/A	2.5	N/A
1.8-V LVTTL/LVCMOS	Single-ended	N/A	1.8	N/A
1.5-V LVCMOS	Single-ended	N/A	1.5	N/A
3.3-V PCI (1)	Single-ended	N/A	3.3	N/A
LVDS (2)	Differential	N/A	2.5	N/A
RSDS (2)	Differential	N/A	2.5	N/A
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5
Differential SSTL-2 (3)	Differential	1.25	2.5	1.25

Notes to Table 2–12:

(1) There is no megafunction support for EP1C3 devices for the PCI compiler. However, EP1C3 devices support PCI by using the LVTTL 16-mA I/O standard and drive strength assignments in the Quartus II software. The device requires an external diode for PCI compliance.

(2) EP1C3 devices in the 100-pin TQFP package do not support the LVDS and RSDS I/O standards.

(3) This I/O standard is only available on output clock pins (PLL_OUT pins). EP1C3 devices in the 100-pin package do not support this I/O standard as it does not have PLL_OUT pins.

Cyclone devices contain four I/O banks, as shown in Figure 2–35. I/O banks 1 and 3 support all the I/O standards listed in Table 2–12. I/O banks 2 and 4 support all the I/O standards listed in Table 2–12 except the 3.3-V PCI standard. I/O banks 2 and 4 contain dual-purpose DQS, DQ,

and DM pins to support a DDR SDRAM or FCRAM interface. I/O bank 1 can also support a DDR SDRAM or FCRAM interface, however, the configuration input pins in I/O bank 1 must operate at 2.5 V. I/O bank 3 can also support a DDR SDRAM or FCRAM interface, however, all the JTAG pins in I/O bank 3 must operate at 2.5 V.

Figure 2–35. Cyclone I/O Banks   *Notes (1), (2)*
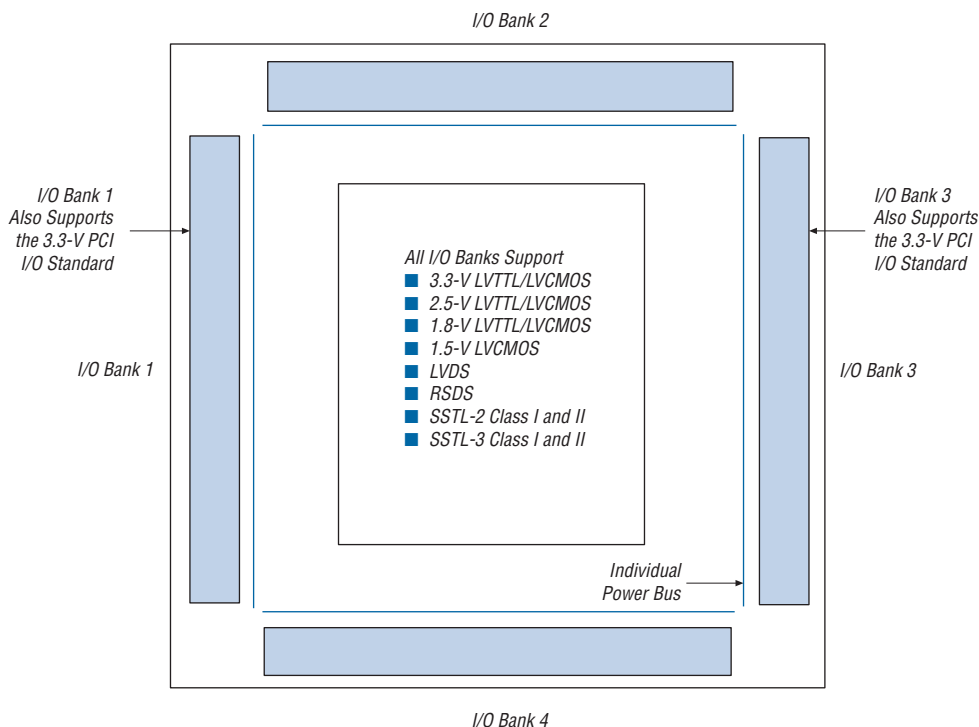
Notes to Figure 2–35:
(1) Figure 2–35 is a top view of the silicon die.
(2) Figure 2–35 is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard with different I/O voltages. Each bank also has dual-purpose `VREF` pins to support any one of the voltage-referenced standards (e.g., SSTL-3) independently. If an I/O bank does not use voltage-referenced standards, the V_{REF} pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

Table 2–13. Cyclone Device LVDS Channels		
Device	**Pin Count**	**Number of LVDS Channels**
EP1C3	100	(1)
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

Note to Table 2–13:
(1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and four sets for I/O output drivers (V_{CCIO}).

Multiple Cyclone devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 3–5. Data Sources for Configuration

Configuration Scheme	Data Source
Active serial	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster or ByteBlasterMV download cable, or serial data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file

Referenced Documents

This chapter references the following document:

■ *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
■ *Jam Programming & Test Language Specification*

Document Revision History

Table 3–6 shows the revision history for this chapter.

Table 3–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added "Referenced Documents" section.	—
January 2007 v1.3	● Added document revision history. ● Updated handpara note below Table 3–4.	—
August 2005 V1.2	Minor updates.	—
February 2005 V1.1	Updated JTAG chain limits. Added information concerning test vectors.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Table 4–10. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	$0.1 \times V_{CCIO}$	V

Table 4–11. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} − 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.15	1.25	1.35	V
V_{IH}	High-level input voltage	—	V_{REF} + 0.18	—	3.0	V
V_{IL}	Low-level input voltage	—	–0.3	—	V_{REF} − 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(11)*	V_{TT} + 0.57	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(11)*	—	—	V_{TT} − 0.57	V

Table 4–12. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.3	2.5	2.7	V
V_{TT}	Termination voltage	—	V_{REF} − 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.15	1.25	1.35	V
V_{IH}	High-level input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	—	V_{REF} − 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(11)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(11)*	—	—	V_{TT} − 0.76	V

Table 4–13. SSTL-3 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{TT}	Termination voltage	—	V_{REF} − 0.05	V_{REF}	V_{REF} + 0.05	V

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–25 through 4–28 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–25. LE Internal Timing Microparameters							
Symbol	**-6**		**-7**		**-8**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{SU}	29	—	33	—	37	—	ps
t_H	12	—	13	—	15	—	ps
t_{CO}	—	173	—	198	—	224	ps
t_{LUT}	—	454	—	522	—	590	ps
t_{CLR}	129	—	148	—	167	—	ps
t_{PRE}	129	—	148	—	167	—	ps
t_{CLKHL}	1,234	—	1,562	—	1,818	—	ps

Table 4–26. IOE Internal Timing Microparameters							
Symbol	**-6**		**-7**		**-8**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{SU}	348	—	400	—	452	—	ps
t_H	0	—	0	—	0	—	ps
t_{CO}	—	511	—	587	—	664	ps
$t_{PIN2COMBOUT\_R}$	—	1,130	—	1,299	—	1,469	ps
$t_{PIN2COMBOUT\_C}$	—	1,135	—	1,305	—	1,475	ps
$t_{COMBIN2PIN\_R}$	—	2,627	—	3,021	—	3,415	ps
$t_{COMBIN2PIN\_C}$	—	2,615	—	3,007	—	3,399	ps
t_{CLR}	280	—	322	—	364	—	ps
t_{PRE}	280	—	322	—	364	—	ps
t_{CLKHL}	1,234	—	1,562	—	1,818	—	ps

Table 4–27. M4K Block Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{M4KRC}	—	4,379		5,035		5,691	ps
t_{M4KWC}	—	2,910		3,346		3,783	ps
$t_{M4KWERESU}$	72	—	82	—	93	—	ps
$t_{M4KWEREH}$	43	—	49	—	55	—	ps
$t_{M4KBESU}$	72	—	82	—	93	—	ps
t_{M4KBEH}	43	—	49	—	55	—	ps
$t_{M4KDATAASU}$	72	—	82	—	93	—	ps
$t_{M4KDATAAH}$	43	—	49	—	55	—	ps
$t_{M4KADDRASU}$	72	—	82	—	93	—	ps
$t_{M4KADDRAH}$	43	—	49	—	55	—	ps
$t_{M4KDATABSU}$	72	—	82	—	93	—	ps
$t_{M4KDATABH}$	43	—	49	—	55	—	ps
$t_{M4KADDRBSU}$	72	—	82	—	93	—	ps
$t_{M4KADDRBH}$	43	—	49	—	55	—	ps
$t_{M4KDATACO1}$	—	621	—	714	—	807	ps
$t_{M4KDATACO2}$	—	4,351	—	5,003	—	5,656	ps
$t_{M4KCLKHL}$	1,234	—	1,562	—	1,818	—	ps
t_{M4KCLR}	286	—	328	—	371	—	ps

Table 4–28. Routing Delay Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{R4}	—	261	—	300	—	339	ps
t_{C4}	—	338	—	388	—	439	ps
t_{LOCAL}	—	244	—	281	—	318	ps

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–2 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 4–2. External Timing in Cyclone Devices
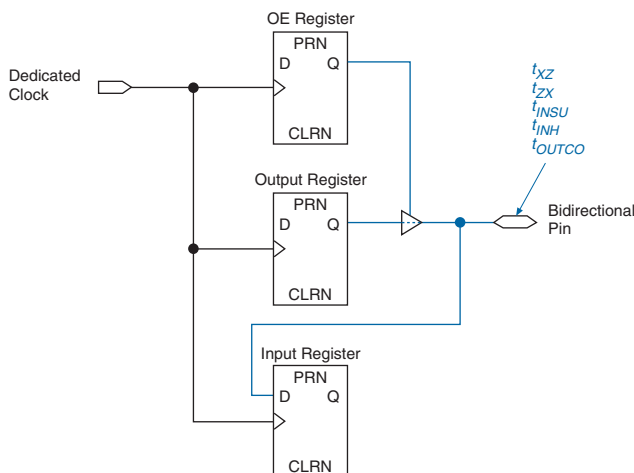
All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–40 through 4–44.

Table 4–29 shows the external I/O timing parameters when using global clock networks.

Table 4–29. Cyclone Global Clock External I/O Timing Parameters	*Notes (1), (2)* *(Part 1 of 2)*	
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin	—
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin	—
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by `CLK` pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting	—
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting	—

Table 4–39. EP1C20 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.417	—	2.779	—	3.140	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.724	2.000	4.282	2.000	4.843	ns
t_{XZ}	—	3.645	—	4.191	—	4.740	ns
t_{ZX}	—	3.645	—	4.191	—	4.740	ns
$t_{INSUPLL}$	1.417	—	1.629	—	1.840	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	1.667	0.500	1.917	0.500	2.169	ns
t_{XZPLL}	—	1.588	—	1.826	—	2.066	ns
t_{ZXPLL}	—	1.588	—	1.826	—	2.066	ns

External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–40 through 4–45 show the adder delays associated with column and row I/O pins for all packages. If an I/O standard is selected other than LVTTL 4 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters shown in Tables 4–25 through 4–28.

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS	—	0	—	0	—	0	ps
3.3-V LVTTL	—	0	—	0	—	0	ps
2.5-V LVTTL	—	27	—	31	—	35	ps
1.8-V LVTTL	—	182	—	209	—	236	ps
1.5-V LVTTL	—	278	—	319	—	361	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps

Table 4–51. Cyclone Maximum Output Clock Rate for Row Pins				
I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	296	285	273	MHz
2.5 V	381	366	349	MHz
1.8 V	286	277	267	MHz
1.5 V	219	208	195	MHz
LVCMOS	367	356	343	MHz
SSTL-3 class I	169	166	162	MHz
SSTL-3 class II	160	151	146	MHz
SSTL-2 class I	160	151	142	MHz
SSTL-2 class II	131	123	115	MHz
3.3-V PCI *(1)*	66	66	66	MHz
LVDS	320	303	275	MHz

Note to Tables 4–50 through 4–51:
(1)   EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

PLL Timing

Table 4–52 describes the Cyclone FPGA PLL specifications.

Table 4–52. Cyclone PLL Specifications (Part 1 of 2)				
Symbol	Parameter	Min	Max	Unit
f_{IN}	Input frequency (-6 speed grade)	15.625	464	MHz
	Input frequency (-7 speed grade)	15.625	428	MHz
	Input frequency (-8 speed grade)	15.625	387	MHz
f_{IN} DUTY	Input clock duty cycle	40.00	60	%
t_{IN} JITTER	Input clock period jitter	—	$\pm$ 200	ps
f_{OUT_EXT} (external PLL clock output)	PLL output frequency (-6 speed grade)	15.625	320	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz

Table 4–52. Cyclone PLL Specifications (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
f_{OUT} (to global clock)	PLL output frequency (-6 speed grade)	15.625	405	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz
t_{OUT} DUTY	Duty cycle for external clock output (when set to 50%)	45.00	55	%
t_{JITTER} *(1)*	Period jitter for external clock output	—	±300 *(2)*	ps
t_{LOCK} *(3)*	Time required to lock from end of device configuration	10.00	100	μs
f_{VCO}	PLL internal VCO operating range	500.00	1,000	MHz
-	Minimum areset time	10	—	ns
N, G0, G1, E	Counter values	1	32	integer

Notes to Table 4–52:
(1) The t_{JITTER} specification for the `PLL[2..1]_OUT` pins are dependent on the I/O pins in its V_{CCIO} bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength or slow slew rate.
(2) $f_{OUT} \geq 100$ MHz. When the PLL external clock output frequency (f_{OUT}) is smaller than 100 MHz, the jitter specification is 60 mUI.
(3) $f_{IN/N}$ must be greater than 200 MHz to ensure correct lock detect circuit operation below –20 C. Otherwise, the PLL operates with the specified parameters under the specified conditions.

| July 2003 v1.1 | Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section. | — |
| May 2003 v1.0 | Added document to Cyclone Device Handbook. | — |

C51005-1.4

Software

Cyclone® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analysis, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Cyclone devices are available on the Altera website (www.altera.com) and in the *Cyclone Device Handbook*.

Ordering Information

Figure 5–1 describes the ordering codes for Cyclone devices. For more information about a specific package, refer to the *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*.