Intel - EP1C12Q240I7N Datasheet

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1206
Number of Logic Elements/Cells	12060
Total RAM Bits	239616
Number of I/O	173
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c12q240i7n

1. Introduction

C51001-1.5

Introduction

The Cyclone® field programmable gate array family is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 Kbits of RAM. With features like phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements, Cyclone devices are a cost-effective solution for data-path applications. Cyclone devices support various I/O standards, including LVDS at data rates up to 640 megabits per second (Mbps), and 66- and 33-MHz, 64- and 32-bit peripheral component interconnect (PCI), for interfacing with and supporting ASSP and ASIC devices. Altera also offers new low-cost serial configuration devices to configure Cyclone devices.

Features

The Cyclone device family offers the following features:

- 2,910 to 20,060 LEs, see Table 1–1
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66- and 33-MHz, 64- and 32-bit PCI standard
- High-speed (640 Mbps) LVDS I/O support
- Low-speed (311 Mbps) LVDS I/O support
- 311-Mbps RSDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz), FCRAM, and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) cores, including Altera® MegaCore® functions and Altera Megafunctions Partners Program (AMPP℠) megafunctions.

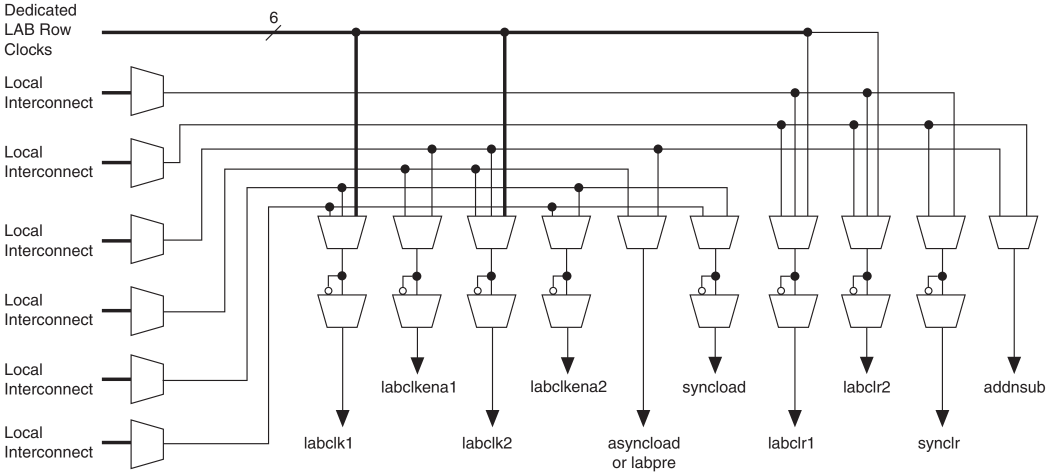
Table 1–1. Cyclone Device Features (Part 1 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
LEs	2,910	4,000	5,980	12,060	20,060
M4K RAM blocks (128 × 36 bits)	13	17	20	52	64

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in Figure 2–7, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry-in0
```

or

```
data1 + data2 + carry-in1
```

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–2 shows the Cyclone device's routing scheme.

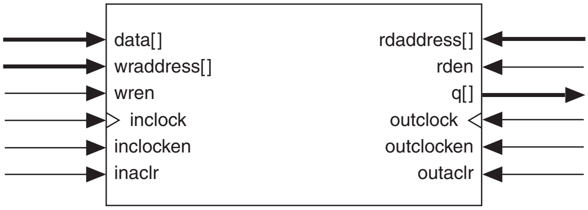
Table 2–2. Cyclone Device Routing Scheme

Source	Destination										
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	C4 Interconnect	LE	M4K RAM Block	PLL	Column IOE	Row IOE
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	✓
Direct Link Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	—	—	—
M4K RAM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
PLL	—	—	—	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

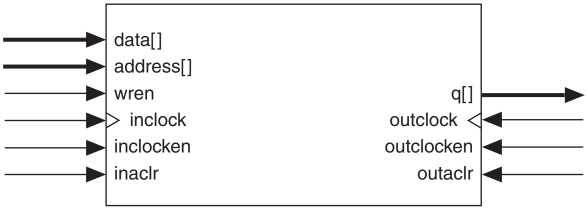
In addition to true dual-port memory, the M4K memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write. Single-port memory supports non-simultaneous reads and writes. Figure 2–13 shows these different M4K RAM memory port configurations.

Figure 2–13. Simple Dual-Port and Single-Port Memory Configurations

Simple Dual-Port Memory



Single-Port Memory *(1)*



Note to Figure 2–13:

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

The Cyclone memory architecture can implement fully synchronous RAM by registering both the input and output signals to the M4K RAM block. All M4K memory block inputs are registered, providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`wren`) signal derived from a global clock. In contrast, a circuit using asynchronous RAM must generate the RAM `wren` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `wren` is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

Table 2–4. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Table 2–9 shows the programmable delays for Cyclone devices.

Table 2–9. Cyclone Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Output pin delay	Increase delay to output pin

There are two paths in the IOE for a combinatorial input to reach the logic array. Each of the two paths can have a different delay. This allows you adjust delays from the pin to internal LE registers that reside in two different areas of the device. The designer sets the two combinatorial input delays by selecting different delays for two different paths under the **Decrease input delay to internal cells** logic option in the Quartus II software. When the input signal requires two different delays for the combinatorial input, the input register in the IOE is no longer available.

The IOE registers in Cyclone devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

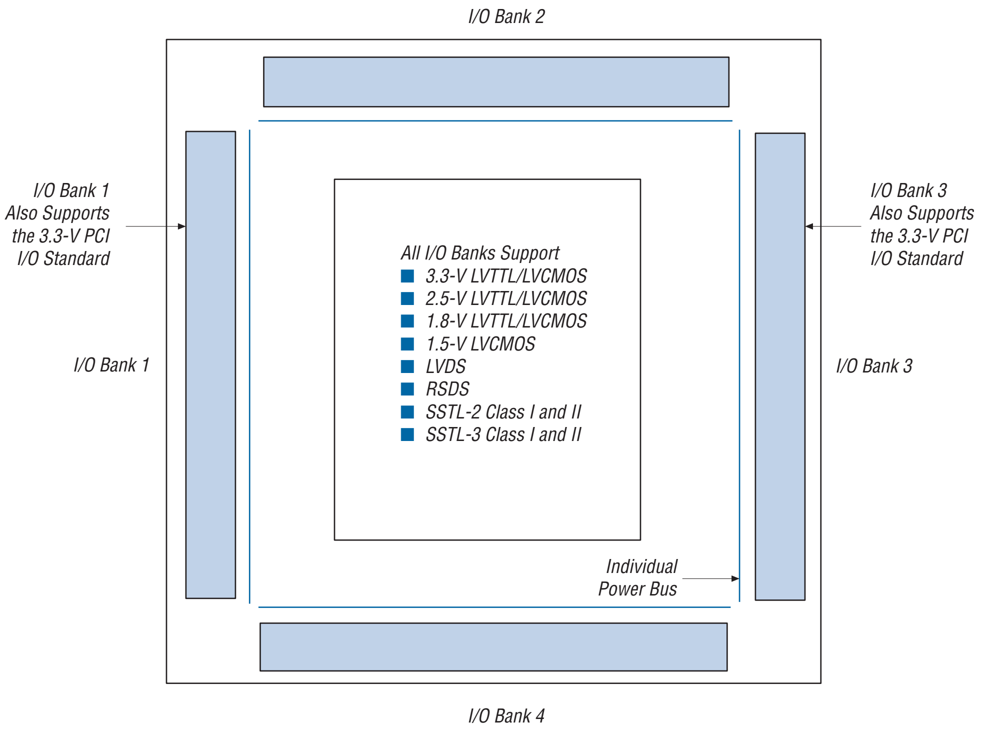
External RAM Interfacing

Cyclone devices support DDR SDRAM and FCRAM interfaces at up to 133 MHz through dedicated circuitry.

DDR SDRAM and FCRAM

Cyclone devices have dedicated circuitry for interfacing with DDR SDRAM. All I/O banks support DDR SDRAM and FCRAM I/O pins. However, the configuration input pins in bank 1 must operate at 2.5 V because the SSTL-2 V_{CCIO} level is 2.5 V. Additionally, the configuration and DM pins to support a DDR SDRAM or FCRAM interface. I/O bank 1 can also support a DDR SDRAM or FCRAM interface, however, the configuration input pins in I/O bank 1 must operate at 2.5 V. I/O bank 3 can also support a DDR SDRAM or FCRAM interface, however, all the JTAG pins in I/O bank 3 must operate at 2.5 V.

Figure 2–35. Cyclone I/O Banks *Notes (1), (2)*



Notes to Figure 2–35:

(1) Figure 2–35 is a top view of the silicon die.

(2) Figure 2–35 is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard with different I/O voltages. Each bank also has dual-purpose `VREF` pins to support any one of the voltage-referenced standards (e.g., SSTL-3) independently. If an I/O bank does not use voltage-referenced standards, the V_{REF} pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

Table 2–13. Cyclone Device LVDS Channels

Device	Pin Count	Number of LVDS Channels
EP1C3	100	*(1)*
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

Note to Table 2–13:

(1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and four sets for I/O output drivers (V_{CCIO}).

The Cyclone V_{CCINT} pins must always be connected to a 1.5-V power supply. If the V_{CCINT} level is 1.5 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The V_{CCIO} pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when V_{CCIO} pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V or 5.0-V systems. Table 2–14 summarizes Cyclone MultiVolt I/O support.

Table 2–14. Cyclone MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.5	✓	✓	✓ *(2)*	✓ *(2)*	—	✓	—	—	—	—
1.8	✓	✓	✓ *(2)*	✓ *(2)*	—	✓ *(3)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(5)*	✓ *(5)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(6)*	✓ *(7)*	✓ *(7)*	✓ *(7)*	✓	✓ *(8)*

Notes to Table 2–14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 1.5-V or 1.8-V and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected. Turn on **Allow voltage overdrive for LVTTL / LVCMOS input pins** in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combinations.

(3) When V_{CCIO} = 1.8-V, a Cyclone device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected.

(5) When V_{CCIO} = 2.5-V, a Cyclone device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(6) Cyclone devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.

(7) When V_{CCIO} = 3.3-V, a Cyclone device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(8) When V_{CCIO} = 3.3-V, a Cyclone device can drive a device with 5.0-V LVTTL inputs but not 5.0-V LVCMOS inputs.

Power Sequencing and Hot Socketing

Because Cyclone devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into Cyclone devices before and during power up without damaging the device. In addition, Cyclone devices do not drive out during power up. Once operating conditions are reached and the device is configured, Cyclone devices operate as specified by the user.

Referenced Documents

This chapter references the following document:

- *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*

Document Revision History

Table 2–15 shows the revision history for this chapter.

Table 2–15. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.6	Minor textual and style changes. Added "Referenced Documents" section.	—
January 2007 v1.5	● Added document revision history. ● Updated Figures 2–17, 2–18, 2–19, 2–20, 2–21, and 2–32.	—
August 2005 v1.4	Minor updates.	—
February 2005 v1.3	● Updated JTAG chain limits. Added test vector information. ● Corrected Figure 2-12. ● Added a note to Tables 2-17 through 2-21 regarding violating the setup or hold time.	—
October 2003 v1.2	● Updated phase shift information. ● Added 64-bit PCI support information.	—
September 2003 v1.1	Updated LVDS data rates to 640 Mbps from 311 Mbps.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

3. Configuration and Testing

C51003-1.4

IEEE Std. 1149.1 (JTAG) Boundary Scan Support

All Cyclone® devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Cyclone devices can also use the JTAG port for configuration together with either the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Cyclone devices support reconfiguring the I/O standard settings on the IOE through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode. Designers can use this ability for JTAG testing before configuration when some of the Cyclone pins drive or receive from other devices on the board using voltage-referenced standards. Since the Cyclone device might not be configured before JTAG testing, the I/O pins might not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows designers to fully test I/O connection to other devices.

The JTAG pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The TDO pin voltage is determined by the V_{CCIO} of the bank where it resides. The bank V_{CCIO} selects whether the JTAG inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Cyclone devices also use the JTAG port to monitor the operation of the device with the SignalTap® II embedded logic analyzer. Cyclone devices support the JTAG instructions shown in Table 3–1.

Table 3–1. Cyclone JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
`SAMPLE/PRELOAD`	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
`EXTEST` *(1)*	00 0000 0000	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
`BYPASS`	11 1111 1111	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA	—	0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1	—	V
		I_{OH} = –1 mA	2.0	—	V
		I_{OH} = –2 to –16 mA *(11)*	1.7	—	V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	—	0.2	V
		I_{OH} = 1 mA	—	0.4	V
		I_{OH} = 2 to 16 mA *(11)*	—	0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.65	1.95	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(12)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(11)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(11)*	—	0.45	V

Power Consumption

Designers can use the Altera web Early Power Estimator to estimate the device power.

Cyclone devices require a certain amount of power-up current to successfully power up because of the nature of the leading-edge process on which they are fabricated. Table 4–17 shows the maximum power-up current required to power up a Cyclone device.

Table 4–17. Cyclone Maximum Power-Up Current (I_{CCINT}) Requirements (In-Rush Current)

Device	Commercial Specification	Industrial Specification	Unit
EP1C3	150	180	mA
EP1C4	150	180	mA
EP1C6	175	210	mA
EP1C12	300	360	mA
EP1C20	500	600	mA

Notes to Table 4–17:

(1) The Cyclone devices (except for the EP1C20 device) meet the power up specification for Mini PCI.

(2) The lot codes 9G0082 to 9G2999, or 9G3109 and later comply to the specifications in Table 4–17 and meet the Mini PCI specification. Lot codes appear at the top of the device.

(3) The lot codes 9H0004 to 9H29999, or 9H3014 and later comply to the specifications in this table and meet the Mini PCI specification. Lot codes appear at the top of the device.

Designers should select power supplies and regulators that can supply this amount of current when designing with Cyclone devices. This specification is for commercial operating conditions. Measurements were performed with an isolated Cyclone device on the board. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$$I = C\,(dV/dt)$$

The exact amount of current that is consumed varies according to the process, temperature, and power ramp rate. If the power supply or regulator can supply more current than required, the Cyclone device may consume more current than the maximum current specified in Table 4–17. However, the device does not require any more current to successfully power up than what is listed in Table 4–17.

The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time. The power-up current consumption drops when the V_{CCINT} supply reaches approximately 0.75 V. For example, if the V_{CCINT} rise time has a linear rise of 15 ms, the current consumption spike drops by 7.5 ms.

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
M4K memory block	RAM 128 × 36 bit	Single port	—	4,608	1	256.00	222.67	197.01
	RAM 128 × 36 bit	Simple dual-port mode	—	4,608	1	255.95	222.67	196.97
	RAM 256 × 18 bit	True dual-port mode	—	4,608	1	255.95	222.67	196.97
	FIFO 128 × 36 bit	—	40	4,608	1	256.02	222.67	197.01
	Shift register 9 × 4 × 128	Shift register	11	4,536	1	255.95	222.67	196.97

Note to Table 4–20:

(1) The performance numbers for this function are from an EP1C6 device in a 240-pin PQFP package.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–21 through 4–24 describe the Cyclone device internal timing microparameters for LEs, IOEs, M4K memory structures, and MultiTrack interconnects.

Table 4–21. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–22. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	IOE input and output register setup time before clock
t_{H}	IOE input and output register hold time after clock
t_{CO}	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–23. M4K Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width

Table 4–29. Cyclone Global Clock External I/O Timing Parameters Notes (1), (2) (Part 2 of 2)

Symbol	Parameter	Conditions
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 4–29:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for IOE pins using a 3.3-V LVTTL, 24-mA setting. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–30 through 4–31 show the external timing parameters on column and row pins for EP1C3 devices.

Table 4–30. EP1C3 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.085	—	3.547	—	4.009	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	4.073	2.000	4.682	2.000	5.295	ns
$t_{INSUPLL}$	1.795	—	2.063	—	2.332	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	2.306	0.500	2.651	0.500	2.998	ns

Table 4–31. EP1C3 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.157	—	3.630	—	4.103	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.984	2.000	4.580	2.000	5.180	ns
$t_{INSUPLL}$	1.867	—	2.146	—	2.426	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	2.217	0.500	2.549	0.500	2.883	ns

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-3 class I	—	1,390	—	1,598	—	1,807	ps
SSTL-3 class II	—	989	—	1,137	—	1,285	ps
SSTL-2 class I	—	1,965	—	2,259	—	2,554	ps
SSTL-2 class II	—	1,692	—	1,945	—	2,199	ps
LVDS	—	802	—	922	—	1,042	ps

Note to Tables 4–40 through 4–45:

(1) EP1C3 devices do not support the PCI I/O standard.

Tables 4–46 through 4–47 show the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

Table 4–46. Cyclone IOE Programmable Delays on Column Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	155	—	178	—	201	ps
	Small	—	2,122	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	155	—	178	—	201	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	552	—	634	—	717	ps

Table 4–47. Cyclone IOE Programmable Delays on Row Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	154	—	177	—	200	ps
	Small	—	2,212	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	154	—	177	—	200	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	556	—	639	—	722	ps

Note to Table 4–47:

(1) EPC1C3 devices do not support the PCI I/O standard.

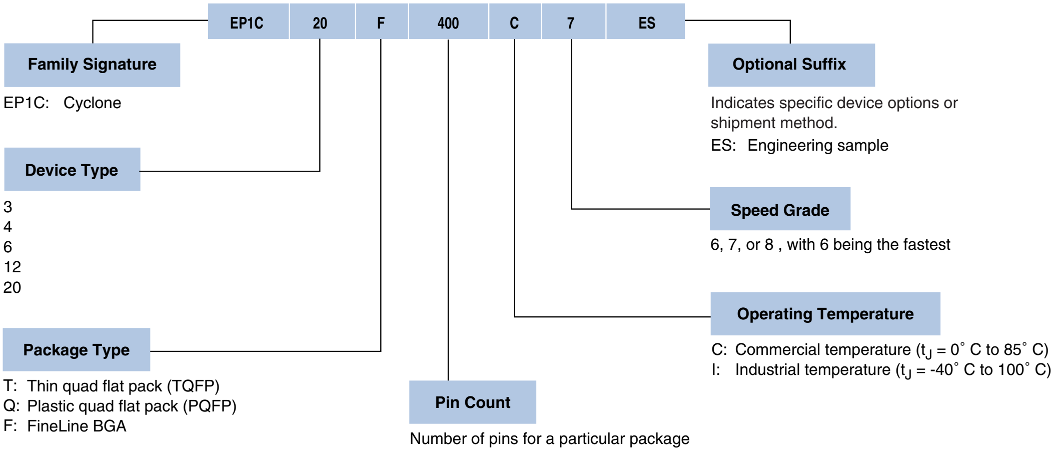
Maximum Input and Output Clock Rates

Tables 4–48 and 4–49 show the maximum input clock rate for column and row pins in Cyclone devices.

Table 4–48. Cyclone Maximum Input Clock Rate for Column Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVCMOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
LVDS	567	549	531	MHz

Figure 5–1. Cyclone Device Packaging Ordering Information



Referenced Documents

This chapter references the following documents:

- *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*
- *Quartus II Handbook*

Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added "Referenced Documents" section.	—
January 2007 v1.3	Added document revision history.	—
August 2005 v1.2	Minor updates.	—