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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2006
Number of Logic Elements/Cells	20060
Total RAM Bits	294912
Number of I/O	233
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c20f324c7">https://www.e-xfl.com/product-detail/intel/ep1c20f324c7</a>

### Functional Description

Cyclone® devices contain a two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varying speeds provide signal interconnects between LABs and embedded memory blocks.

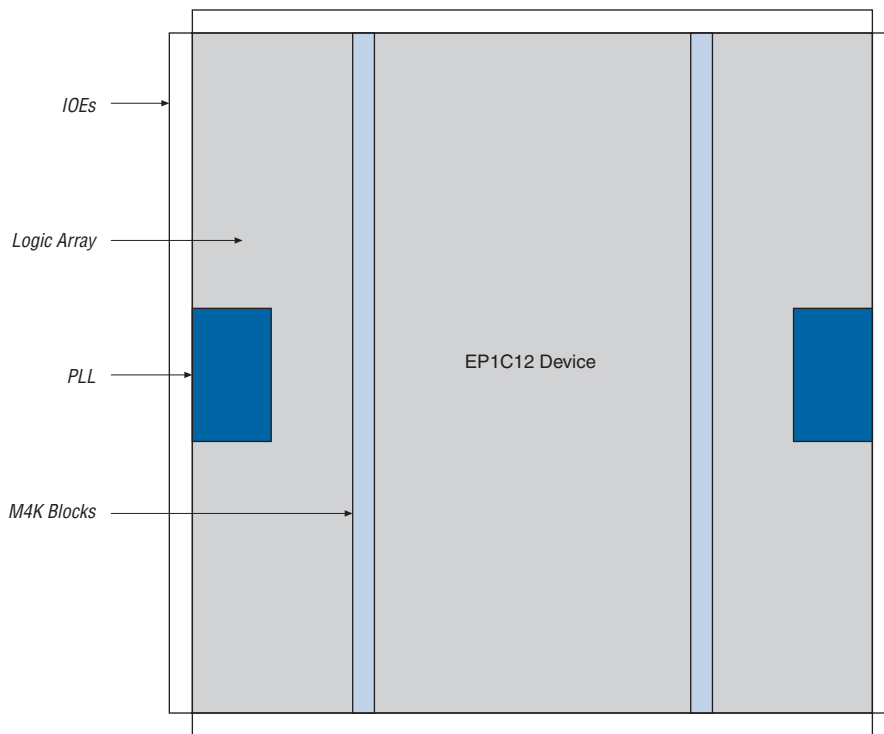
The logic array consists of LABs, with 10 LEs in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. Cyclone devices range between 2,910 to 20,060 LEs.

M4K RAM blocks are true dual-port memory blocks with 4K bits of memory plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 250 MHz. These blocks are grouped into columns across the device in between certain LABs. Cyclone devices offer between 60 to 288 Kbits of embedded RAM.

Each Cyclone device I/O pin is fed by an I/O element (IOE) located at the ends of LAB rows and columns around the periphery of the device. I/O pins support various single-ended and differential I/O standards, such as the 66- and 33-MHz, 64- and 32-bit PCI standard and the LVDS I/O standard at up to 640 Mbps. Each IOE contains a bidirectional I/O buffer and three registers for registering input, output, and output-enable signals. Dual-purpose DQS, DQ, and DM pins along with delay chains (used to phase-align DDR signals) provide interface support with external memory devices such as DDR SDRAM, and FCRAM devices at up to 133 MHz (266 Mbps).

Cyclone devices provide a global clock network and up to two PLLs. The global clock network consists of eight global clock lines that drive throughout the entire device. The global clock network can provide clocks for all resources within the device, such as IOEs, LEs, and memory blocks. The global clock lines can also be used for control signals. Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as external outputs for high-speed differential I/O support.

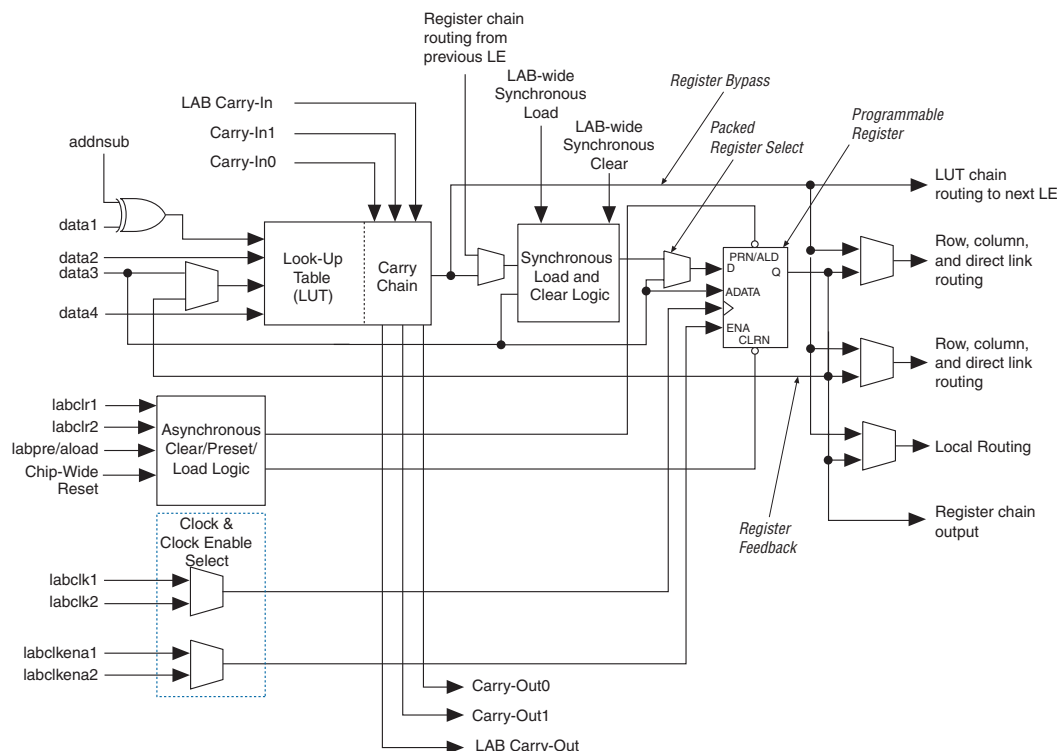
Figure 2–1 shows a diagram of the Cyclone EP1C12 device.

**Figure 2–1. Cyclone EP1C12 Device Block Diagram**

The number of M4K RAM blocks, PLLs, rows, and columns vary per device. [Table 2–1](#) lists the resources available in each Cyclone device.

**Table 2–1. Cyclone Device Resources**

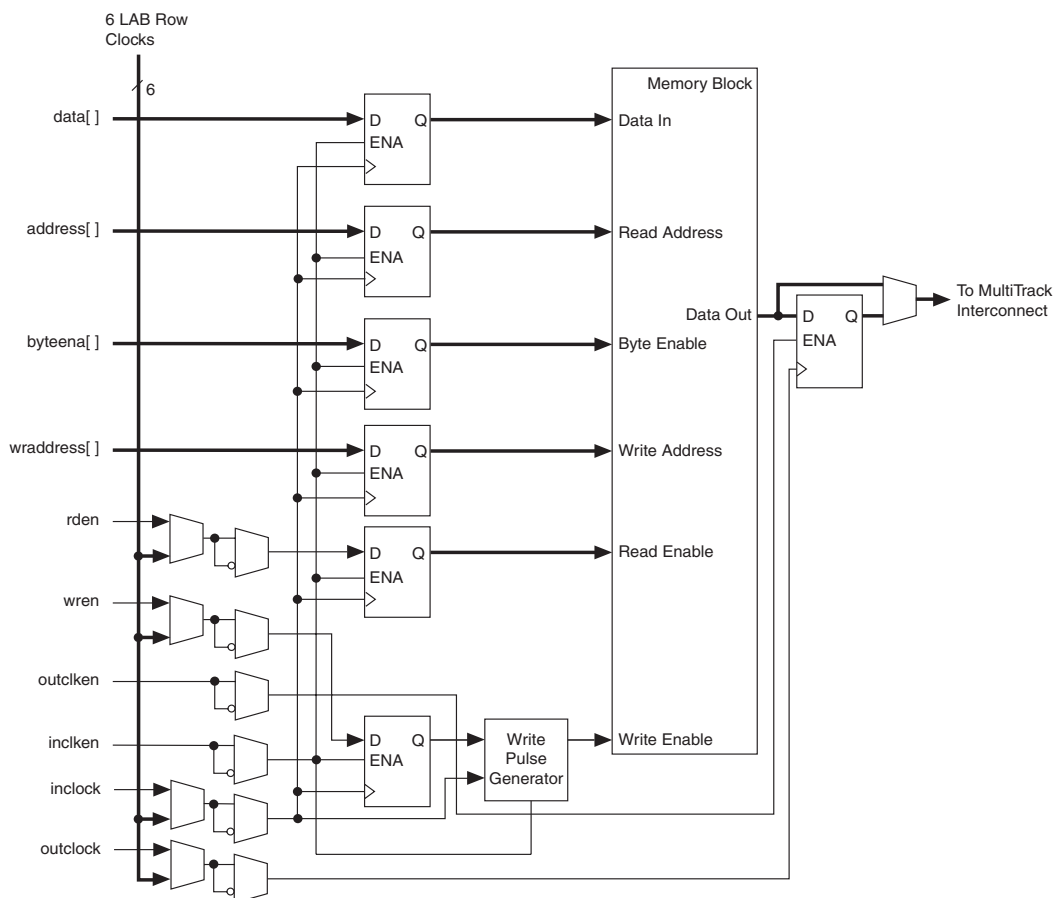
Device	M4K RAM		PLLs	LAB Columns	LAB Rows
	Columns	Blocks			
EP1C3	1	13	1	24	13
EP1C4	1	17	2	26	17
EP1C6	1	20	2	32	20
EP1C12	2	52	2	48	26
EP1C20	2	64	2	64	32

**Figure 2–5. Cyclone LE**

Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the data3 input of the LE. For combinatorial functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated

**Figure 2–19. Input/Output Clock Mode in Simple Dual-Port Mode** *Notes (1), (2)*

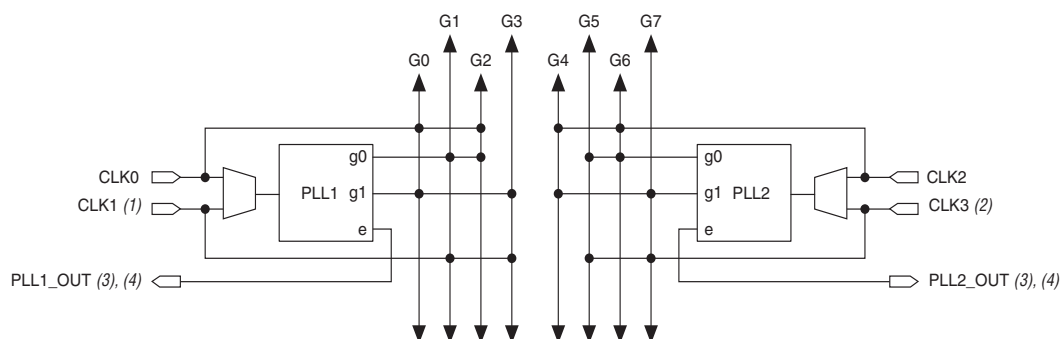


**Notes to Figure 2–19:**

- (1) All registers shown except the rden register have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Figure 2–26 shows the PLL global clock connections.

**Figure 2–26. Cyclone PLL Global Clock Connections**



**Notes to Figure 2–26:**

- (1) PLL 1 supports one single-ended or LVDS input via pins CLK0 and CLK1.
- (2) PLL2 supports one single-ended or LVDS input via pins CLK2 and CLK3.
- (3) PLL1\_OUT and PLL2\_OUT support single-ended or LVDS output. If external output is not required, these pins are available as regular user I/O pins.
- (4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Table 2–7 shows the global clock network sources available in Cyclone devices.

**Table 2–7. Global Clock Network Sources (Part 1 of 2)**

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
PLL Counter Output	PLL1 G0	—	✓	✓	—	—	—	—	—
	PLL1 G1	✓	—	—	✓	—	—	—	—
	PLL2 G0 (1)	—	—	—	—	—	✓	✓	—
	PLL2 G1 (1)	—	—	—	—	✓	—	—	✓
Dedicated Clock Input Pins	CLK0	✓	—	✓	—	—	—	—	—
	CLK1 (2)	—	✓	—	✓	—	—	—	—
	CLK2	—	—	—	—	✓	—	✓	—
	CLK3 (2)	—	—	—	—	—	✓	—	✓

does not have dedicated clock output pins. The EP1C6 device in the 144-pin TQFP package only supports dedicated clock outputs from PLL 1.

## Clock Feedback

Cyclone PLLs have three modes for multiplication and/or phase shifting:

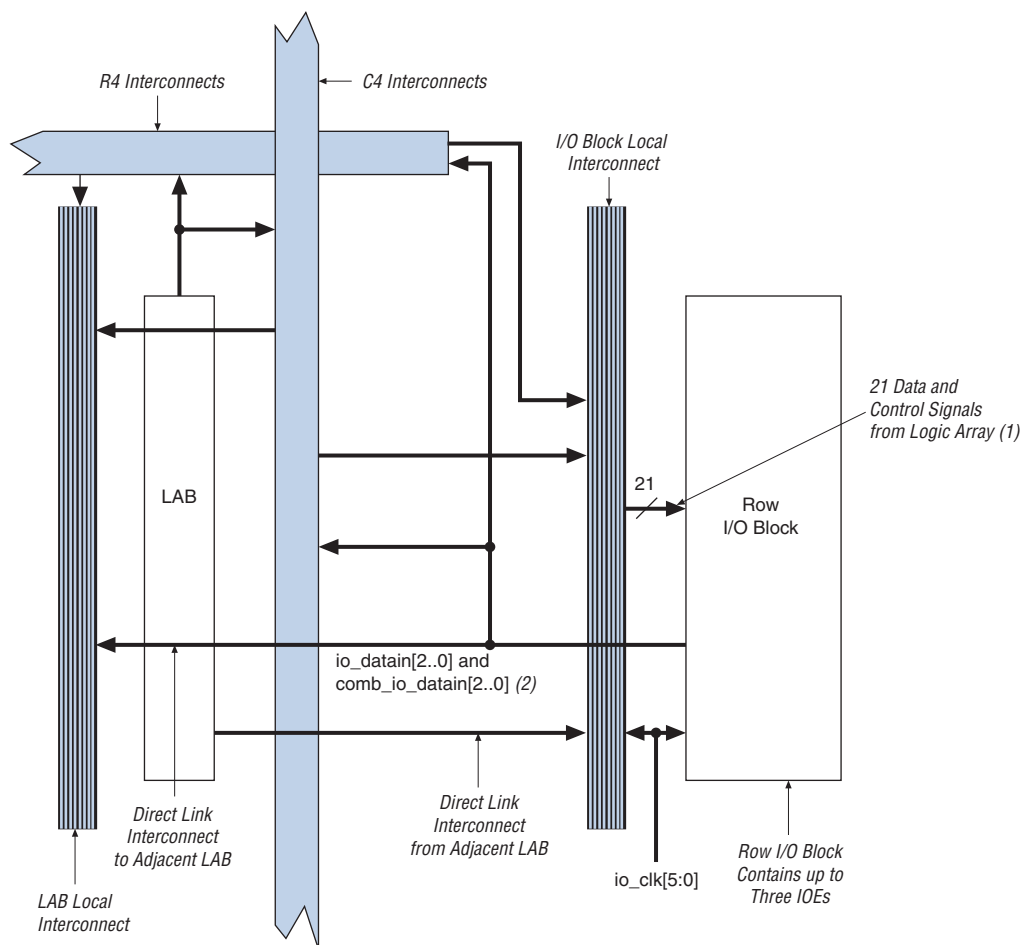
- Zero delay buffer mode—The external clock output pin is phase-aligned with the clock input pin for zero delay.
- Normal mode—If the design uses an internal PLL clock output, the normal mode compensates for the internal clock delay from the input clock pin to the IOE registers. The external clock output pin is phase shifted with respect to the clock input pin if connected in this mode. You defines which internal clock output from the PLL should be phase-aligned to compensate for internal clock delay.
- No compensation mode—In this mode, the PLL will not compensate for any clock networks.

## Phase Shifting

Cyclone PLLs have an advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 125 to 250 ps. The finest resolution equals one eighth of the VCO period. The VCO period is a function of the frequency input and the multiplication and division factors. Each clock output counter can choose a different phase of the VCO period from up to eight taps. You can use this clock output counter along with an initial setting on the post-scale counter to achieve a phase-shift range for the entire period of the output clock. The phase tap feedback to the m counter can shift all outputs to a single phase. The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entered.

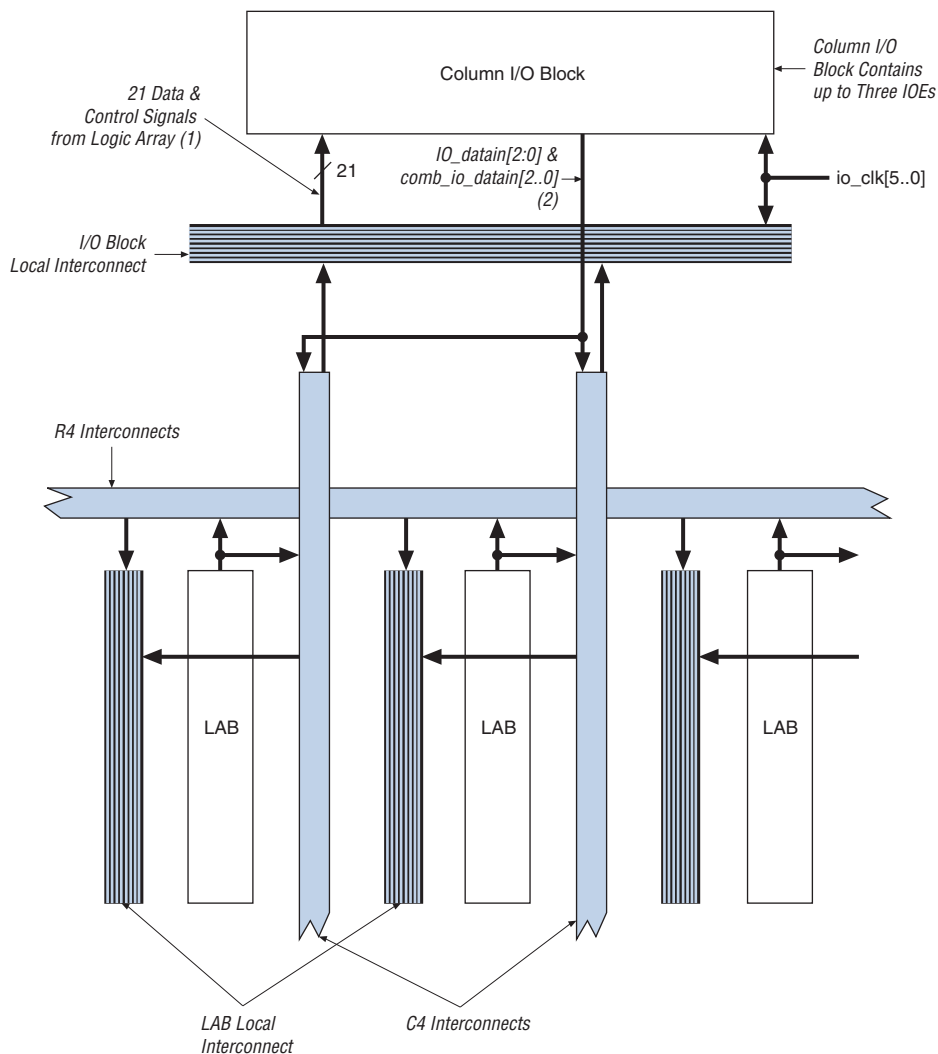
## Lock Detect Signal

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. Therefore, you may need to gate the lock signal for use as a system-control signal. For correct operation of the lock circuit below  $-20^{\circ}\text{C}$ ,  $f_{\text{IN}/N} > 200\text{ MHz}$ .

**Figure 2–28. Row I/O Block Connection to the Interconnect****Notes to Figure 2–28:**

- (1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_clk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.
- (2) Each of the three IOEs in the row I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.



**Figure 2–29. Column I/O Block Connection to the Interconnect****Notes to Figure 2–29:**

- (1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.
- (2) Each of the three IOEs in the column I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Table 2–9 shows the programmable delays for Cyclone devices.

<b>Table 2–9. Cyclone Programmable Delay Chain</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to logic array delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Output pin delay	Increase delay to output pin

There are two paths in the IOE for a combinatorial input to reach the logic array. Each of the two paths can have a different delay. This allows you adjust delays from the pin to internal LE registers that reside in two different areas of the device. The designer sets the two combinatorial input delays by selecting different delays for two different paths under the **Decrease input delay to internal cells** logic option in the Quartus II software. When the input signal requires two different delays for the combinatorial input, the input register in the IOE is no longer available.

The IOE registers in Cyclone devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

## External RAM Interfacing

Cyclone devices support DDR SDRAM and FCRAM interfaces at up to 133 MHz through dedicated circuitry.

## DDR SDRAM and FCRAM

Cyclone devices have dedicated circuitry for interfacing with DDR SDRAM. All I/O banks support DDR SDRAM and FCRAM I/O pins. However, the configuration input pins in bank 1 must operate at 2.5 V because the SSTL-2  $V_{CCIO}$  level is 2.5 V. Additionally, the configuration

## Advanced I/O Standard Support

Cyclone device IOEs support the following I/O standards:

- 3.3-V LVTTTL/LVCMOS
- 2.5-V LVTTTL/LVCMOS
- 1.8-V LVTTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- LVDS
- RSDS
- SSTL-2 class I and II
- SSTL-3 class I and II
- Differential SSTL-2 class II (on output clocks only)

Table 2–12 describes the I/O standards supported by Cyclone devices.

<b>I/O Standard</b>	<b>Type</b>	<b>Input Reference Voltage (<math>V_{REF}</math>) (V)</b>	<b>Output Supply Voltage (<math>V_{CCIO}</math>) (V)</b>	<b>Board Termination Voltage (<math>V_{TT}</math>) (V)</b>
3.3-V LVTTTL/LVCMOS	Single-ended	N/A	3.3	N/A
2.5-V LVTTTL/LVCMOS	Single-ended	N/A	2.5	N/A
1.8-V LVTTTL/LVCMOS	Single-ended	N/A	1.8	N/A
1.5-V LVCMOS	Single-ended	N/A	1.5	N/A
3.3-V PCI (1)	Single-ended	N/A	3.3	N/A
LVDS (2)	Differential	N/A	2.5	N/A
RSDS (2)	Differential	N/A	2.5	N/A
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5
Differential SSTL-2 (3)	Differential	1.25	2.5	1.25

**Notes to Table 2–12:**

- (1) There is no megafunction support for EP1C3 devices for the PCI compiler. However, EP1C3 devices support PCI by using the LVTTTL 16-mA I/O standard and drive strength assignments in the Quartus II software. The device requires an external diode for PCI compliance.
- (2) EP1C3 devices in the 100-pin TQFP package do not support the LVDS and RSDS I/O standards.
- (3) This I/O standard is only available on output clock pins ( $PLL\_OUT$  pins). EP1C3 devices in the 100-pin package do not support this I/O standard as it does not have  $PLL\_OUT$  pins.

Cyclone devices contain four I/O banks, as shown in Figure 2–35. I/O banks 1 and 3 support all the I/O standards listed in Table 2–12. I/O banks 2 and 4 support all the I/O standards listed in Table 2–12 except the 3.3-V PCI standard. I/O banks 2 and 4 contain dual-purpose DQS, DQ,



**Table 4–10. 3.3-V PCI Specifications (Part 2 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>OH</sub>	High-level output voltage	I <sub>OUT</sub> = –500 µA	0.9 × V <sub>CCIO</sub>	—	—	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OUT</sub> = 1,500 µA	—	—	0.1 × V <sub>CCIO</sub>	V

**Table 4–11. SSTL-2 Class I Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>CCIO</sub>	Output supply voltage	—	2.375	2.5	2.625	V
V <sub>TT</sub>	Termination voltage	—	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	V
V <sub>REF</sub>	Reference voltage	—	1.15	1.25	1.35	V
V <sub>IH</sub>	High-level input voltage	—	V <sub>REF</sub> + 0.18	—	3.0	V
V <sub>IL</sub>	Low-level input voltage	—	–0.3	—	V <sub>REF</sub> – 0.18	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –8.1 mA (11)	V <sub>TT</sub> + 0.57	—	—	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 8.1 mA (11)	—	—	V <sub>TT</sub> – 0.57	V

**Table 4–12. SSTL-2 Class II Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>CCIO</sub>	Output supply voltage	—	2.3	2.5	2.7	V
V <sub>TT</sub>	Termination voltage	—	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	V
V <sub>REF</sub>	Reference voltage	—	1.15	1.25	1.35	V
V <sub>IH</sub>	High-level input voltage	—	V <sub>REF</sub> + 0.18	—	V <sub>CCIO</sub> + 0.3	V
V <sub>IL</sub>	Low-level input voltage	—	–0.3	—	V <sub>REF</sub> – 0.18	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –16.4 mA (11)	V <sub>TT</sub> + 0.76	—	—	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 16.4 mA (11)	—	—	V <sub>TT</sub> – 0.76	V

**Table 4–13. SSTL-3 Class I Specifications (Part 1 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>CCIO</sub>	Output supply voltage	—	3.0	3.3	3.6	V
V <sub>TT</sub>	Termination voltage	—	V <sub>REF</sub> – 0.05	V <sub>REF</sub>	V <sub>REF</sub> + 0.05	V

## Power Consumption

Designers can use the Altera web Early Power Estimator to estimate the device power.

Cyclone devices require a certain amount of power-up current to successfully power up because of the nature of the leading-edge process on which they are fabricated. Table 4–17 shows the maximum power-up current required to power up a Cyclone device.

**Table 4–17. Cyclone Maximum Power-Up Current ( $I_{CCINT}$ ) Requirements (In-Rush Current)**

Device	Commercial Specification	Industrial Specification	Unit
EP1C3	150	180	mA
EP1C4	150	180	mA
EP1C6	175	210	mA
EP1C12	300	360	mA
EP1C20	500	600	mA

**Notes to Table 4–17:**

- (1) The Cyclone devices (except for the EP1C20 device) meet the power up specification for Mini PCI.
- (2) The lot codes 9G0082 to 9G2999, or 9G3109 and later comply to the specifications in Table 4–17 and meet the Mini PCI specification. Lot codes appear at the top of the device.
- (3) The lot codes 9H0004 to 9H2999, or 9H3014 and later comply to the specifications in this table and meet the Mini PCI specification. Lot codes appear at the top of the device.

Designers should select power supplies and regulators that can supply this amount of current when designing with Cyclone devices. This specification is for commercial operating conditions. Measurements were performed with an isolated Cyclone device on the board. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$$I = C (dV/dt)$$

The exact amount of current that is consumed varies according to the process, temperature, and power ramp rate. If the power supply or regulator can supply more current than required, the Cyclone device may consume more current than the maximum current specified in Table 4–17. However, the device does not require any more current to successfully power up than what is listed in Table 4–17.

The duration of the  $I_{CCINT}$  power-up requirement depends on the  $V_{CCINT}$  voltage supply rise time. The power-up current consumption drops when the  $V_{CCINT}$  supply reaches approximately 0.75 V. For example, if the  $V_{CCINT}$  rise time has a linear rise of 15 ms, the current consumption spike drops by 7.5 ms.

## Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in [Table 4–19](#).

**Table 4–19. Clock Tree Maximum Performance Specification**

Parameter	Definition	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock tree $f_{\text{MAX}}$	Maximum frequency that the clock tree can support for clocking registered logic	—	—	405	—	—	320	—	—	275	MHz

[Table 4–20](#) shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

**Table 4–20. Cyclone Device Performance**

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
LE	16-to-1 multiplexer	—	21	—	—	405.00	320.00	275.00
	32-to-1 multiplexer	—	44	—	—	317.36	284.98	260.15
	16-bit counter	—	16	—	—	405.00	320.00	275.00
	64-bit counter (1)	—	66	—	—	208.99	181.98	160.75

**Table 4–20. Cyclone Device Performance**

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
M4K memory block	RAM 128 × 36 bit	Single port	—	4,608	1	256.00	222.67	197.01
	RAM 128 × 36 bit	Simple dual-port mode	—	4,608	1	255.95	222.67	196.97
	RAM 256 × 18 bit	True dual-port mode	—	4,608	1	255.95	222.67	196.97
	FIFO 128 × 36 bit	—	40	4,608	1	256.02	222.67	197.01
	Shift register 9 × 4 × 128	Shift register	11	4,536	1	255.95	222.67	196.97

*Note to Table 4–20:*

(1) The performance numbers for this function are from an EP1C6 device in a 240-pin PQFP package.

## Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–21 through 4–24 describe the Cyclone device internal timing microparameters for LEs, IOEs, M4K memory structures, and MultiTrack interconnects.

**Table 4–21. LE Internal Timing Microparameter Descriptions**

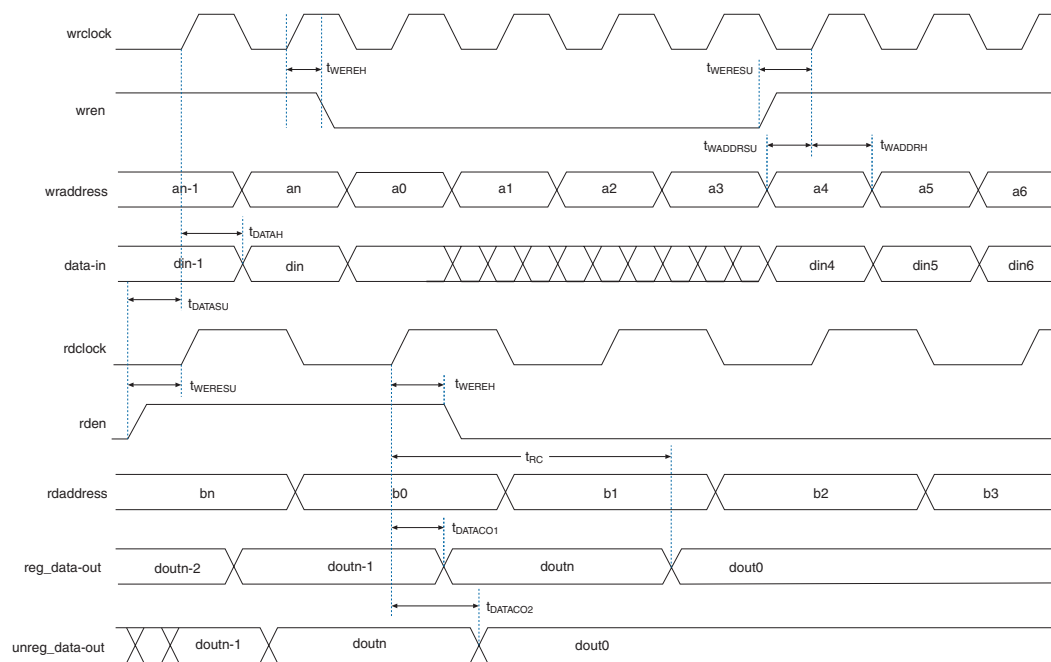
Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LE combinatorial LUT delay for data-in to data-out
$t_{CLR}$	Minimum clear pulse width
$t_{PRE}$	Minimum preset pulse width
$t_{CLKHL}$	Minimum clock high or low time



**Table 4–24. Routing Delay Internal Timing Microparameter Descriptions**

Symbol	Parameter
$t_{R4}$	Delay for an R4 line with average loading; covers a distance of four LAB columns
$t_{C4}$	Delay for an C4 line with average loading; covers a distance of four LAB rows
$t_{LOCAL}$	Local interconnect delay

Figure 4–1 shows the memory waveforms for the M4K timing parameters shown in Table 4–23.

**Figure 4–1. Dual-Port RAM Timing Microparameter Waveform**

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4-25 through 4-28 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

**Table 4-25. LE Internal Timing Microparameters**

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	29	—	33	—	37	—	ps
$t_H$	12	—	13	—	15	—	ps
$t_{CO}$	—	173	—	198	—	224	ps
$t_{LUT}$	—	454	—	522	—	590	ps
$t_{CLR}$	129	—	148	—	167	—	ps
$t_{PRE}$	129	—	148	—	167	—	ps
$t_{CLKHL}$	1,234	—	1,562	—	1,818	—	ps

**Table 4-26. IOE Internal Timing Microparameters**

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	348	—	400	—	452	—	ps
$t_H$	0	—	0	—	0	—	ps
$t_{CO}$	—	511	—	587	—	664	ps
$t_{PIN2COMBOUT\_R}$	—	1,130	—	1,299	—	1,469	ps
$t_{PIN2COMBOUT\_C}$	—	1,135	—	1,305	—	1,475	ps
$t_{COMBIN2PIN\_R}$	—	2,627	—	3,021	—	3,415	ps
$t_{COMBIN2PIN\_C}$	—	2,615	—	3,007	—	3,399	ps
$t_{CLR}$	280	—	322	—	364	—	ps
$t_{PRE}$	280	—	322	—	364	—	ps
$t_{CLKHL}$	1,234	—	1,562	—	1,818	—	ps

Tables 4–32 through 4–33 show the external timing parameters on column and row pins for EP1C4 devices.

**Table 4–32. EP1C4 Column Pin Global Clock External I/O Timing Parameters** *Note (1)*

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.471	—	2.841	—	3.210	—	ns
$t_{\text{INH}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCO}}$	2.000	3.937	2.000	4.526	2.000	5.119	ns
$t_{\text{INSUPLL}}$	1.471	—	1.690	—	1.910	—	ns
$t_{\text{INHPLL}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCOPLL}}$	0.500	2.080	0.500	2.392	0.500	2.705	ns

**Table 4–33. EP1C4 Row Pin Global Clock External I/O Timing Parameters** *Note (1)*

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.600	—	2.990	—	3.379	—	ns
$t_{\text{INH}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCO}}$	2.000	3.991	2.000	4.388	2.000	5.189	ns
$t_{\text{INSUPLL}}$	1.300	—	1.494	—	1.689	—	ns
$t_{\text{INHPLL}}$	0.000	—	0.000	—	0.000	—	ns
$t_{\text{OUTCOPLL}}$	0.500	2.234	0.500	2.569	0.500	2.905	ns

**Note to Tables 4–32 and 4–33:**

(1) Contact Altera Applications for EP1C4 device timing parameters.

**Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 2 of 2)**

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class II		–278	—	–320	—	–362	ps
LVDS		–261	—	–301	—	–340	ps

**Table 4–41. Cyclone I/O Standard Row Pin Input Delay Adders**

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVC MOS	—	0	—	0	—	0	ps
3.3-V LVTTTL	—	0	—	0	—	0	ps
2.5-V LVTTTL	—	27	—	31	—	35	ps
1.8-V LVTTTL	—	182	—	209	—	236	ps
1.5-V LVTTTL	—	278	—	319	—	361	ps
3.3-V PCI (1)	—	0	—	0	—	0	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps
SSTL-2 class II	—	–278	—	–320	—	–362	ps
LVDS	—	–261	—	–301	—	–340	ps

**Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVC MOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps

**Table 4–49. Cyclone Maximum Input Clock Rate for Row Pins**

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVCMOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
3.3-V PCI (1)	464	428	387	MHz
LVDS	567	549	531	MHz

Note to Tables 4–48 through 4–49:

- (1) EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

Tables 4–50 and 4–51 show the maximum output clock rate for column and row pins in Cyclone devices.

**Table 4–50. Cyclone Maximum Output Clock Rate for Column Pins**

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	304	304	304	MHz
2.5 V	220	220	220	MHz
1.8 V	213	213	213	MHz
1.5 V	166	166	166	MHz
LVCMOS	304	304	304	MHz
SSTL-3 class I	100	100	100	MHz
SSTL-3 class II	100	100	100	MHz
SSTL-2 class I	134	134	134	MHz
SSTL-2 class II	134	134	134	MHz
LVDS	320	320	275	MHz

Note to Table 4–50:

- (1) EP1C3 devices do not support the PCI I/O standard.