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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

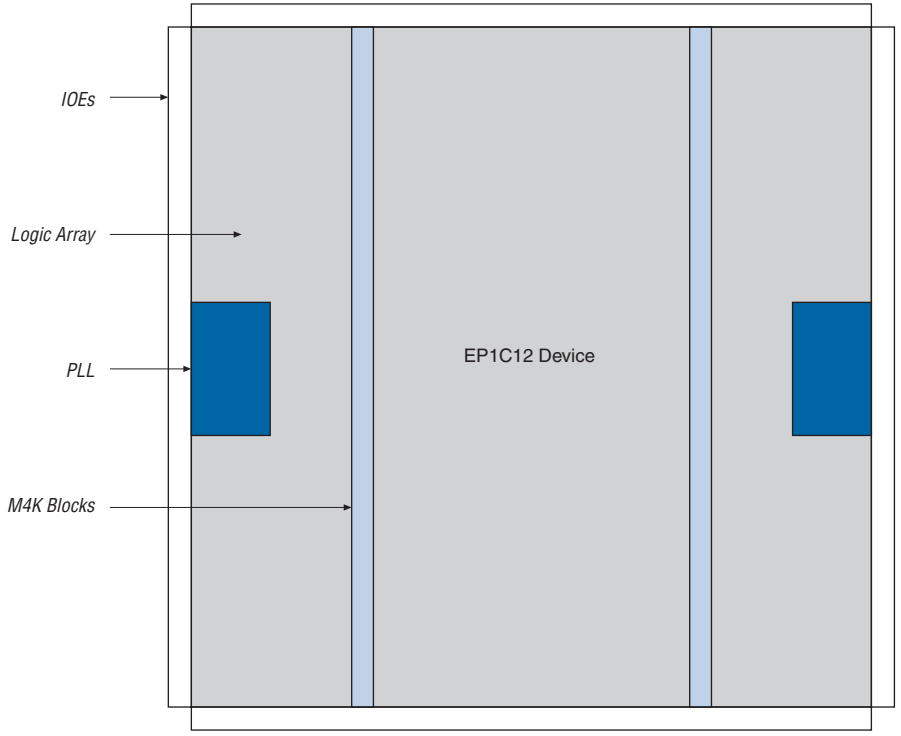
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2006 |
| Number of Logic Elements/Cells | 20060 |
| Total RAM Bits | 294912 |
| Number of I/O | 301 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 400-BGA |
| Supplier Device Package | 400-FBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1c20f400c6 |

*Figure 2–1. Cyclone EP1C12 Device Block Diagram*




The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

*Table 2–1. Cyclone Device Resources*

| Device | M4K RAM | | PLLs | LAB Columns | LAB Rows |
|---|---|---|---|---|---|
| | Columns | Blocks | | | |
| EP1C3 | 1 | 13 | 1 | 24 | 13 |
| EP1C4 | 1 | 17 | 2 | 26 | 17 |
| EP1C6 | 1 | 20 | 2 | 32 | 20 |
| EP1C12 | 2 | 52 | 2 | 48 | 26 |
| EP1C20 | 2 | 64 | 2 | 64 | 32 |

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to M4K memory blocks. A carry chain can continue as far as a full column.

### *Clear and Preset Logic Control*

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Cyclone devices support simultaneous preset/ asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Cyclone devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

## MultiTrack Interconnect

In the Cyclone architecture, connections between LEs, M4K memory blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when

migrating through different device densities. Dedicated row interconnects route signals to and from LABs, PLLs, and M4K memory blocks within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left

The direct link interconnect allows a LAB or M4K memory block to drive into the local interconnect of its left and right neighbors. Only one side of a PLL block interfaces with direct link and row interconnects. The direct link interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, or two LABs and one M4K RAM block. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–9 shows R4 interconnect connections from a LAB. R4 interconnects can drive and be driven by M4K memory blocks, PLLs, and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–2 shows the Cyclone device's routing scheme.

*Table 2–2. Cyclone Device Routing Scheme*

| Source | Destination | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | LUT Chain | Register Chain | Local Interconnect | Direct Link Interconnect | R4 Interconnect | C4 Interconnect | LE | M4K RAM Block | PLL | Column IOE | Row IOE |
| LUT Chain | — | — | — | — | — | — | ✓ | — | — | — | — |
| Register Chain | — | — | — | — | — | — | ✓ | — | — | — | — |
| Local Interconnect | — | — | — | — | — | — | ✓ | ✓ | ✓ | ✓ | ✓ |
| Direct Link Interconnect | — | — | ✓ | — | — | — | — | — | — | — | — |
| R4 Interconnect | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — |
| C4 Interconnect | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — |
| LE | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — | — | — |
| M4K RAM Block | — | — | ✓ | ✓ | ✓ | ✓ | — | — | — | — | — |
| PLL | — | — | — | ✓ | ✓ | ✓ | — | — | — | — | — |
| Column IOE | — | — | — | — | — | ✓ | — | — | — | — | — |
| Row IOE | — | — | — | ✓ | ✓ | ✓ | — | — | — | — | — |

is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

*Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)*

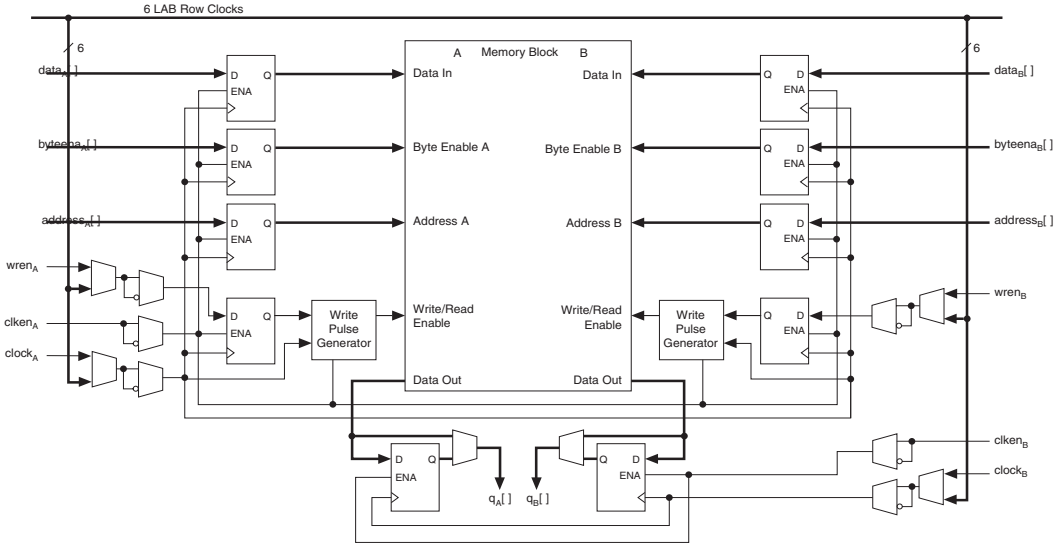
| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 4K × 1 | 2K × 2 | 1K × 4 | 512 × 8 | 256 × 16 | 128 × 32 | 512 × 9 | 256 × 18 | 128 × 36 |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 128 × 32 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 512 × 9 | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| 256 × 18 | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| 128 × 36 | — | — | — | — | — | — | ✓ | ✓ | ✓ |

*Table 2–4. M4K RAM Block Configurations (True Dual-Port)*

| Port A | Port B | | | | | | |
|---|---|---|---|---|---|---|---|
| | 4K × 1 | 2K × 2 | 1K × 4 | 512 × 8 | 256 × 16 | 512 × 9 | 256 × 18 |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | — | — |
| 512 × 9 | — | — | — | — | — | ✓ | ✓ |
| 256 × 18 | — | — | — | — | — | ✓ | ✓ |

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

*Figure 2–18. Input/Output Clock Mode in True Dual-Port Mode* *Notes (1), (2)*




*Notes to Figure 2–18:*

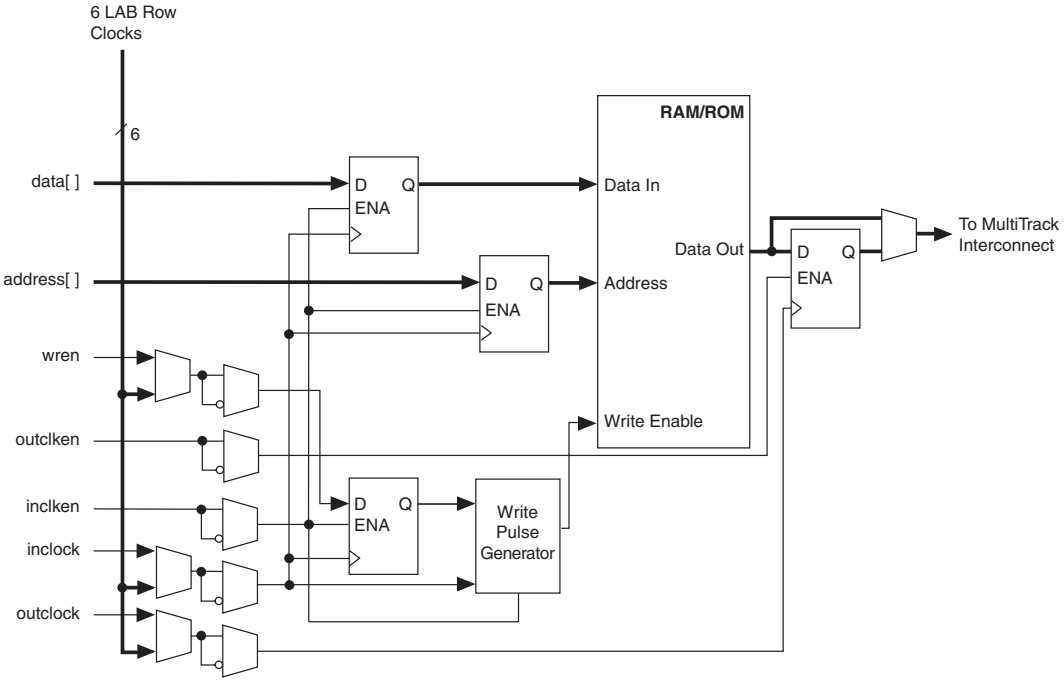
(1) All registers shown have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

### Single-Port Mode

The M4K memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–21. A single M4K memory block can support up to two single-port mode RAM blocks if each RAM block is less than or equal to 2K bits in size.

*Figure 2–21. Single-Port Mode* *Note (1)*




*Note to Figure 2–21:*

(1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

# Global Clock Network and Phase-Locked Loops

Cyclone devices provide a global clock network and up to two PLLs for a complete clock management solution.

### Global Clock Network

There are four dedicated clock pins (`CLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network, as shown in Figure 2–22. PLL outputs, logic array, and dual-purpose clock (`DPCLK[7..0]`) pins can also drive the global clock network.

Table 2–6 shows the PLL features in Cyclone devices. Figure 2–25 shows a Cyclone PLL.

*Table 2–6. Cyclone PLL Features*

| Feature | PLL Support |
|---|---|
| Clock multiplication and division | *m*/(*n* × post-scale counter) *(1)* |
| Phase shift | Down to 125-ps increments *(2)*, *(3)* |
| Programmable duty cycle | Yes |
| Number of internal clock outputs | 2 |
| Number of external clock outputs | One differential or one single-ended *(4)* |

***Notes to Table 2–6:***

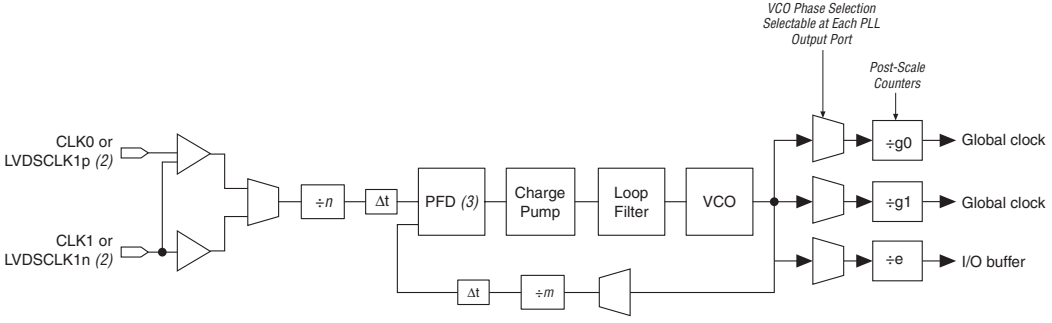
(1) The *m* counter ranges from 2 to 32. The *n* counter and the post-scale counters range from 1 to 32.

(2) The smallest phase shift is determined by the voltage-controlled oscillator (VCO) period divided by 8.

(3) For degree increments, Cyclone devices can shift all output frequencies in increments of 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

(4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

*Figure 2–25. Cyclone PLL* *Note (1)*




***Notes to Figure 2–25:***

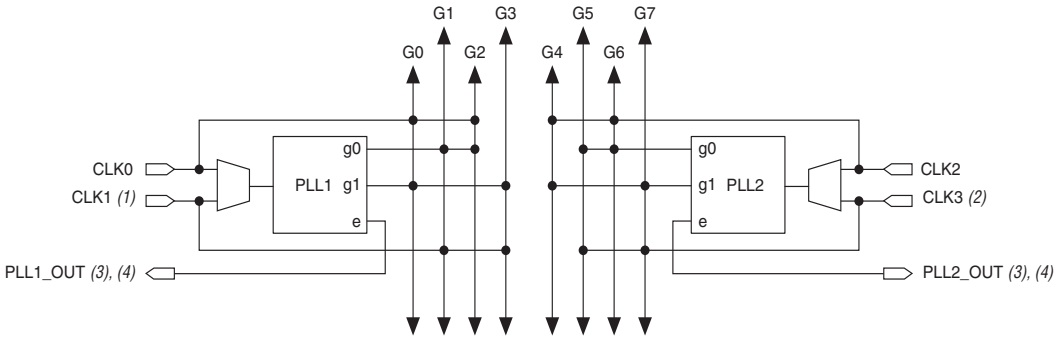
(1) The EP1C3 device in the 100-pin TQFP package does not support external outputs or LVDS inputs. The EP1C6 device in the 144-pin TQFP package does not support external output from PLL2.

(2) LVDS input is supported via the secondary function of the dedicated clock pins. For PLL 1, the `CLK0` pin's secondary function is `LVDSCLK1p` and the `CLK1` pin's secondary function is `LVDSCLK1n`. For PLL 2, the `CLK2` pin's secondary function is `LVDSCLK2p` and the `CLK3` pin's secondary function is `LVDSCLK2n`.

(3) PFD: phase frequency detector.

Figure 2–26 shows the PLL global clock connections.

*Figure 2–26. Cyclone PLL Global Clock Connections*




*Notes to Figure 2–26:*

(1) PLL 1 supports one single-ended or LVDS input via pins CLK0 and CLK1.

(2) PLL2 supports one single-ended or LVDS input via pins CLK2 and CLK3.

(3) PLL1_OUT and PLL2_OUT support single-ended or LVDS output. If external output is not required, these pins are available as regular user I/O pins.

(4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Table 2–7 shows the global clock network sources available in Cyclone devices.

*Table 2–7. Global Clock Network Sources (Part 1 of 2)*

| Source | | GCLK0 | GCLK1 | GCLK2 | GCLK3 | GCLK4 | GCLK5 | GCLK6 | GCLK7 |
|---|---|---|---|---|---|---|---|---|---|
| PLL Counter Output | PLL1 G0 | — | ✓ | ✓ | — | — | — | — | — |
| | PLL1 G1 | ✓ | — | — | ✓ | — | — | — | — |
| | PLL2 G0 *(1)* | — | — | — | — | — | ✓ | ✓ | — |
| | PLL2 G1 *(1)* | — | — | — | — | ✓ | — | — | ✓ |
| Dedicated Clock Input Pins | CLK0 | ✓ | — | ✓ | — | — | — | — | — |
| | CLK1 *(2)* | — | ✓ | — | ✓ | — | — | — | — |
| | CLK2 | — | — | — | — | ✓ | — | ✓ | — |
| | CLK3 *(2)* | — | — | — | — | — | ✓ | — | ✓ |

## Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

## Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Table 2–9 shows the programmable delays for Cyclone devices.

*Table 2–9. Cyclone Programmable Delay Chain*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input pin to logic array delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input registers |
| Output pin delay | Increase delay to output pin |

There are two paths in the IOE for a combinatorial input to reach the logic array. Each of the two paths can have a different delay. This allows you adjust delays from the pin to internal LE registers that reside in two different areas of the device. The designer sets the two combinatorial input delays by selecting different delays for two different paths under the **Decrease input delay to internal cells** logic option in the Quartus II software. When the input signal requires two different delays for the combinatorial input, the input register in the IOE is no longer available.

The IOE registers in Cyclone devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

## External RAM Interfacing

Cyclone devices support DDR SDRAM and FCRAM interfaces at up to 133 MHz through dedicated circuitry.

## DDR SDRAM and FCRAM

Cyclone devices have dedicated circuitry for interfacing with DDR SDRAM. All I/O banks support DDR SDRAM and FCRAM I/O pins. However, the configuration input pins in bank 1 must operate at 2.5 V because the SSTL-2 $V_{CCIO}$ level is 2.5 V. Additionally, the configuration

The Cyclone $V_{CCINT}$ pins must always be connected to a 1.5-V power supply. If the $V_{CCINT}$ level is 1.5 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The $V_{CCIO}$ pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when $V_{CCIO}$ pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When $V_{CCIO}$ pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V or 5.0-V systems. Table 2–14 summarizes Cyclone MultiVolt I/O support.

*Table 2–14. Cyclone MultiVolt I/O Support* *Note (1)*

| $V_{CCIO}$ (V) | Input Signal | | | | | Output Signal | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| 1.5 | ✓ | ✓ | ✓ (2) | ✓ (2) | — | ✓ | — | — | — | — |
| 1.8 | ✓ | ✓ | ✓ (2) | ✓ (2) | — | ✓ (3) | ✓ | — | — | — |
| 2.5 | — | — | ✓ | ✓ | — | ✓ (5) | ✓ (5) | ✓ | — | — |
| 3.3 | — | — | ✓ (4) | ✓ | ✓ (6) | ✓ (7) | ✓ (7) | ✓ (7) | ✓ | ✓ (8) |

*Notes to Table 2–14:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$.
(2) When $V_{CCIO}$ = 1.5-V or 1.8-V and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected. Turn on **Allow voltage overdrive for LVTTL / LVCMOS input pins** in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combinations.
(3) When $V_{CCIO}$ = 1.8-V, a Cyclone device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When $V_{CCIO}$ = 3.3-V and a 2.5-V input signal feeds an input pin, the $V_{CCIO}$ supply current will be slightly larger than expected.
(5) When $V_{CCIO}$ = 2.5-V, a Cyclone device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(6) Cyclone devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.
(7) When $V_{CCIO}$ = 3.3-V, a Cyclone device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
(8) When $V_{CCIO}$ = 3.3-V, a Cyclone device can drive a device with 5.0-V LVTTL inputs but not 5.0-V LVCMOS inputs.

## Power Sequencing and Hot Socketing

Because Cyclone devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the $V_{CCIO}$ and $V_{CCINT}$ power supplies may be powered in any order.

Signals can be driven into Cyclone devices before and during power up without damaging the device. In addition, Cyclone devices do not drive out during power up. Once operating conditions are reached and the device is configured, Cyclone devices operate as specified by the user.

The Cyclone device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone devices.

*Table 3–2. Cyclone Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP1C3 | 339 |
| EP1C4 | 930 |
| EP1C6 | 582 |
| EP1C12 | 774 |
| EP1C20 | 930 |

*Table 3–3. 32-Bit Cyclone Device IDCODE*

| Device | IDCODE (32 bits) *(1)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) *(2)* |
| EP1C3 | 0000 | 0010 0000 1000 0001 | 000 0110 1110 | 1 |
| EP1C4 | 0000 | 0010 0000 1000 0101 | 000 0110 1110 | 1 |
| EP1C6 | 0000 | 0010 0000 1000 0010 | 000 0110 1110 | 1 |
| EP1C12 | 0000 | 0010 0000 1000 0011 | 000 0110 1110 | 1 |
| EP1C20 | 0000 | 0010 0000 1000 0100 | 000 0110 1110 | 1 |

*Notes to Table 3–3:*

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

*Table 4–13. SSTL-3 Class I Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{REF}$ | Reference voltage | — | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | — | $V_{REF}$ + 0.2 | — | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | — | –0.3 | — | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(11)* | $V_{TT}$ + 0.6 | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(11)* | — | — | $V_{TT}$ – 0.6 | V |

*Table 4–14. SSTL-3 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | — | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | — | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | — | $V_{REF}$ + 0.2 | — | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | — | –0.3 | — | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16 mA *(11)* | $V_{TT}$ + 0.8 | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16 mA *(11)* | — | — | $V_{TT}$ – 0.8 | V |

*Table 4–15. Bus Hold Parameters*

| Parameter | Conditions | $V_{CCIO}$ Level | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.5 V | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $V_{IN} > V_{IL}$ (maximum) | — | — | 30 | — | 50 | — | 70 | — | µA |
| High sustaining current | $V_{IN} < V_{IH}$ (minimum) | — | — | –30 | — | –50 | — | –70 | — | µA |
| Low overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | — | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | — | — | –200 | — | –300 | — | –500 | µA |

| Table 4–22. IOE Internal Timing Microparameter Descriptions | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{SU}$ | IOE input and output register setup time before clock |
| $t_{H}$ | IOE input and output register hold time after clock |
| $t_{CO}$ | IOE input and output register clock-to-output delay |
| $t_{PIN2COMBOUT\_R}$ | Row input pin to IOE combinatorial output |
| $t_{PIN2COMBOUT\_C}$ | Column input pin to IOE combinatorial output |
| $t_{COMBIN2PIN\_R}$ | Row IOE data input to combinatorial output pin |
| $t_{COMBIN2PIN\_C}$ | Column IOE data input to combinatorial output pin |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{PRE}$ | Minimum preset pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

| Table 4–23. M4K Block Internal Timing Microparameter Descriptions | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{M4KRC}$ | Synchronous read cycle time |
| $t_{M4KWC}$ | Synchronous write cycle time |
| $t_{M4KWERESU}$ | Write or read enable setup time before clock |
| $t_{M4KWEREH}$ | Write or read enable hold time after clock |
| $t_{M4KBESU}$ | Byte enable setup time before clock |
| $t_{M4KBEH}$ | Byte enable hold time after clock |
| $t_{M4KDATAASU}$ | A port data setup time before clock |
| $t_{M4KDATAAH}$ | A port data hold time after clock |
| $t_{M4KADDRASU}$ | A port address setup time before clock |
| $t_{M4KADDRAH}$ | A port address hold time after clock |
| $t_{M4KDATABSU}$ | B port data setup time before clock |
| $t_{M4KDATABH}$ | B port data hold time after clock |
| $t_{M4KADDRBSU}$ | B port address setup time before clock |
| $t_{M4KADDRBH}$ | B port address hold time after clock |
| $t_{M4KDATACO1}$ | Clock-to-output delay when using output registers |
| $t_{M4KDATACO2}$ | Clock-to-output delay without output registers |
| $t_{M4KCLKHL}$ | Minimum clock high or low time |
| $t_{M4KCLR}$ | Minimum clear pulse width |

| Table 4–29. Cyclone Global Clock External I/O Timing Parameters Notes (1), (2) (Part 2 of 2) | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{OUTCOPLL}$ | Clock-to-output delay output or bidirectional pin using IOE output register with global clock enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |

*Notes to Table 4–29:*
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for IOE pins using a 3.3-V LVTTL, 24-mA setting. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–30 through 4–31 show the external timing parameters on column and row pins for EP1C3 devices.

**Table 4–30. EP1C3 Column Pin Global Clock External I/O Timing Parameters**

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.085 | — | 3.547 | — | 4.009 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 4.073 | 2.000 | 4.682 | 2.000 | 5.295 | ns |
| $t_{INSUPLL}$ | 1.795 | — | 2.063 | — | 2.332 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.306 | 0.500 | 2.651 | 0.500 | 2.998 | ns |

**Table 4–31. EP1C3 Row Pin Global Clock External I/O Timing Parameters**

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.157 | — | 3.630 | — | 4.103 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.984 | 2.000 | 4.580 | 2.000 | 5.180 | ns |
| $t_{INSUPLL}$ | 1.867 | — | 2.146 | — | 2.426 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.217 | 0.500 | 2.549 | 0.500 | 2.883 | ns |

| Table 4–39. EP1C20 Row Pin Global Clock External I/O Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.417 | — | 2.779 | — | 3.140 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.724 | 2.000 | 4.282 | 2.000 | 4.843 | ns |
| $t_{XZ}$ | — | 3.645 | — | 4.191 | — | 4.740 | ns |
| $t_{ZX}$ | — | 3.645 | — | 4.191 | — | 4.740 | ns |
| $t_{INSUPLL}$ | 1.417 | — | 1.629 | — | 1.840 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 1.667 | 0.500 | 1.917 | 0.500 | 2.169 | ns |
| $t_{XZPLL}$ | — | 1.588 | — | 1.826 | — | 2.066 | ns |
| $t_{ZXPLL}$ | — | 1.588 | — | 1.826 | — | 2.066 | ns |

## External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–40 through 4–45 show the adder delays associated with column and row I/O pins for all packages. If an I/O standard is selected other than LVTTL 4 mA with a fast slew rate, add the selected delay to the external $t_{CO}$ and $t_{SU}$ I/O parameters shown in Tables 4–25 through 4–28.

| Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 1 of 2) | | | | | | | |
|---|---|---|---|---|---|---|---|
| I/O Standard | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| LVCMOS | — | 0 | — | 0 | — | 0 | ps |
| 3.3-V LVTTL | — | 0 | — | 0 | — | 0 | ps |
| 2.5-V LVTTL | — | 27 | — | 31 | — | 35 | ps |
| 1.8-V LVTTL | — | 182 | — | 209 | — | 236 | ps |
| 1.5-V LVTTL | — | 278 | — | 319 | — | 361 | ps |
| SSTL-3 class I | — | –250 | — | –288 | — | –325 | ps |
| SSTL-3 class II | — | –250 | — | –288 | — | –325 | ps |
| SSTL-2 class I | — | –278 | — | –320 | — | –362 | ps |

| Table 4–49. Cyclone Maximum Input Clock Rate for Row Pins | | | | |
|---|---|---|---|---|
| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
| LVTTL | 464 | 428 | 387 | MHz |
| 2.5 V | 392 | 302 | 207 | MHz |
| 1.8 V | 387 | 311 | 252 | MHz |
| 1.5 V | 387 | 320 | 243 | MHz |
| LVCMOS | 405 | 374 | 333 | MHz |
| SSTL-3 class I | 405 | 356 | 293 | MHz |
| SSTL-3 class II | 414 | 365 | 302 | MHz |
| SSTL-2 class I | 464 | 428 | 396 | MHz |
| SSTL-2 class II | 473 | 432 | 396 | MHz |
| 3.3-V PCI *(1)* | 464 | 428 | 387 | MHz |
| LVDS | 567 | 549 | 531 | MHz |

***Note to Tables 4–48 through 4–49:***
(1) EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

Tables 4–50 and 4–51 show the maximum output clock rate for column and row pins in Cyclone devices.

| Table 4–50. Cyclone Maximum Output Clock Rate for Column Pins | | | | |
|---|---|---|---|---|
| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
| LVTTL | 304 | 304 | 304 | MHz |
| 2.5 V | 220 | 220 | 220 | MHz |
| 1.8 V | 213 | 213 | 213 | MHz |
| 1.5 V | 166 | 166 | 166 | MHz |
| LVCMOS | 304 | 304 | 304 | MHz |
| SSTL-3 class I | 100 | 100 | 100 | MHz |
| SSTL-3 class II | 100 | 100 | 100 | MHz |
| SSTL-2 class I | 134 | 134 | 134 | MHz |
| SSTL-2 class II | 134 | 134 | 134 | MHz |
| LVDS | 320 | 320 | 275 | MHz |

***Note to Table 4–50:***
(1) EP1C3 devices do not support the PCI I/O standard.

| | | |
|---|---|---|
| February 2005<br>v1.1 | Updated Figure 5-1. | — |
| May 2003<br>v1.0 | Added document to Cyclone Device Handbook. | — |