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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2006
Number of Logic Elements/Cells	20060
Total RAM Bits	294912
Number of I/O	301
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c20f400c7n">https://www.e-xfl.com/product-detail/intel/ep1c20f400c7n</a>

## Introduction

The Cyclone® field programmable gate array family is based on a 1.5-V, 0.13-μm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 Kbits of RAM. With features like phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements, Cyclone devices are a cost-effective solution for data-path applications. Cyclone devices support various I/O standards, including LVDS at data rates up to 640 megabits per second (Mbps), and 66- and 33-MHz, 64- and 32-bit peripheral component interconnect (PCI), for interfacing with and supporting ASSP and ASIC devices. Altera also offers new low-cost serial configuration devices to configure Cyclone devices.

## Features

The Cyclone device family offers the following features:

- 2,910 to 20,060 LEs, see [Table 1–1](#)
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66- and 33-MHz, 64- and 32-bit PCI standard
- High-speed (640 Mbps) LVDS I/O support
- Low-speed (311 Mbps) LVDS I/O support
- 311-Mbps RSDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz), FCRAM, and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) cores, including Altera® MegaCore® functions and Altera Megafunctions Partners Program (AMPP<sup>SM</sup>) megafunctions.

**Table 1–1. Cyclone Device Features (Part 1 of 2)**

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
LEs	2,910	4,000	5,980	12,060	20,060
M4K RAM blocks (128 × 36 bits)	13	17	20	52	64

### Functional Description

Cyclone® devices contain a two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varying speeds provide signal interconnects between LABs and embedded memory blocks.

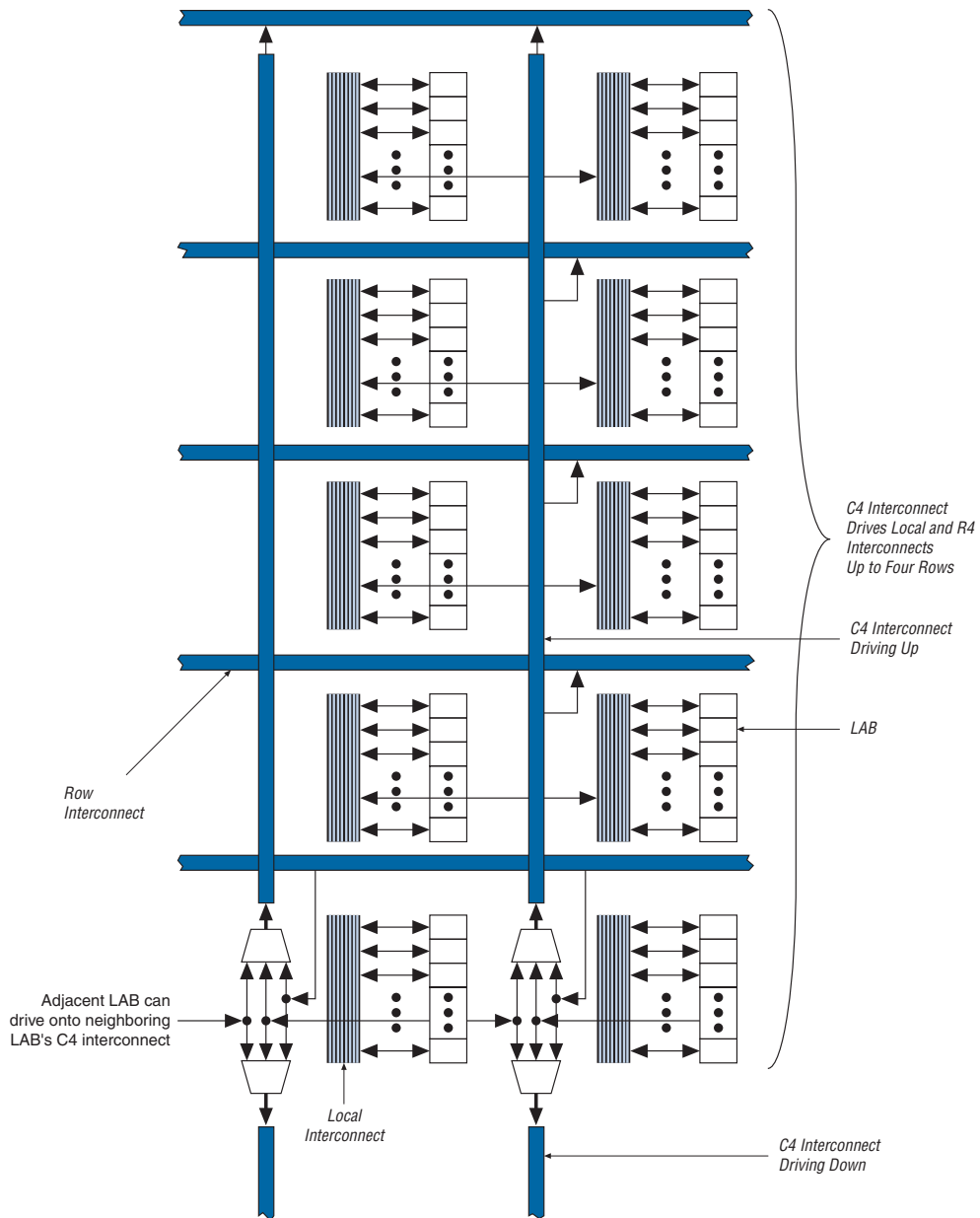
The logic array consists of LABs, with 10 LEs in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. Cyclone devices range between 2,910 to 20,060 LEs.

M4K RAM blocks are true dual-port memory blocks with 4K bits of memory plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 250 MHz. These blocks are grouped into columns across the device in between certain LABs. Cyclone devices offer between 60 to 288 Kbits of embedded RAM.

Each Cyclone device I/O pin is fed by an I/O element (IOE) located at the ends of LAB rows and columns around the periphery of the device. I/O pins support various single-ended and differential I/O standards, such as the 66- and 33-MHz, 64- and 32-bit PCI standard and the LVDS I/O standard at up to 640 Mbps. Each IOE contains a bidirectional I/O buffer and three registers for registering input, output, and output-enable signals. Dual-purpose DQS, DQ, and DM pins along with delay chains (used to phase-align DDR signals) provide interface support with external memory devices such as DDR SDRAM, and FCRAM devices at up to 133 MHz (266 Mbps).

Cyclone devices provide a global clock network and up to two PLLs. The global clock network consists of eight global clock lines that drive throughout the entire device. The global clock network can provide clocks for all resources within the device, such as IOEs, LEs, and memory blocks. The global clock lines can also be used for control signals. Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as external outputs for high-speed differential I/O support.

Figure 2–1 shows a diagram of the Cyclone EP1C12 device.

**Figure 2–11. C4 Interconnect Connections** *Note (1)***Note to Figure 2–11:**

(1) Each C4 interconnect can drive either up or down four rows.

signal. The output registers can be bypassed. Pseudo-asynchronous reading is possible in the simple dual-port mode of M4K blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple M4K memory blocks. For example, two 256×16-bit RAM blocks can be combined to form a 256×32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words allowed. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

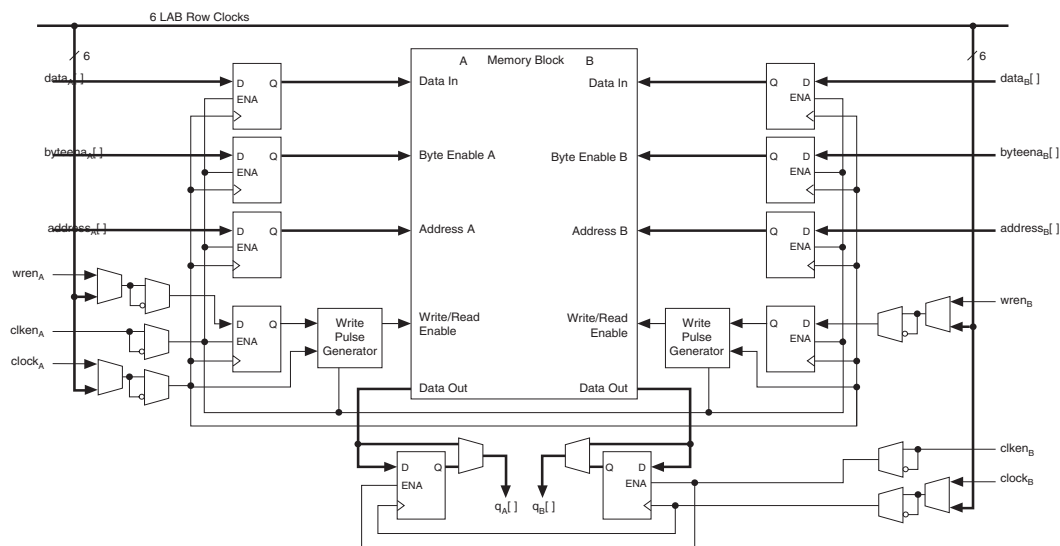
## Parity Bit Support

The M4K blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. Byte enables are also available for data input masking during write operations.

## Shift Register Support

You can configure M4K memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a  $w \times m \times n$  shift register is determined by the input data width ( $w$ ), the length of the taps ( $m$ ), and the number of taps ( $n$ ). The size of a  $w \times m \times n$  shift register must be less than or equal to the maximum number of memory bits in the M4K block (4,608 bits). The total number of shift

**Figure 2–18. Input/Output Clock Mode in True Dual-Port Mode** *Notes (1), (2)***Notes to Figure 2–18:**

- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

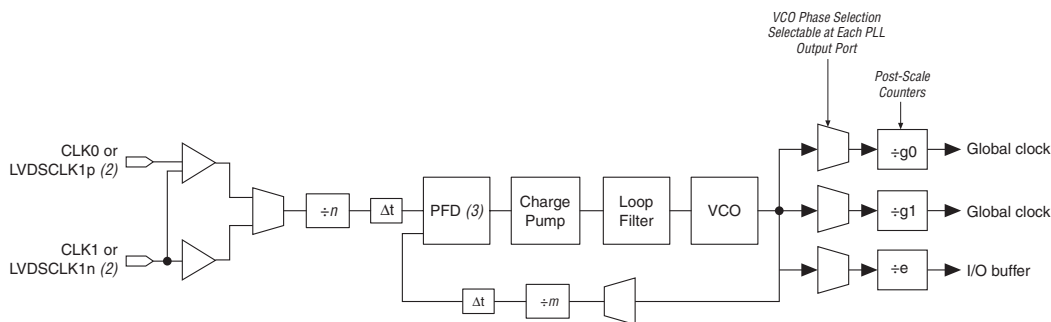
Table 2–6 shows the PLL features in Cyclone devices. Figure 2–25 shows a Cyclone PLL.

<b>Table 2–6. Cyclone PLL Features</b>	
<b>Feature</b>	<b>PLL Support</b>
Clock multiplication and division	$m/(n \times \text{post-scale counter})$ (1)
Phase shift	Down to 125-ps increments (2), (3)
Programmable duty cycle	Yes
Number of internal clock outputs	2
Number of external clock outputs	One differential or one single-ended (4)

**Notes to Table 2–6:**

- (1) The  $m$  counter ranges from 2 to 32. The  $n$  counter and the post-scale counters range from 1 to 32.
- (2) The smallest phase shift is determined by the voltage-controlled oscillator (VCO) period divided by 8.
- (3) For degree increments, Cyclone devices can shift all output frequencies in increments of 45°. Smaller degree increments are possible depending on the frequency and divide parameters.
- (4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

**Figure 2–25. Cyclone PLL**      *Note (1)*

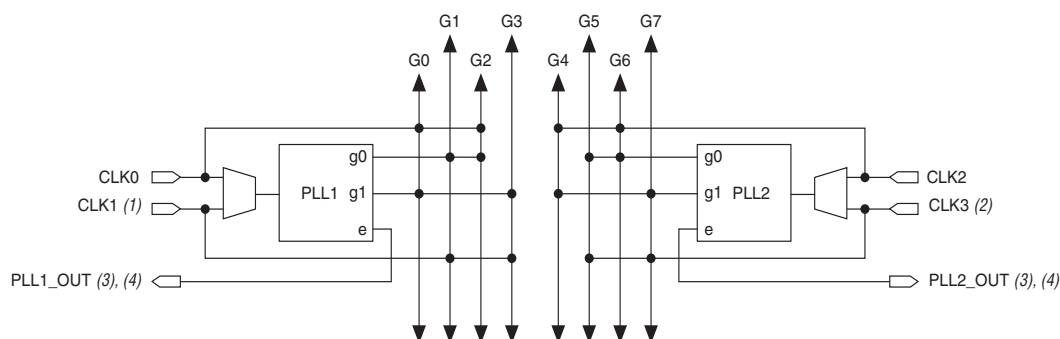


**Notes to Figure 2–25:**

- (1) The EP1C3 device in the 100-pin TQFP package does not support external outputs or LVDS inputs. The EP1C6 device in the 144-pin TQFP package does not support external output from PLL2.
- (2) LVDS input is supported via the secondary function of the dedicated clock pins. For PLL 1, the CLK0 pin's secondary function is LVDSCLK1p and the CLK1 pin's secondary function is LVDSCLK1n. For PLL 2, the CLK2 pin's secondary function is LVDSCLK2p and the CLK3 pin's secondary function is LVDSCLK2n.
- (3) PFD: phase frequency detector.

Figure 2–26 shows the PLL global clock connections.

**Figure 2–26. Cyclone PLL Global Clock Connections**



**Notes to Figure 2–26:**

- (1) PLL 1 supports one single-ended or LVDS input via pins CLK0 and CLK1.
- (2) PLL2 supports one single-ended or LVDS input via pins CLK2 and CLK3.
- (3) PLL1\_OUT and PLL2\_OUT support single-ended or LVDS output. If external output is not required, these pins are available as regular user I/O pins.
- (4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Table 2–7 shows the global clock network sources available in Cyclone devices.

**Table 2–7. Global Clock Network Sources (Part 1 of 2)**

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
PLL Counter Output	PLL1 G0	—	✓	✓	—	—	—	—	—
	PLL1 G1	✓	—	—	✓	—	—	—	—
	PLL2 G0 (1)	—	—	—	—	—	✓	✓	—
	PLL2 G1 (1)	—	—	—	—	✓	—	—	✓
Dedicated Clock Input Pins	CLK0	✓	—	✓	—	—	—	—	—
	CLK1 (2)	—	✓	—	✓	—	—	—	—
	CLK2	—	—	—	—	✓	—	✓	—
	CLK3 (2)	—	—	—	—	—	✓	—	✓



**Table 2–7. Global Clock Network Sources (Part 2 of 2)**

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
Dual-Purpose Clock Pins	DPCLK0 (3)	—	—	—	✓	—	—	—	—
	DPCLK1 (3)	—	—	✓	—	—	—	—	—
	DPCLK2	✓	—	—	—	—	—	—	—
	DPCLK3	—	—	—	—	✓	—	—	—
	DPCLK4	—	—	—	—	—	—	✓	—
	DPCLK5 (3)	—	—	—	—	—	—	—	✓
	DPCLK6	—	—	—	—	—	✓	—	—
	DPCLK7	—	✓	—	—	—	—	—	—

**Notes to Table 2–7:**

- (1) EP1C3 devices only have one PLL (PLL 1).
- (2) EP1C3 devices in the 100-pin TQFP package do not have dedicated clock pins CLK1 and CLK3.
- (3) EP1C3 devices in the 100-pin TQFP package do not have the DPCLK0, DPCLK1, or DPCLK5 pins.

## Clock Multiplication and Division

Cyclone PLLs provide clock synthesis for PLL output ports using  $m/(n \times \text{post scale counter})$  scaling factors. The input clock is divided by a pre-scale divider,  $n$ , and is then multiplied by the  $m$  feedback factor. The control loop drives the VCO to match  $f_{IN} \times (m/n)$ . Each output port has a unique post-scale counter to divide down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least-common multiple in the VCO's range).

Each PLL has one pre-scale divider,  $n$ , that can range in value from 1 to 32. Each PLL also has one multiply divider,  $m$ , that can range in value from 2 to 32. Global clock outputs have two post scale G dividers for global clock outputs, and external clock outputs have an E divider for external clock output, both ranging from 1 to 32. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

## External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (CLK[3..0]) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See [Figure 2-25](#).

[Table 2-8](#) shows the I/O standards supported by PLL input and output pins.

<b>Table 2-8. PLL I/O Standards</b>		
<b>I/O Standard</b>	<b>CLK Input</b>	<b>EXTCLK Output</b>
3.3-V LVTTTL/LVCMOS	✓	✓
2.5-V LVTTTL/LVCMOS	✓	✓
1.8-V LVTTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

For more information on LVDS I/O support, refer to “LVDS I/O Pins” on [page 2-54](#).

## External Clock Outputs

Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these PLL\_OUT pins, the pins are available for use as general-purpose I/O pins. The PLL\_OUT pins support all I/O standards shown in [Table 2-8](#).

The external clock outputs do not have their own V<sub>CC</sub> and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

does not have dedicated clock output pins. The EP1C6 device in the 144-pin TQFP package only supports dedicated clock outputs from PLL 1.

## Clock Feedback

Cyclone PLLs have three modes for multiplication and/or phase shifting:

- Zero delay buffer mode—The external clock output pin is phase-aligned with the clock input pin for zero delay.
- Normal mode—If the design uses an internal PLL clock output, the normal mode compensates for the internal clock delay from the input clock pin to the IOE registers. The external clock output pin is phase shifted with respect to the clock input pin if connected in this mode. You defines which internal clock output from the PLL should be phase-aligned to compensate for internal clock delay.
- No compensation mode—In this mode, the PLL will not compensate for any clock networks.

## Phase Shifting

Cyclone PLLs have an advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 125 to 250 ps. The finest resolution equals one eighth of the VCO period. The VCO period is a function of the frequency input and the multiplication and division factors. Each clock output counter can choose a different phase of the VCO period from up to eight taps. You can use this clock output counter along with an initial setting on the post-scale counter to achieve a phase-shift range for the entire period of the output clock. The phase tap feedback to the m counter can shift all outputs to a single phase. The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entered.

## Lock Detect Signal

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. Therefore, you may need to gate the lock signal for use as a system-control signal. For correct operation of the lock circuit below  $-20^{\circ}\text{C}$ ,  $f_{\text{IN}/N} > 200\text{ MHz}$ .

## Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

## Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.



For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

## I/O Structure

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

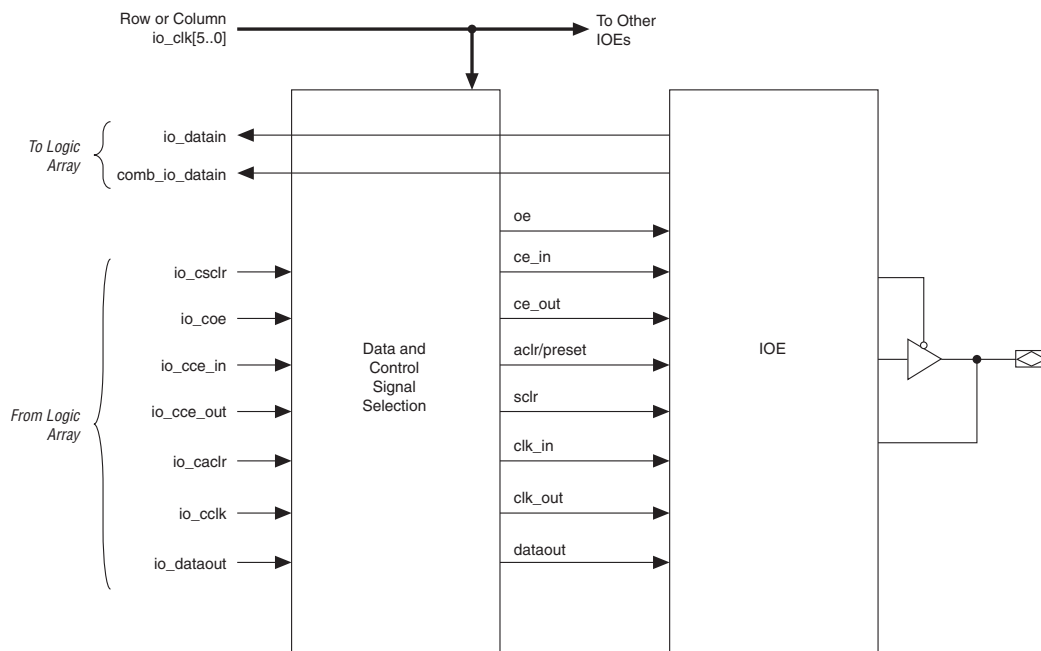
Cyclone device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer.

Figure 2–27 shows the Cyclone IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. IOEs can be used as input, output, or bidirectional pins.

The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, `io_clk[5..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see “Global Clock Network and Phase-Locked Loops” on page 2–29).

Figure 2–30 illustrates the signal paths through the I/O block.

**Figure 2–30. Signal Path through the I/O Block**



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 2–31 illustrates the control signal selection.

## Operating Modes

The Cyclone architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Cyclone devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to  $V_{CCIO}$  before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the  $V_{CCIO}$  of the bank where the pins reside. The bank  $V_{CCIO}$  selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

## Configuration Schemes

Designers can load the configuration data for a Cyclone device with one of three configuration schemes (see [Table 3–5](#)), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone device. A low-cost configuration device can automatically configure a Cyclone device at system power-up.

**Table 4–5. LVCMOS Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	3.0	3.6	V
$V_{IH}$	High-level input voltage	—	1.7	4.1	V
$V_{IL}$	Low-level input voltage	—	–0.5	0.7	V
$V_{OH}$	High-level output voltage	$V_{CCIO} = 3.0$ , $I_{OH} = -0.1$ mA	$V_{CCIO} - 0.2$	—	V
$V_{OL}$	Low-level output voltage	$V_{CCIO} = 3.0$ , $I_{OL} = 0.1$ mA	—	0.2	V

**Table 4–6. 2.5-V I/O Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	2.375	2.625	V
$V_{IH}$	High-level input voltage	—	1.7	4.1	V
$V_{IL}$	Low-level input voltage	—	–0.5	0.7	V
$V_{OH}$	High-level output voltage	$I_{OH} = -0.1$ mA	2.1	—	V
		$I_{OH} = -1$ mA	2.0	—	V
		$I_{OH} = -2$ to $-16$ mA (11)	1.7	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 0.1$ mA	—	0.2	V
		$I_{OH} = 1$ mA	—	0.4	V
		$I_{OH} = 2$ to $16$ mA (11)	—	0.7	V

**Table 4–7. 1.8-V I/O Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	1.65	1.95	V
$V_{IH}$	High-level input voltage	—	$0.65 \times V_{CCIO}$	2.25 (12)	V
$V_{IL}$	Low-level input voltage	—	–0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -2$ to $-8$ mA (11)	$V_{CCIO} - 0.45$	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2$ to $8$ mA (11)	—	0.45	V



Typically, the user-mode current during device operation is lower than the power-up current in Table 4–17. Altera recommends using the Cyclone Power Calculator, available on the Altera web site, to estimate the user-mode  $I_{CCINT}$  consumption and then select power supplies or regulators based on the higher value.

## Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

### Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–18 shows the status of the Cyclone device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

**Table 4–18. Cyclone Device Timing Model Status**

Device	Preliminary	Final
EP1C3	—	✓
EP1C4	—	✓
EP1C6	—	✓
EP1C12	—	✓
EP1C20	—	✓

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4-25 through 4-28 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

**Table 4-25. LE Internal Timing Microparameters**

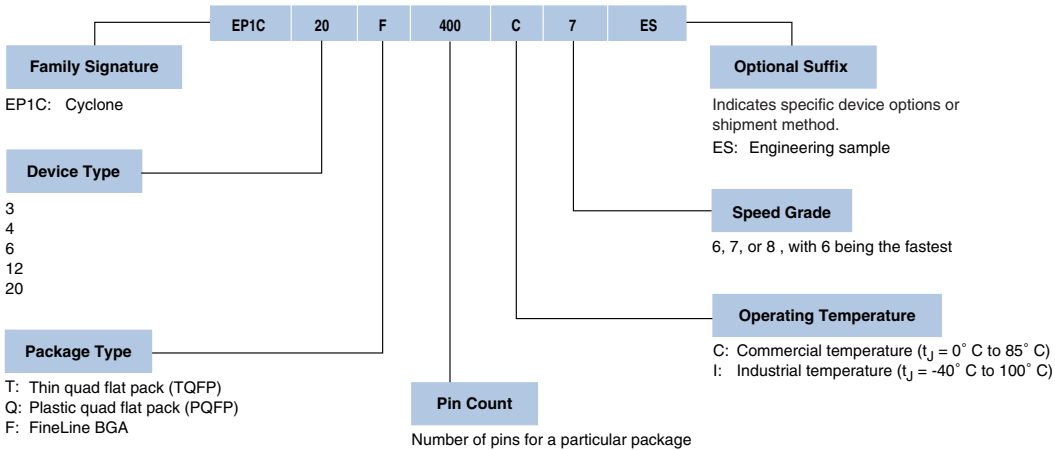
Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	29	—	33	—	37	—	ps
$t_H$	12	—	13	—	15	—	ps
$t_{CO}$	—	173	—	198	—	224	ps
$t_{LUT}$	—	454	—	522	—	590	ps
$t_{CLR}$	129	—	148	—	167	—	ps
$t_{PRE}$	129	—	148	—	167	—	ps
$t_{CLKHL}$	1,234	—	1,562	—	1,818	—	ps

**Table 4-26. IOE Internal Timing Microparameters**

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	348	—	400	—	452	—	ps
$t_H$	0	—	0	—	0	—	ps
$t_{CO}$	—	511	—	587	—	664	ps
$t_{PIN2COMBOUT\_R}$	—	1,130	—	1,299	—	1,469	ps
$t_{PIN2COMBOUT\_C}$	—	1,135	—	1,305	—	1,475	ps
$t_{COMBIN2PIN\_R}$	—	2,627	—	3,021	—	3,415	ps
$t_{COMBIN2PIN\_C}$	—	2,615	—	3,007	—	3,399	ps
$t_{CLR}$	280	—	322	—	364	—	ps
$t_{PRE}$	280	—	322	—	364	—	ps
$t_{CLKHL}$	1,234	—	1,562	—	1,818	—	ps

July 2003 v1.1	Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Figure 5–1. Cyclone Device Packaging Ordering Information



## Referenced Documents

This chapter references the following documents:

- *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*
- *Quartus II Handbook*

## Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History		
Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added “Referenced Documents” section.	—
January 2007 v1.3	Added document revision history.	—
August 2005 v1.2	Minor updates.	—

