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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2006
Number of Logic Elements/Cells	20060
Total RAM Bits	294912
Number of I/O	301
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c20f400i7">https://www.e-xfl.com/product-detail/intel/ep1c20f400i7</a>

to the appropriate plane on the board. The Quartus II software reserves I/O pins as power pins as necessary for layout with the larger densities in the same package having more power pins.

**Table 1–3. Cyclone QFP and FineLine BGA Package Sizes**

Dimension	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0.5	0.5	0.5	1.0	1.0	1.0
Area (mm <sup>2</sup> )	256	484	1,024	289	361	441
Length × width (mm × mm)	16×16	22×22	34.6×34.6	17×17	19×19	21×21

## Document Revision History

Table 1–4 shows the revision history for this document.

**Table 1–4. Document Revision History**

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.5	Minor textual and style changes.	—
January 2007 v1.4	Added document revision history.	—
August 2005 v1.3	Minor updates.	—
October 2003 v1.2	Added 64-bit PCI support information.	—
September 2003 v1.1	<ul style="list-style-type: none"> <li>Updated LVDS data rates to 640 Mbps from 311 Mbps.</li> <li>Updated RSDS feature information.</li> </ul>	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

## LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within a LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows a LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. [“MultiTrack Interconnect” on page 2–12](#) for more information on LUT chain and register chain connections.

## addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either  $A + B$  or  $A - B$ . The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

## LE Operating Modes

The Cyclone LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous

### *Dynamic Arithmetic Mode*

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in [Figure 2-7](#), the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

$$\text{data1} + \text{data2} + \text{carry-in0}$$

or

$$\text{data1} + \text{data2} + \text{carry-in1}$$

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

## Embedded Memory

The Cyclone embedded memory consists of columns of M4K memory blocks. EP1C3 and EP1C6 devices have one column of M4K blocks, while EP1C12 and EP1C20 devices have two columns (refer to [Table 1–1 on page 1–1](#) for total RAM bits per density). Each M4K block can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. The M4K blocks support the following features:

- 4,608 RAM bits
- 250 MHz performance
- True dual-port memory
- Simple dual-port memory
- Single-port memory
- Byte enable
- Parity bits
- Shift register
- FIFO buffer
- ROM
- Mixed clock mode

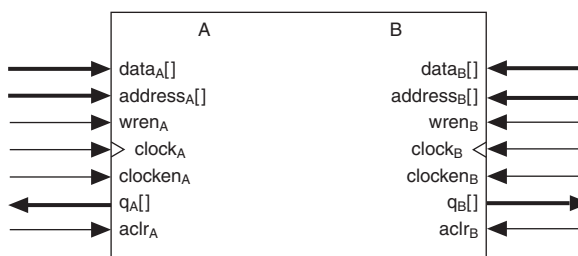


Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

### Memory Modes

The M4K memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. [Figure 2–12](#) shows true dual-port memory.

**Figure 2–12. True Dual-Port Memory Configuration**



## Byte Enables

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. [Table 2-5](#) summarizes the byte selection.

<b>Table 2-5. Byte Enable for M4K Blocks</b> <i>Notes (1), (2)</i>		
<b>byteena[3..0]</b>	<b>datain ×18</b>	<b>datain ×36</b>
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	—	[26..18]
[3] = 1	—	[35..27]

**Notes to [Table 2-5](#):**

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

## Control Signals and M4K Interface

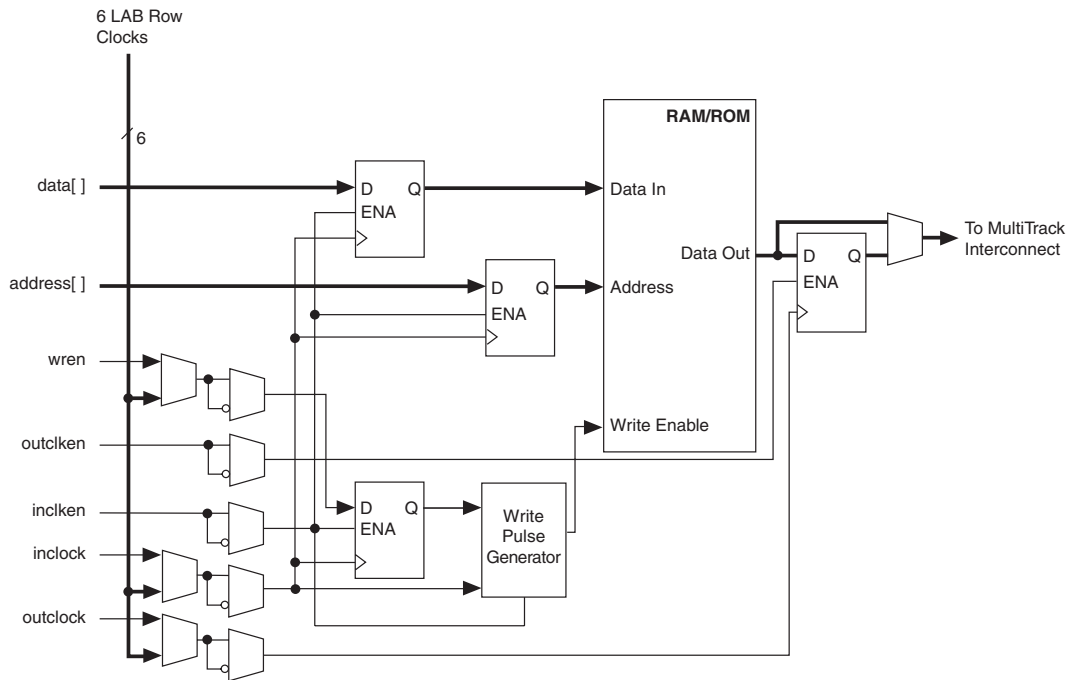
The M4K blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K block registers (*renwe*, *address*, *byte enable*, *datain*, and output registers). Only the output register can be bypassed. The six *labclk* signals or local interconnects can drive the control signals for the A and B ports of the M4K block. LEs can also control the *clock\_a*, *clock\_b*, *renwe\_a*, *renwe\_b*, *clr\_a*, *clr\_b*, *clocken\_a*, and *clocken\_b* signals, as shown in [Figure 2-15](#).

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through 10 direct link interconnects each. [Figure 2-16](#) shows the M4K block to logic array interface.

## Single-Port Mode

The M4K memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See [Figure 2–21](#). A single M4K memory block can support up to two single-port mode RAM blocks if each RAM block is less than or equal to 2K bits in size.

**Figure 2–21. Single-Port Mode** *Note (1)*



**Note to Figure 2–21:**

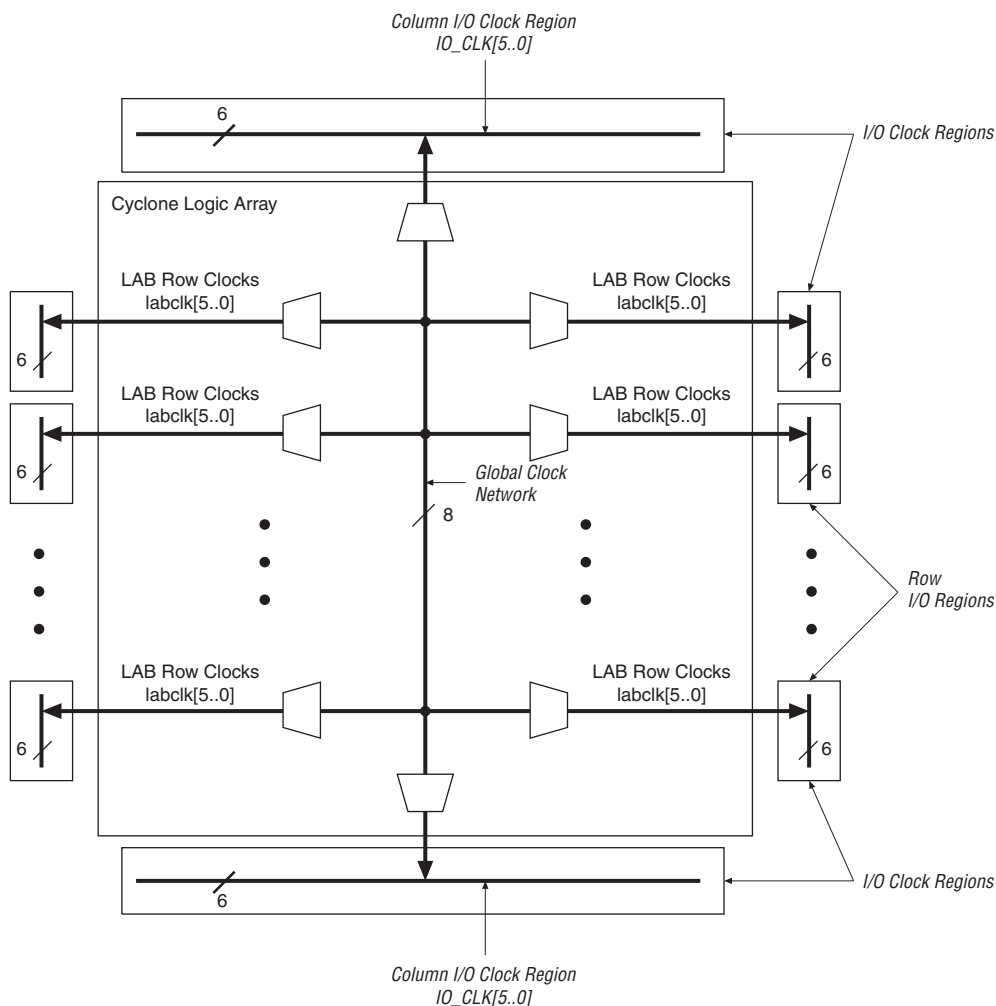
- (1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

## Global Clock Network and Phase-Locked Loops

Cyclone devices provide a global clock network and up to two PLLs for a complete clock management solution.

### Global Clock Network

There are four dedicated clock pins ( $CLK[3..0]$ , two pins on the left side and two pins on the right side) that drive the global clock network, as shown in [Figure 2–22](#). PLL outputs, logic array, and dual-purpose clock ( $DPCLK[7..0]$ ) pins can also drive the global clock network.

**Figure 2–24. I/O Clock Regions**

## PLLs

Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as outputs for differential I/O support. Cyclone devices contain two PLLs, except for the EP1C3 device, which contains one PLL.



**Table 2–7. Global Clock Network Sources (Part 2 of 2)**

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
Dual-Purpose Clock Pins	DPCLK0 (3)	—	—	—	✓	—	—	—	—
	DPCLK1 (3)	—	—	✓	—	—	—	—	—
	DPCLK2	✓	—	—	—	—	—	—	—
	DPCLK3	—	—	—	—	✓	—	—	—
	DPCLK4	—	—	—	—	—	—	✓	—
	DPCLK5 (3)	—	—	—	—	—	—	—	✓
	DPCLK6	—	—	—	—	—	✓	—	—
	DPCLK7	—	✓	—	—	—	—	—	—

**Notes to Table 2–7:**

- (1) EP1C3 devices only have one PLL (PLL 1).
- (2) EP1C3 devices in the 100-pin TQFP package do not have dedicated clock pins CLK1 and CLK3.
- (3) EP1C3 devices in the 100-pin TQFP package do not have the DPCLK0, DPCLK1, or DPCLK5 pins.

## Clock Multiplication and Division

Cyclone PLLs provide clock synthesis for PLL output ports using  $m/(n \times \text{post scale counter})$  scaling factors. The input clock is divided by a pre-scale divider,  $n$ , and is then multiplied by the  $m$  feedback factor. The control loop drives the VCO to match  $f_{IN} \times (m/n)$ . Each output port has a unique post-scale counter to divide down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least-common multiple in the VCO's range).

Each PLL has one pre-scale divider,  $n$ , that can range in value from 1 to 32. Each PLL also has one multiply divider,  $m$ , that can range in value from 2 to 32. Global clock outputs have two post scale G dividers for global clock outputs, and external clock outputs have an E divider for external clock output, both ranging from 1 to 32. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

## External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (CLK[3..0]) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See [Figure 2-25](#).

[Table 2-8](#) shows the I/O standards supported by PLL input and output pins.

<b>Table 2-8. PLL I/O Standards</b>		
<b>I/O Standard</b>	<b>CLK Input</b>	<b>EXTCLK Output</b>
3.3-V LVTTTL/LVCMOS	✓	✓
2.5-V LVTTTL/LVCMOS	✓	✓
1.8-V LVTTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

For more information on LVDS I/O support, refer to “[LVDS I/O Pins](#)” on [page 2-54](#).

## External Clock Outputs

Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these PLL\_OUT pins, the pins are available for use as general-purpose I/O pins. The PLL\_OUT pins support all I/O standards shown in [Table 2-8](#).

The external clock outputs do not have their own V<sub>CC</sub> and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

## Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

## Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

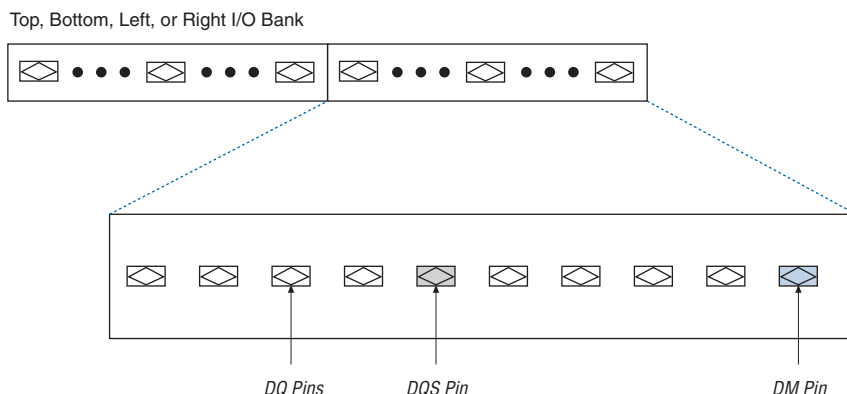


For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

output pins (`nSTATUS` and `CONF_DONE`) and all the JTAG pins in I/O bank 3 must operate at 2.5 V because the  $V_{CCIO}$  level of SSTL-2 is 2.5 V. I/O banks 1, 2, 3, and 4 support DQS signals with DQ bus modes of  $\times 8$ .

For  $\times 8$  mode, there are up to eight groups of programmable DQS and DQ pins, I/O banks 1, 2, 3, and 4 each have two groups in the 324-pin and 400-pin FineLine BGA packages. Each group consists of one DQS pin, a set of eight DQ pins, and one DM pin (see Figure 2–33). Each DQS pin drives the set of eight DQ pins within that group.

**Figure 2–33. Cyclone Device DQ and DQS Groups in  $\times 8$  Mode** *Note (1)*



**Note to Figure 2–33:**

- (1) Each DQ group consists of one DQS pin, eight DQ pins, and one DM pin.

Table 2–10 shows the number of DQ pin groups per device.

<b>Table 2–10. DQ Pin Groups (Part 1 of 2)</b>			
<b>Device</b>	<b>Package</b>	<b>Number of <math>\times 8</math> DQ Pin Groups</b>	<b>Total DQ Pin Count</b>
EP1C3	100-pin TQFP (1)	3	24
	144-pin TQFP	4	32
EP1C4	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

<b>Table 2–10. DQ Pin Groups (Part 2 of 2)</b>			
<b>Device</b>	<b>Package</b>	<b>Number of × 8 DQ Pin Groups</b>	<b>Total DQ Pin Count</b>
EP1C6	144-pin TQFP	4	32
	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
EP1C12	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
	324-pin FineLine BGA	8	64
EP1C20	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

**Note to Table 2–10:**

- (1) EP1C3 devices in the 100-pin TQFP package do not have any DQ pin groups in I/O bank 1.

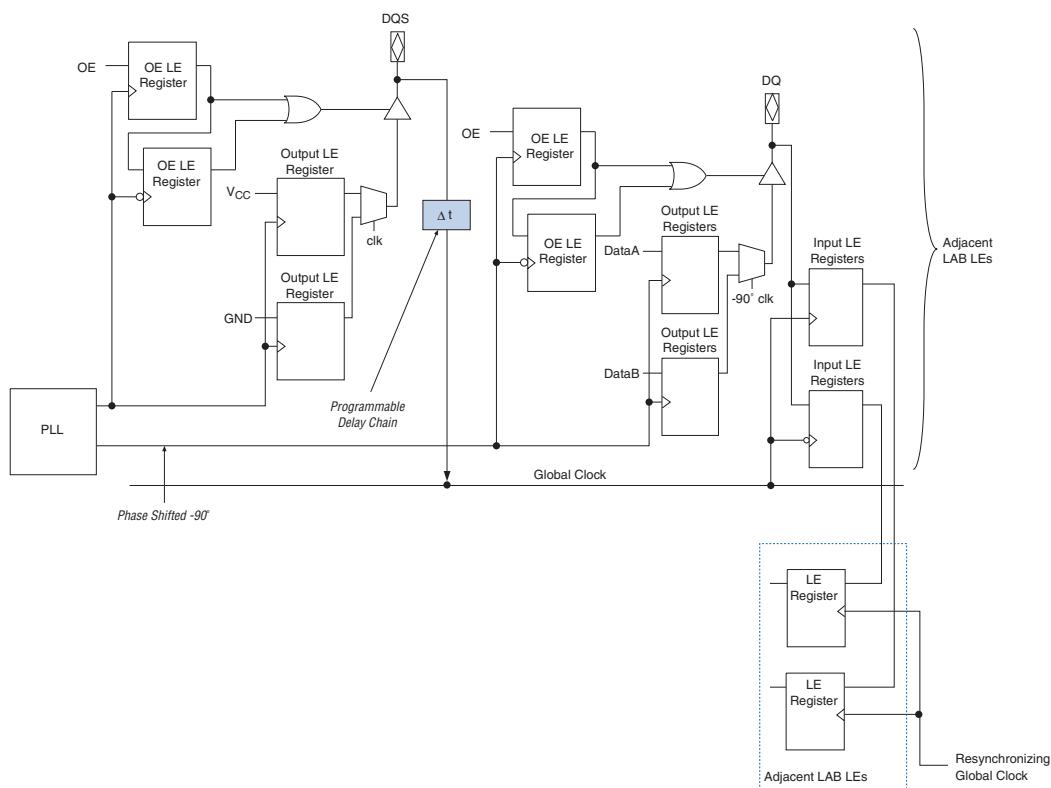
A programmable delay chain on each DQS pin allows for either a 90° phase shift (for DDR SDRAM), or a 72° phase shift (for FCRAM) which automatically center-aligns input DQS synchronization signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal clocks DQ signals on internal LE registers.

These DQS delay elements combine with the PLL's clocking and phase shift ability to provide a complete hardware solution for interfacing to high-speed memory.

The clock phase shift allows the PLL to clock the DQ output enable and output paths. The designer should use the following guidelines to meet 133 MHz performance for DDR SDRAM and FCRAM interfaces:

- The DQS signal must be in the middle of the DQ group it clocks
- Resynchronize the incoming data to the logic array clock using successive LE registers or FIFO buffers
- LE registers must be placed in the LAB adjacent to the DQ I/O pin column it is fed by

Figure 2–34 illustrates DDR SDRAM and FCRAM interfacing from the I/O through the dedicated circuitry to the logic array.

**Figure 2–34. DDR SDRAM and FCRAM Interfacing**

## Programmable Drive Strength

The output buffer for each Cyclone device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTTL and LVCMOS standards have several levels of drive strength that the designer can control. SSTL-3 class I and II, and SSTL-2 class I and II support a minimum setting, the lowest drive strength that guarantees the  $I_{OH}/I_{OL}$

Each I/O bank can support multiple standards with the same  $V_{CCIO}$  for input and output pins. For example, when  $V_{CCIO}$  is 3.3-V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

## LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100- $\Omega$  termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

<b>Table 2–13. Cyclone Device LVDS Channels</b>		
<b>Device</b>	<b>Pin Count</b>	<b>Number of LVDS Channels</b>
EP1C3	100	(1)
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

**Note to Table 2–13:**

- (1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

## MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and four sets for I/O output drivers ( $V_{CCIO}$ ).

**Table 3–1. Cyclone JTAG Instructions (Part 2 of 2)**

JTAG Instruction	Instruction Code	Description
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP (1)	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring a Cyclone device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction will hold nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured.
SignalTap II instructions	—	Monitors internal device operation with the SignalTap II embedded logic analyzer.

**Note to Table 3–1:**

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

In the Quartus II software, there is an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. Choose Assignments > Device > Device and Pin Options > General. Turn on **Auto Usercode**.





Cyclone devices must be within the first 8 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone devices are in the 9th or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.



For more information on JTAG, refer to the following documents:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

## SignalTap II Embedded Logic Analyzer

Cyclone devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. A designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

## Configuration

The logic, circuitry, and interconnects in the Cyclone architecture are configured with CMOS SRAM elements. Altera FPGAs are reconfigurable and every device is tested with a high coverage production test program so the designer does not have to perform fault testing and can instead focus on simulation and design verification.

Cyclone devices are configured at system power-up with data stored in an Altera configuration device or provided by a system controller. The Cyclone device's optimized interface allows the device to act as controller in an active serial configuration scheme with the new low-cost serial configuration device. Cyclone devices can be configured in under 120 ms using serial data at 20 MHz. The serial configuration device can be programmed via the ByteBlaster II download cable, the Altera Programming Unit (APU), or third-party programmers.

In addition to the new low-cost serial configuration device, Altera offers in-system programmability (ISP)-capable configuration devices that can configure Cyclone devices via a serial data stream. The interface also enables microprocessors to treat Cyclone devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy. After a Cyclone device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

**Table 4–8. 1.5-V I/O Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	1.4	1.6	V
$V_{IH}$	High-level input voltage	—	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$ (12)	V
$V_{IL}$	Low-level input voltage	—	–0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -2 \text{ mA}$ (11)	$0.75 \times V_{CCIO}$	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2 \text{ mA}$ (11)	—	$0.25 \times V_{CCIO}$	V

**Table 4–9. 2.5-V LVDS I/O Specifications** Note (13)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	2.375	2.5	2.625	V
$V_{OD}$	Differential output voltage	$R_L = 100 \, \Omega$	250	—	550	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low	$R_L = 100 \, \Omega$	—	—	50	mV
$V_{OS}$	Output offset voltage	$R_L = 100 \, \Omega$	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between high and low	$R_L = 100 \, \Omega$	—	—	50	mV
$V_{TH}$	Differential input threshold	$V_{CM} = 1.2 \text{ V}$	–100	—	100	mV
$V_{IN}$	Receiver input voltage range	—	0.0	—	2.4	V
$R_L$	Receiver differential input resistor	—	90	100	110	$\Omega$

**Table 4–10. 3.3-V PCI Specifications (Part 1 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	3.0	3.3	3.6	V
$V_{IH}$	High-level input voltage	—	$0.5 \times V_{CCIO}$	—	$V_{CCIO} + 0.5$	V
$V_{IL}$	Low-level input voltage	—	–0.5	—	$0.3 \times V_{CCIO}$	V

**Table 4–16. Cyclone Device Capacitance** *Note (14)*

Symbol	Parameter	Typical	Unit
$C_{IO}$	Input capacitance for user I/O pin	4.0	pF
$C_{LVDS}$	Input capacitance for dual-purpose LVDS/user I/O pin	4.7	pF
$C_{VREF}$	Input capacitance for dual-purpose $V_{REF}$ /user I/O pin.	12.0	pF
$C_{DPCLK}$	Input capacitance for dual-purpose $DPCLK$ /user I/O pin.	4.4	pF
$C_{CLK}$	Input capacitance for CLK pin.	4.7	pF

**Notes to Tables 4–1 through 4–16:**

- (1) Refer to the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
- (3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
- (4) Maximum  $V_{CC}$  rise time is 100 ms, and  $V_{CC}$  must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (6) Typical values are for  $T_A = 25^\circ\text{C}$ ,  $V_{CCINT} = 1.5\text{ V}$ , and  $V_{CCIO} = 1.5\text{ V}$ , 1.8 V, 2.5 V, and 3.3 V.
- (7)  $V_I = \text{ground}$ , no load, no toggling inputs.
- (8) This value is specified for normal device operation. The value may vary during power-up. This applies for all  $V_{CCIO}$  settings (3.3, 2.5, 1.8, and 1.5 V).
- (9)  $R_{CONF}$  is the measured value of internal pull-up resistance when the I/O pin is tied directly to GND.  $R_{CONF}$  value will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (10) Pin pull-up resistance values will lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (11) Drive strength is programmable according to values in *Cyclone Architecture* chapter in the *Cyclone Device Handbook*.
- (12) Overdrive is possible when a 1.5 V or 1.8 V and a 2.5 V or 3.3 V input signal feeds an input pin. Turn on “Allow voltage overdrive” for LVTTTL/LVCMOS input pins in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combination. However, higher leakage current is expected.
- (13) The Cyclone LVDS interface requires a resistor network outside of the transmitter channels.
- (14) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within  $\pm 0.5\text{ pF}$ .

**Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.8-V LVTTTL	2 mA	—	1,290	—	1,483	—	1,677	ps
	8 mA	—	4	—	4	—	5	ps
	12 mA	—	–208	—	–240	—	–271	ps
1.5-V LVTTTL	2 mA	—	2,288	—	2,631	—	2,974	ps
	4 mA	—	608	—	699	—	790	ps
	8 mA	—	292	—	335	—	379	ps
3.3-V PCI (†)		—	–877	—	–1,009	—	–1,141	ps
SSTL-3 class I		—	–410	—	–472	—	–533	ps
SSTL-3 class II		—	–811	—	–933	—	–1,055	ps
SSTL-2 class I		—	–485	—	–558	—	–631	ps
SSTL-2 class II		—	–758	—	–872	—	–986	ps
LVDS		—	–998	—	–1,148	—	–1,298	ps

**Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)**

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	1,800	—	2,070	—	2,340	ps
	4 mA	—	1,311	—	1,507	—	1,704	ps
	8 mA	—	945	—	1,086	—	1,228	ps
	12 mA	—	807	—	928	—	1,049	ps
3.3-V LVTTTL	4 mA	—	1,831	—	2,105	—	2,380	ps
	8 mA	—	1,484	—	1,705	—	1,928	ps
	12 mA	—	973	—	1,118	—	1,264	ps
	16 mA	—	1,012	—	1,163	—	1,315	ps
	24 mA	—	838	—	963	—	1,089	ps
2.5-V LVTTTL	2 mA	—	2,747	—	3,158	—	3,570	ps
	8 mA	—	1,757	—	2,019	—	2,283	ps
	12 mA	—	1,763	—	2,026	—	2,291	ps
	16 mA	—	1,623	—	1,865	—	2,109	ps
1.8-V LVTTTL	2 mA	—	5,506	—	6,331	—	7,157	ps
	8 mA	—	4,220	—	4,852	—	5,485	ps
	12 mA	—	4,008	—	4,608	—	5,209	ps

### Software

Cyclone® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analysis, and device configuration.



For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

### Device Pin-Outs

Device pin-outs for Cyclone devices are available on the Altera website ([www.altera.com](http://www.altera.com)) and in the *Cyclone Device Handbook*.

### Ordering Information

Figure 5–1 describes the ordering codes for Cyclone devices. For more information about a specific package, refer to the *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*.