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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

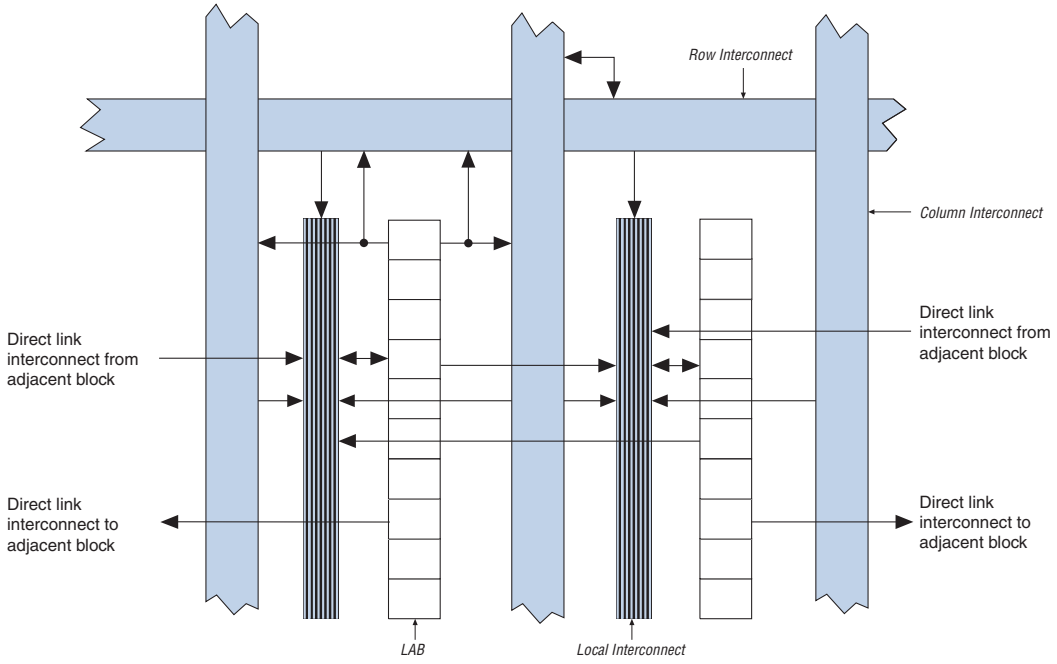
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	291
Number of Logic Elements/Cells	2910
Total RAM Bits	59904
Number of I/O	104
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c3t144c6n

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, look-up table (LUT) chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within a LAB. The Quartus® II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 details the Cyclone LAB.

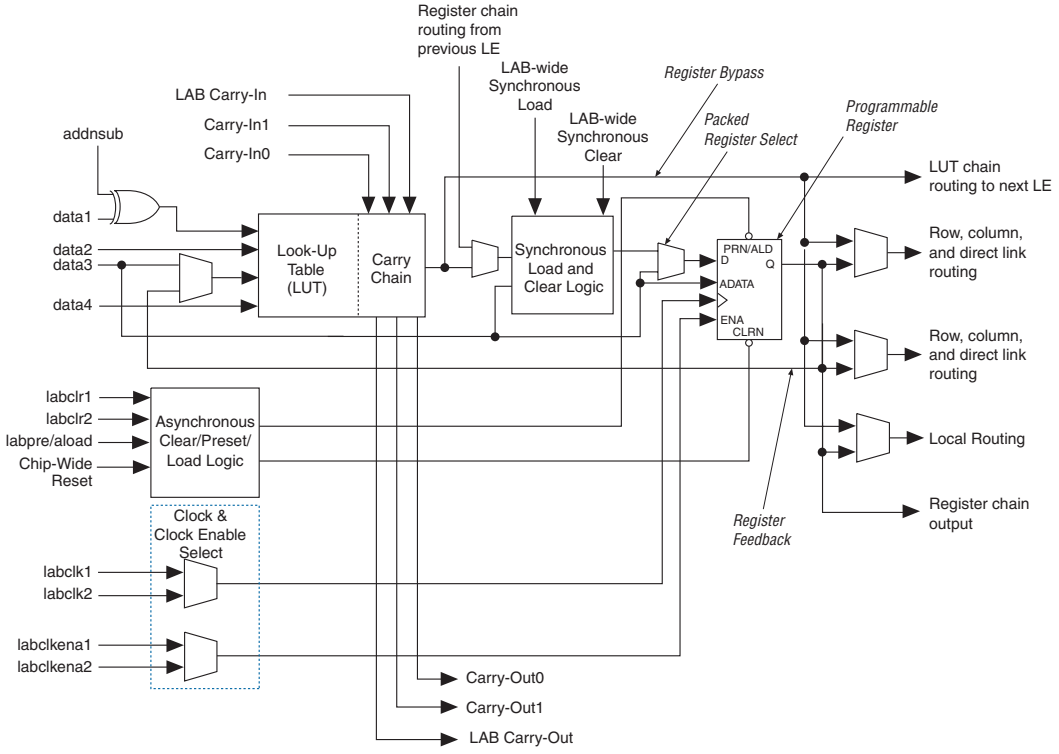
Figure 2–2. Cyclone LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, and M4K RAM blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher

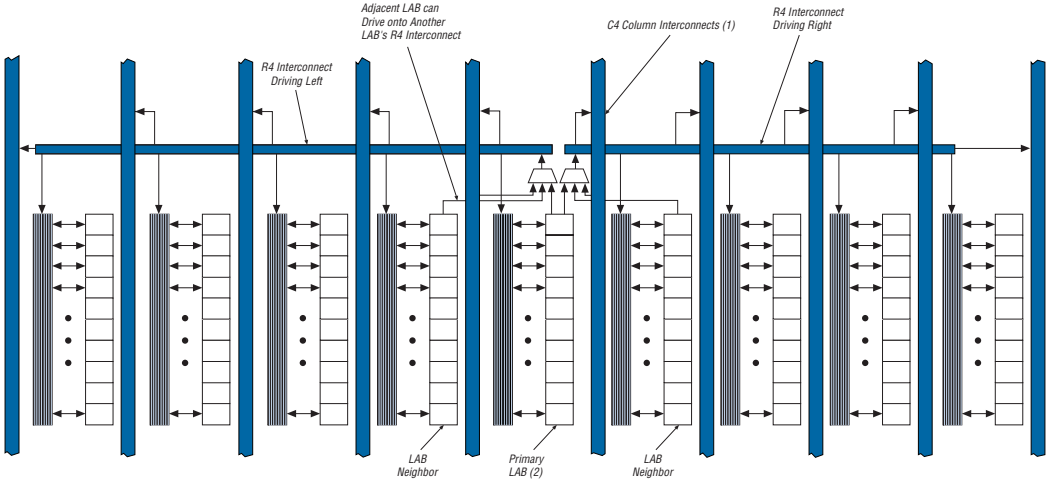
Figure 2–5. Cyclone LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated

Figure 2–9. R4 Interconnect Connections



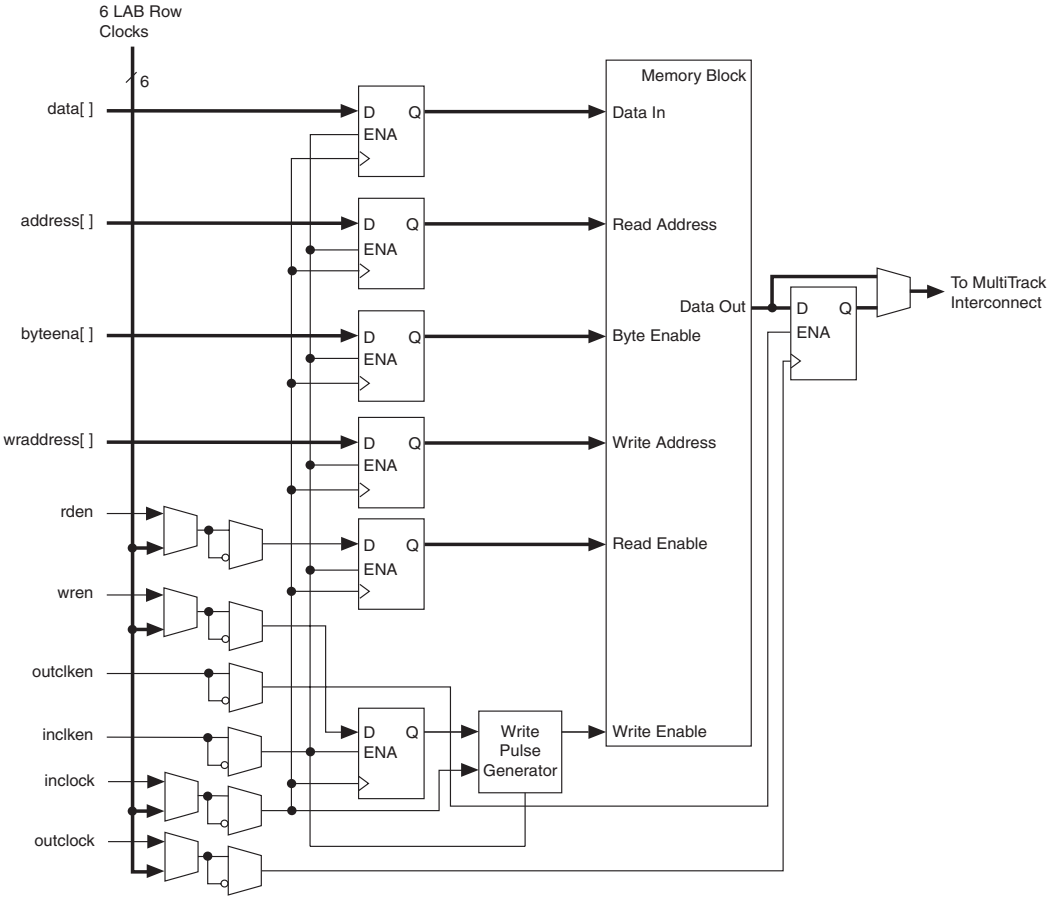
Notes to Figure 2–9:
(1) C4 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, M4K memory blocks, and row and column IOEs. These column resources include:

- LUT chain interconnects within a LAB
- Register chain interconnects within a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction

Cyclone devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

Figure 2–19. Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*



Notes to Figure 2–19:

(1) All registers shown except the rden register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Table 2–6 shows the PLL features in Cyclone devices. Figure 2–25 shows a Cyclone PLL.

Table 2–6. Cyclone PLL Features

Feature	PLL Support
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*
Phase shift	Down to 125-ps increments *(2)*, *(3)*
Programmable duty cycle	Yes
Number of internal clock outputs	2
Number of external clock outputs	One differential or one single-ended *(4)*

Notes to Table 2–6:

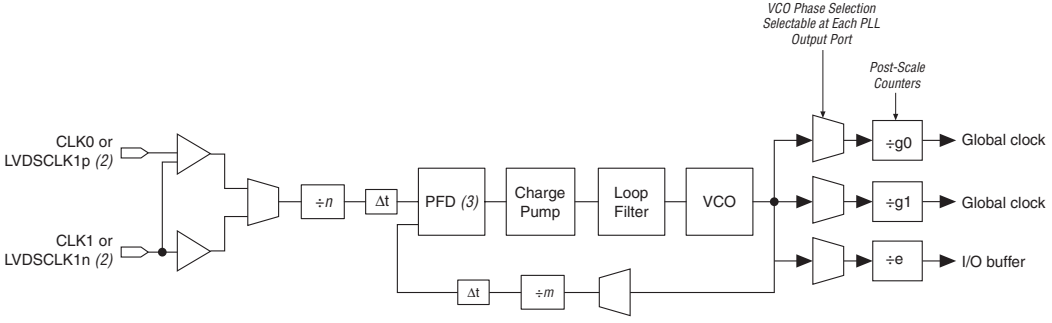
(1) The *m* counter ranges from 2 to 32. The *n* counter and the post-scale counters range from 1 to 32.

(2) The smallest phase shift is determined by the voltage-controlled oscillator (VCO) period divided by 8.

(3) For degree increments, Cyclone devices can shift all output frequencies in increments of 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

(4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Figure 2–25. Cyclone PLL *Note (1)*



Notes to Figure 2–25:

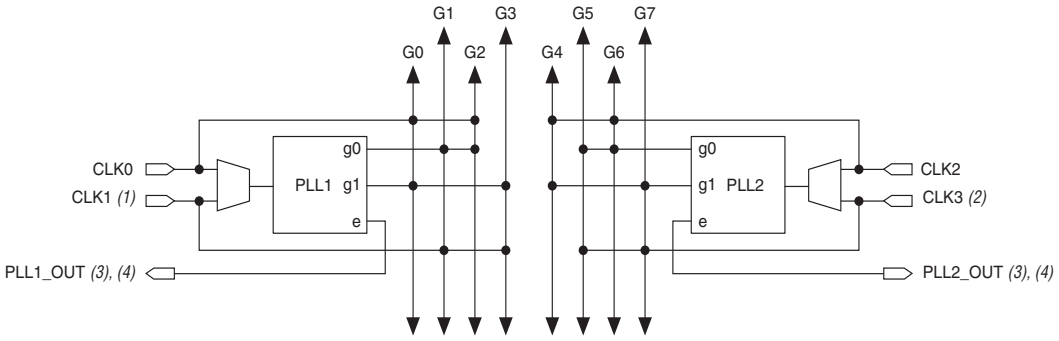
(1) The EP1C3 device in the 100-pin TQFP package does not support external outputs or LVDS inputs. The EP1C6 device in the 144-pin TQFP package does not support external output from PLL2.

(2) LVDS input is supported via the secondary function of the dedicated clock pins. For PLL 1, the `CLK0` pin's secondary function is `LVDSCLK1p` and the `CLK1` pin's secondary function is `LVDSCLK1n`. For PLL 2, the `CLK2` pin's secondary function is `LVDSCLK2p` and the `CLK3` pin's secondary function is `LVDSCLK2n`.

(3) PFD: phase frequency detector.

Figure 2–26 shows the PLL global clock connections.

Figure 2–26. Cyclone PLL Global Clock Connections



Notes to Figure 2–26:

(1) PLL 1 supports one single-ended or LVDS input via pins CLK0 and CLK1.

(2) PLL2 supports one single-ended or LVDS input via pins CLK2 and CLK3.

(3) PLL1_OUT and PLL2_OUT support single-ended or LVDS output. If external output is not required, these pins are available as regular user I/O pins.

(4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Table 2–7 shows the global clock network sources available in Cyclone devices.

Table 2–7. Global Clock Network Sources (Part 1 of 2)

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
PLL Counter Output	PLL1 G0	—	✓	✓	—	—	—	—	—
	PLL1 G1	✓	—	—	✓	—	—	—	—
	PLL2 G0 *(1)*	—	—	—	—	—	✓	✓	—
	PLL2 G1 *(1)*	—	—	—	—	✓	—	—	✓
Dedicated Clock Input Pins	CLK0	✓	—	✓	—	—	—	—	—
	CLK1 *(2)*	—	✓	—	✓	—	—	—	—
	CLK2	—	—	—	—	✓	—	✓	—
	CLK3 *(2)*	—	—	—	—	—	✓	—	✓

External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (CLK[3..0]) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See Figure 2–25.

Table 2–8 shows the I/O standards supported by PLL input and output pins.

Table 2–8. PLL I/O Standards

I/O Standard	CLK Input	EXTCLK Output
3.3-V LVTTL/LVCMOS	✓	✓
2.5-V LVTTL/LVCMOS	✓	✓
1.8-V LVTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

For more information on LVDS I/O support, refer to "LVDS I/O Pins" on page 2–54.

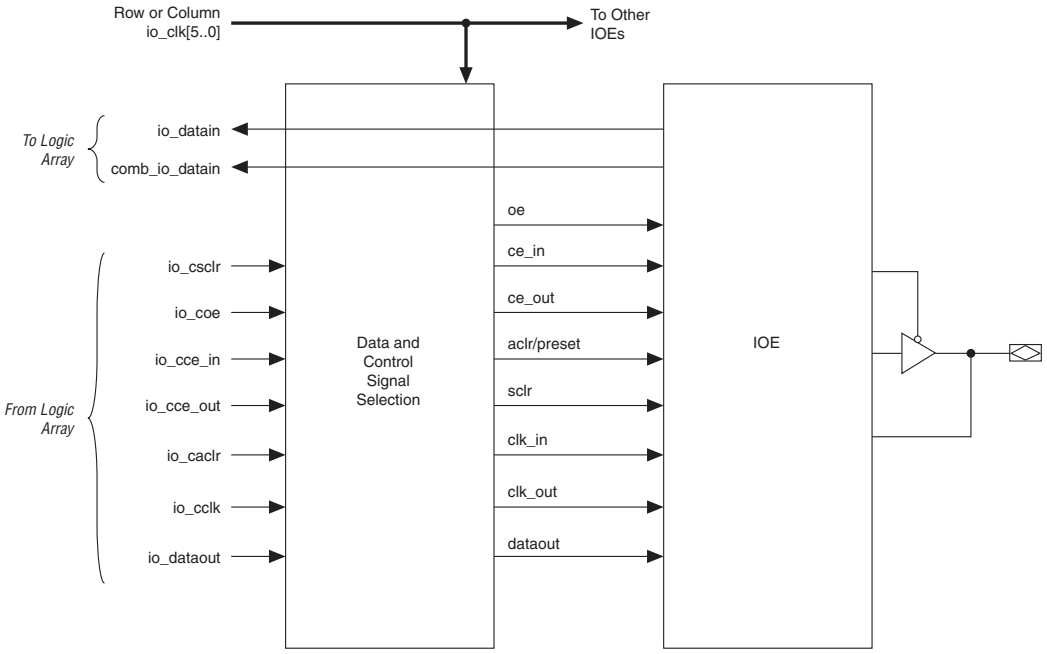
External Clock Outputs

Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these PLL_OUT pins, the pins are available for use as general-purpose I/O pins. The PLL_OUT pins support all I/O standards shown in Table 2–8.

The external clock outputs do not have their own V_{CC} and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, `io_clk[5..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see "Global Clock Network and Phase-Locked Loops" on page 2–29). Figure 2–30 illustrates the signal paths through the I/O block.

Figure 2–30. Signal Path through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 2–31 illustrates the control signal selection.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

Table 2–13. Cyclone Device LVDS Channels

Device	Pin Count	Number of LVDS Channels
EP1C3	100	*(1)*
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

Note to Table 2–13:

(1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and four sets for I/O output drivers (V_{CCIO}).

Operating Modes

The Cyclone architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Cyclone devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the V_{CCIO} of the bank where the pins reside. The bank V_{CCIO} selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Configuration Schemes

Designers can load the configuration data for a Cyclone device with one of three configuration schemes (see Table 3–5), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone device. A low-cost configuration device can automatically configure a Cyclone device at system power-up.

4. DC and Switching Characteristics

C51004-1.7

Operating Conditions

Cyclone® devices are offered in both commercial, industrial, and extended temperature grades. However, industrial-grade and extended-temperature-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Cyclone devices.

Table 4–1. Cyclone Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_{CCA}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	BGA packages under bias	—	135	°C

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(5)*	–0.5	4.1	V

Typically, the user-mode current during device operation is lower than the power-up current in Table 4–17. Altera recommends using the Cyclone Power Calculator, available on the Altera web site, to estimate the user-mode I_{CCINT} consumption and then select power supplies or regulators based on the higher value.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–18 shows the status of the Cyclone device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–18. Cyclone Device Timing Model Status

Device	Preliminary	Final
EP1C3	—	✓
EP1C4	—	✓
EP1C6	—	✓
EP1C12	—	✓
EP1C20	—	✓

Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in Table 4–19.

Table 4–19. Clock Tree Maximum Performance Specification

Parameter	Definition	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock tree f_{MAX}	Maximum frequency that the clock tree can support for clocking registered logic	—	—	405	—	—	320	—	—	275	MHz

Table 4–20 shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
LE	16-to-1 multiplexer	—	21	—	—	405.00	320.00	275.00
	32-to-1 multiplexer	—	44	—	—	317.36	284.98	260.15
	16-bit counter	—	16	—	—	405.00	320.00	275.00
	64-bit counter *(1)*	—	66	—	—	208.99	181.98	160.75

Table 4–24. Routing Delay Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{R4}	Delay for an R4 line with average loading; covers a distance of four LAB columns
t_{C4}	Delay for an C4 line with average loading; covers a distance of four LAB rows
t_{LOCAL}	Local interconnect delay

Figure 4–1 shows the memory waveforms for the M4K timing parameters shown in Table 4–23.

Figure 4–1. Dual-Port RAM Timing Microparameter Waveform

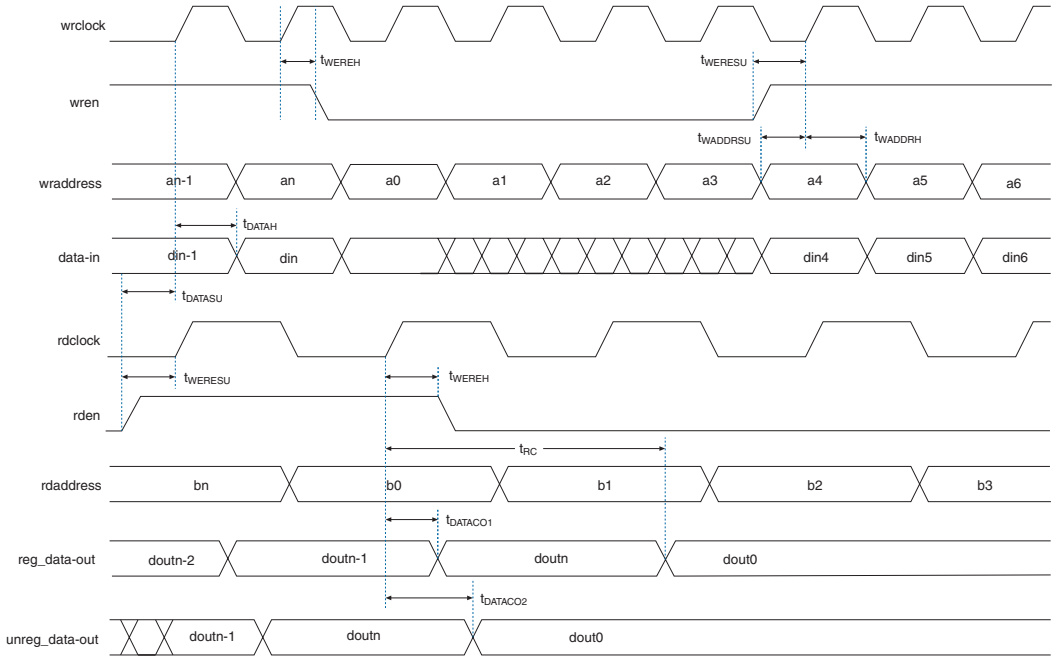


Table 4–39. EP1C20 Row Pin Global Clock External I/O Timing Parameters							
Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.417	—	2.779	—	3.140	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.724	2.000	4.282	2.000	4.843	ns
t_{XZ}	—	3.645	—	4.191	—	4.740	ns
t_{ZX}	—	3.645	—	4.191	—	4.740	ns
$t_{INSUPLL}$	1.417	—	1.629	—	1.840	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	1.667	0.500	1.917	0.500	2.169	ns
t_{XZPLL}	—	1.588	—	1.826	—	2.066	ns
t_{ZXPLL}	—	1.588	—	1.826	—	2.066	ns

External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–40 through 4–45 show the adder delays associated with column and row I/O pins for all packages. If an I/O standard is selected other than LVTTL 4 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters shown in Tables 4–25 through 4–28.

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 1 of 2)							
I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS	—	0	—	0	—	0	ps
3.3-V LVTTL	—	0	—	0	—	0	ps
2.5-V LVTTL	—	27	—	31	—	35	ps
1.8-V LVTTL	—	182	—	209	—	236	ps
1.5-V LVTTL	—	278	—	319	—	361	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class II		–278	—	–320	—	–362	ps
LVDS		–261	—	–301	—	–340	ps

Table 4–41. Cyclone I/O Standard Row Pin Input Delay Adders

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS	—	0	—	0	—	0	ps
3.3-V LVTTL	—	0	—	0	—	0	ps
2.5-V LVTTL	—	27	—	31	—	35	ps
1.8-V LVTTL	—	182	—	209	—	236	ps
1.5-V LVTTL	—	278	—	319	—	361	ps
3.3-V PCI *(1)*	—	0	—	0	—	0	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps
SSTL-2 class II	—	–278	—	–320	—	–362	ps
LVDS	—	–261	—	–301	—	–340	ps

Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps

Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTL	2 mA	—	329	—	378	—	427	ps
	8 mA	—	–661	—	–761	—	–860	ps
	12 mA	—	–655	—	–754	—	–852	ps
	16 mA	—	–795	—	–915	—	–1034	ps
1.8-V LVTTL	2 mA	—	4	—	4	—	5	ps
	8 mA	—	–208	—	–240	—	–271	ps
	12 mA	—	–208	—	–240	—	–271	ps
1.5-V LVTTL	2 mA	—	2,288	—	2,631	—	2,974	ps
	4 mA	—	608	—	699	—	790	ps
	8 mA	—	292	—	335	—	379	ps
SSTL-3 class I		—	–410	—	–472	—	–533	ps
SSTL-3 class II		—	–811	—	–933	—	–1,055	ps
SSTL-2 class I		—	–485	—	–558	—	–631	ps
SSTL-2 class II		—	–758	—	–872	—	–986	ps
LVDS		—	–998	—	–1,148	—	–1,298	ps

Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps
2.5-V LVTTL	2 mA	—	329	—	378	—	427	ps
	8 mA	—	–661	—	–761	—	–860	ps
	12 mA	—	–655	—	–754	—	–852	ps
	16 mA	—	–795	—	–915	—	–1,034	ps

Table 4–47. Cyclone IOE Programmable Delays on Row Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	154	—	177	—	200	ps
	Small	—	2,212	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	154	—	177	—	200	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	556	—	639	—	722	ps

Note to Table 4–47:
(1) EPC1C3 devices do not support the PCI I/O standard.

Maximum Input and Output Clock Rates

Tables 4–48 and 4–49 show the maximum input clock rate for column and row pins in Cyclone devices.

Table 4–48. Cyclone Maximum Input Clock Rate for Column Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVCMOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
LVDS	567	549	531	MHz

5. Reference and Ordering Information

C51005-1.4

Software

Cyclone® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analysis, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

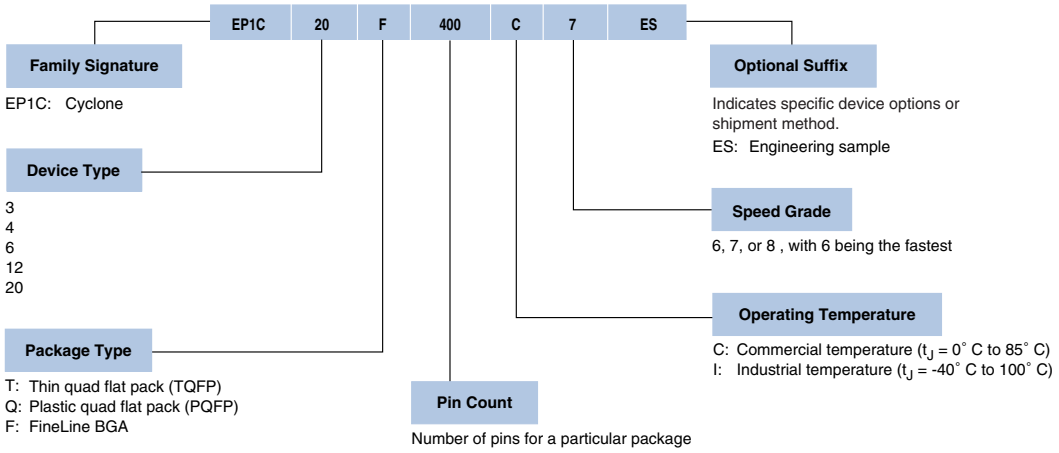
Device Pin-Outs

Device pin-outs for Cyclone devices are available on the Altera website (www.altera.com) and in the *Cyclone Device Handbook*.

Ordering Information

Figure 5–1 describes the ordering codes for Cyclone devices. For more information about a specific package, refer to the *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*.

Figure 5–1. Cyclone Device Packaging Ordering Information



Referenced Documents

This chapter references the following documents:

- *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*
- *Quartus II Handbook*

Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added "Referenced Documents" section.	—
January 2007 v1.3	Added document revision history.	—
August 2005 v1.2	Minor updates.	—