Intel - EP1C3T144C7 Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	291
Number of Logic Elements/Cells	2910
Total RAM Bits	59904
Number of I/O	104
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c3t144c7

1. Introduction

C51001-1.5

Introduction

The Cyclone® field programmable gate array family is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 Kbits of RAM. With features like phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements, Cyclone devices are a cost-effective solution for data-path applications. Cyclone devices support various I/O standards, including LVDS at data rates up to 640 megabits per second (Mbps), and 66- and 33-MHz, 64- and 32-bit peripheral component interconnect (PCI), for interfacing with and supporting ASSP and ASIC devices. Altera also offers new low-cost serial configuration devices to configure Cyclone devices.

Features

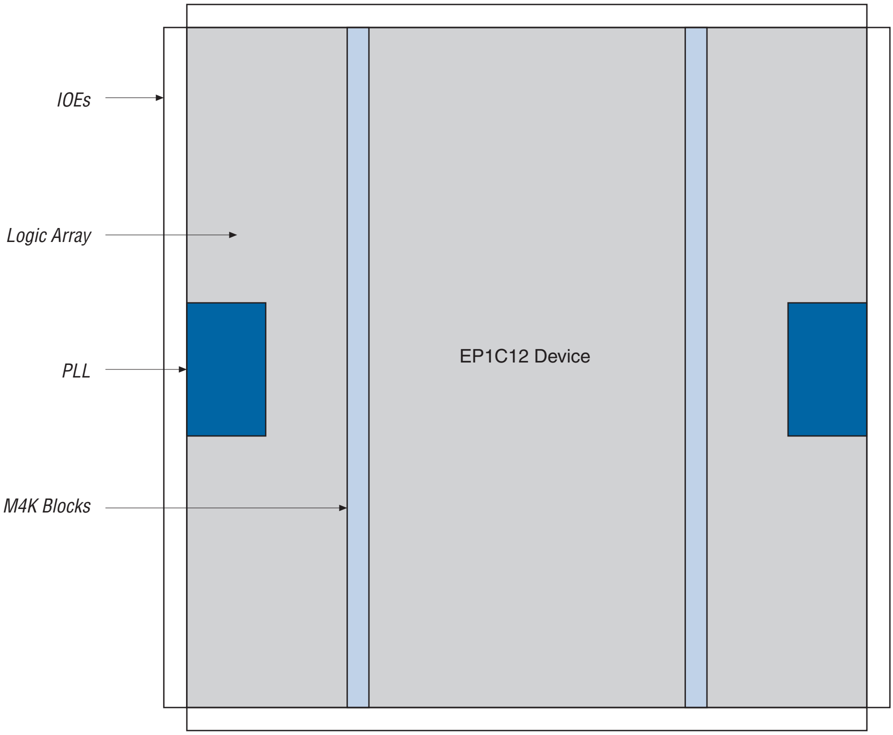
The Cyclone device family offers the following features:

- 2,910 to 20,060 LEs, see Table 1–1
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66- and 33-MHz, 64- and 32-bit PCI standard
- High-speed (640 Mbps) LVDS I/O support
- Low-speed (311 Mbps) LVDS I/O support
- 311-Mbps RSDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz), FCRAM, and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) cores, including Altera® MegaCore® functions and Altera Megafunctions Partners Program (AMPP℠) megafunctions.

Table 1–1. Cyclone Device Features (Part 1 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
LEs	2,910	4,000	5,980	12,060	20,060
M4K RAM blocks (128 × 36 bits)	13	17	20	52	64

Figure 2–1. Cyclone EP1C12 Device Block Diagram



The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

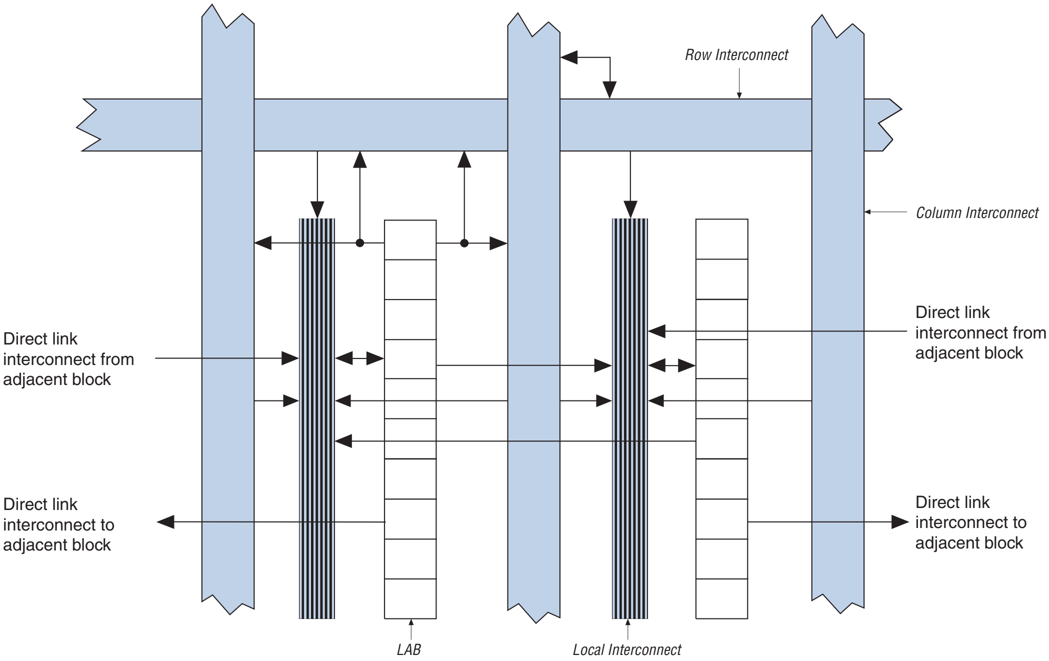
Table 2–1. Cyclone Device Resources

Device	M4K RAM		PLLs	LAB Columns	LAB Rows
	Columns	Blocks			
EP1C3	1	13	1	24	13
EP1C4	1	17	2	26	17
EP1C6	1	20	2	32	20
EP1C12	2	52	2	48	26
EP1C20	2	64	2	64	32

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, look-up table (LUT) chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within a LAB. The Quartus® II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 details the Cyclone LAB.

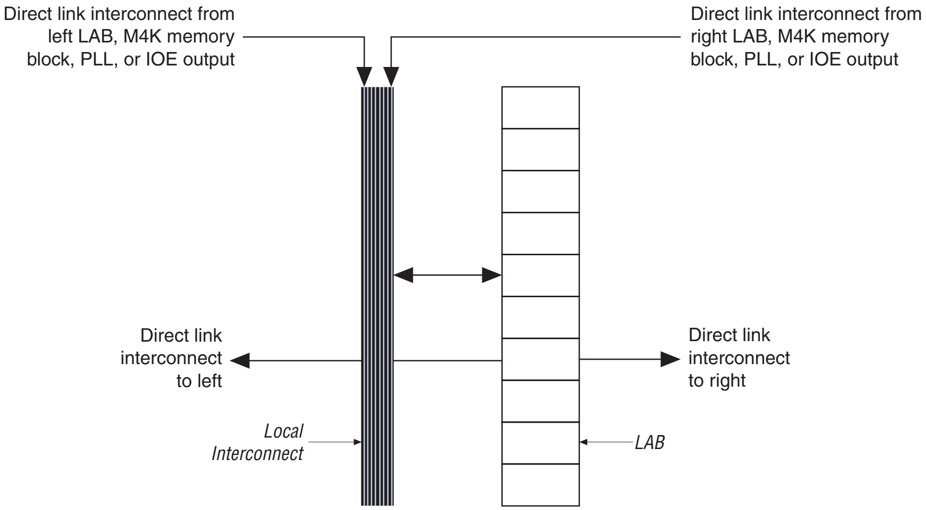
Figure 2–2. Cyclone LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, and M4K RAM blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

Figure 2–3. Direct Link Connection



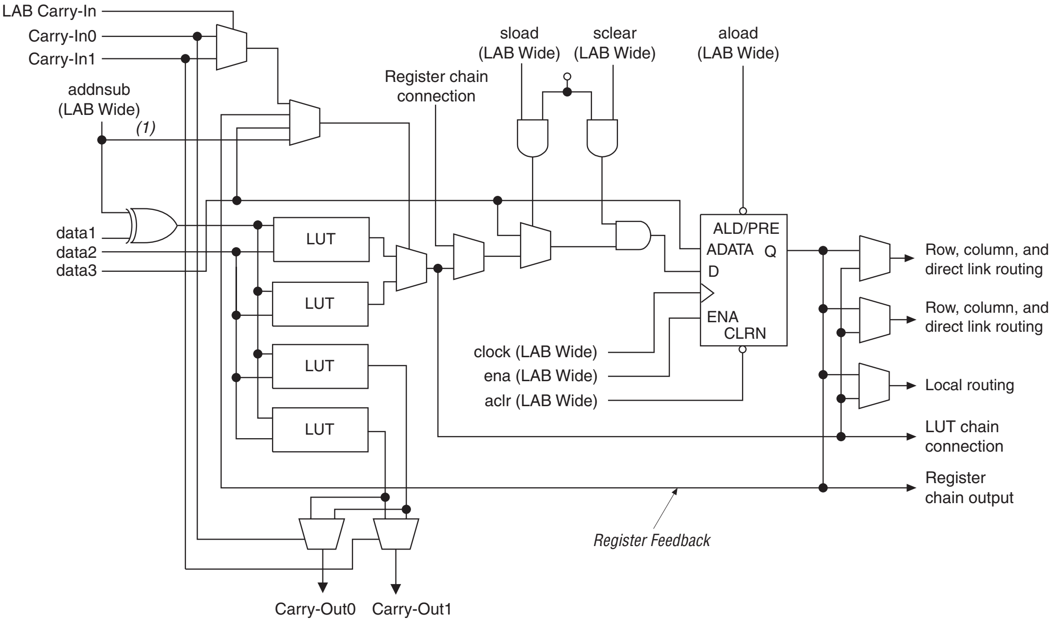
LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

Figure 2–7. LE in Dynamic Arithmetic Mode



Note to Figure 2–7:

(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within a LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Cyclone architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to M4K memory blocks. A carry chain can continue as far as a full column.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Cyclone devices support simultaneous preset/ asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Cyclone devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Cyclone architecture, connections between LEs, M4K memory blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

Table 2–4. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 2–15. M4K RAM Block Control Signals

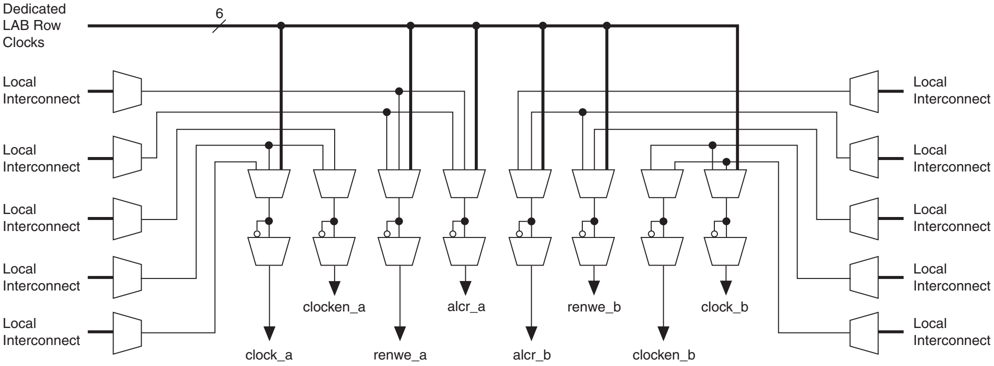


Figure 2–16. M4K RAM Block LAB Row Interface

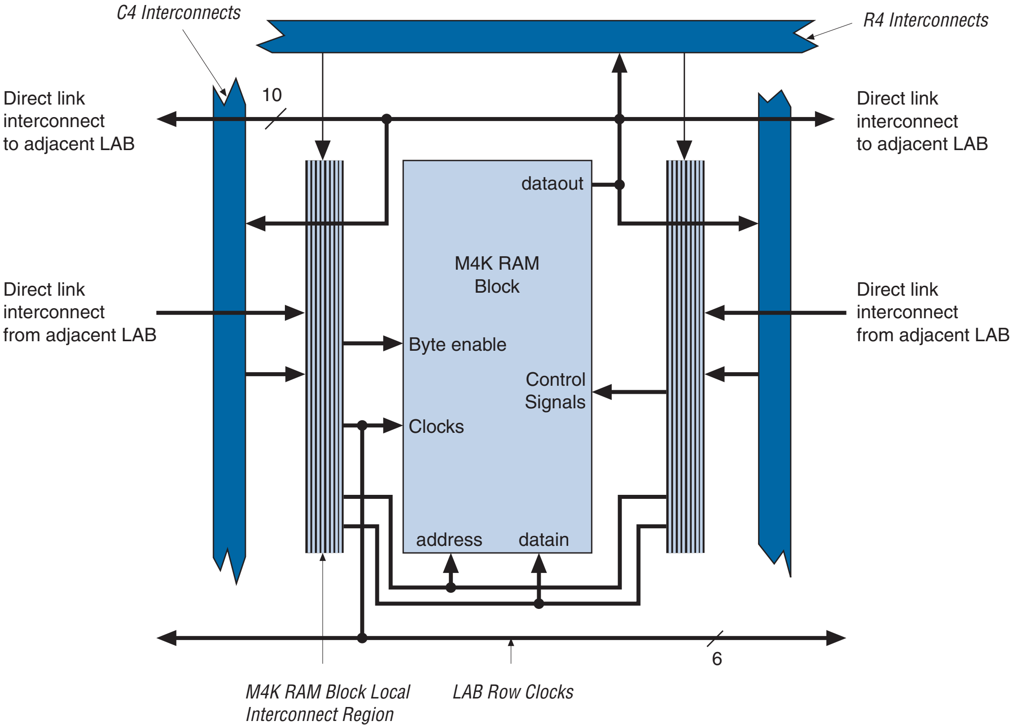
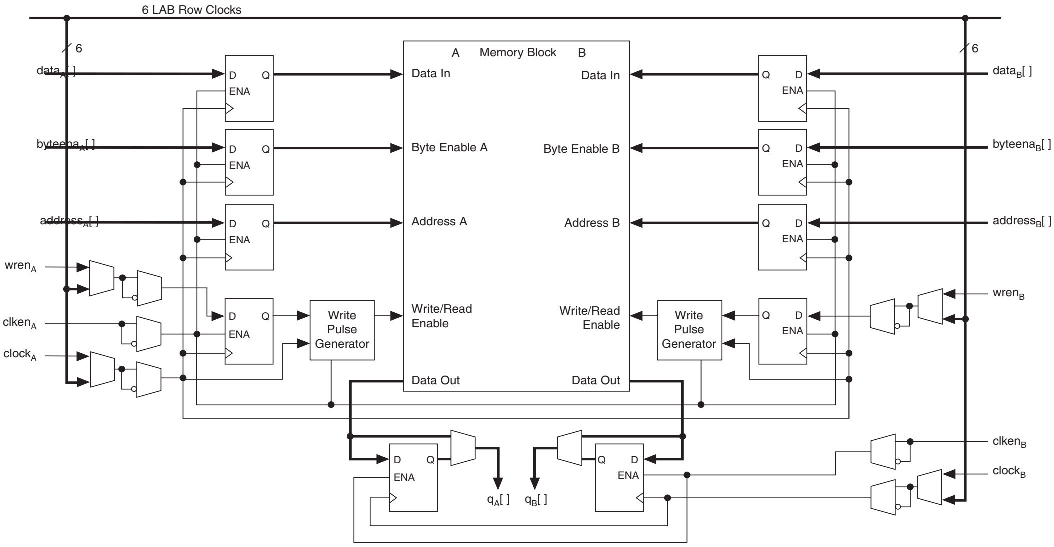


Figure 2–18. Input/Output Clock Mode in True Dual-Port Mode *Notes (1), (2)*



Notes to Figure 2–18:

(1) All registers shown have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

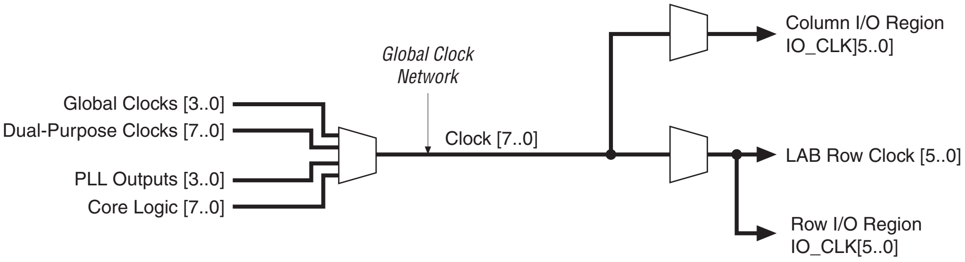
Dual-Purpose Clock Pins

Each Cyclone device except the EP1C3 device has eight dual-purpose clock pins, `DPCLK[7..0]` (two on each I/O bank). EP1C3 devices have five `DPCLK` pins in the 100-pin TQFP package. These dual-purpose pins can connect to the global clock network (see Figure 2–22) for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables, or protocol control signals such as `TRDY` and `IRDY` for PCI, or DQS signals for external memory interfaces.

Combined Resources

Each Cyclone device contains eight distinct dedicated clocking resources. The device uses multiplexers with these clocks to form six-bit buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. See Figure 2–23. Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

Figure 2–23. Global Clock Network Multiplexers



IOE clocks have row and column block regions. Six of the eight global clock resources feed to these row and column regions. Figure 2–24 shows the I/O clock regions.

External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (`CLK[3..0]`) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See Figure 2–25.

Table 2–8 shows the I/O standards supported by PLL input and output pins.

Table 2–8. PLL I/O Standards

I/O Standard	CLK Input	EXTCLK Output
3.3-V LVTTL/LVCMOS	✓	✓
2.5-V LVTTL/LVCMOS	✓	✓
1.8-V LVTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

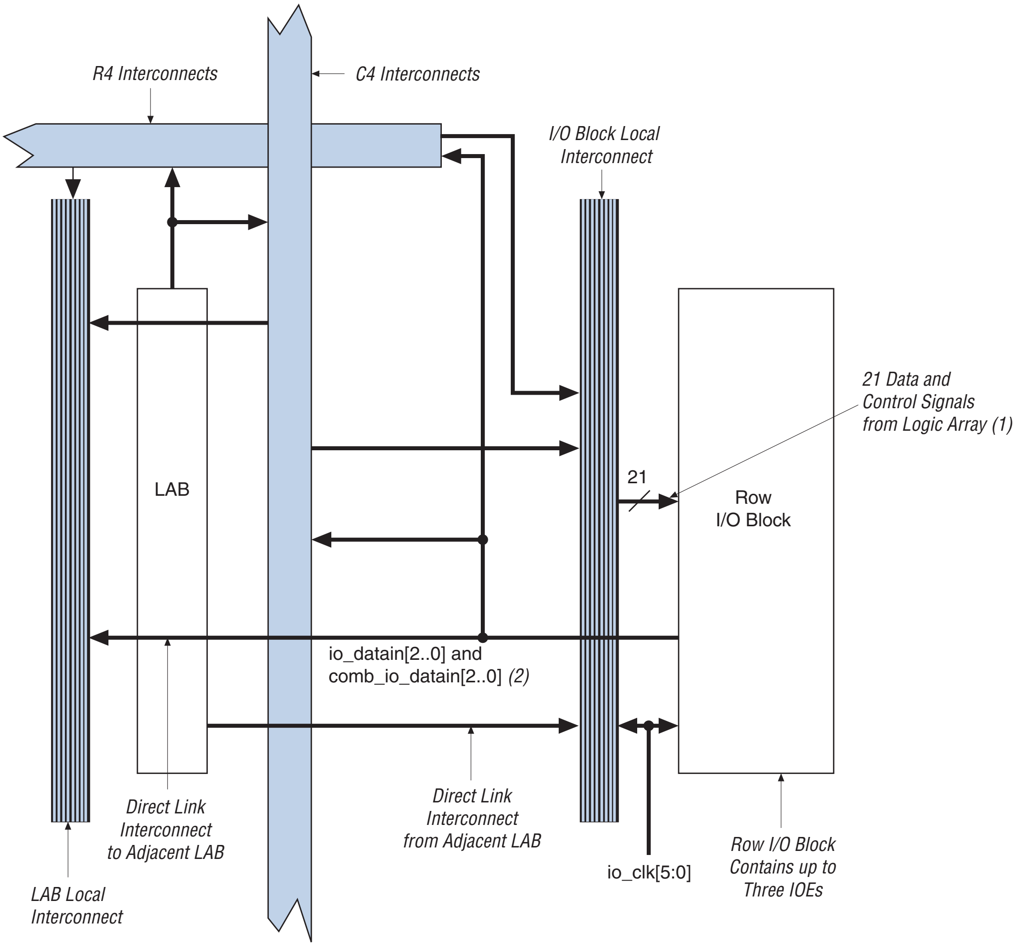
For more information on LVDS I/O support, refer to "LVDS I/O Pins" on page 2–54.

External Clock Outputs

Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these `PLL_OUT` pins, the pins are available for use as general-purpose I/O pins. The `PLL_OUT` pins support all I/O standards shown in Table 2–8.

The external clock outputs do not have their own V_{CC} and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

Figure 2–28. Row I/O Block Connection to the Interconnect

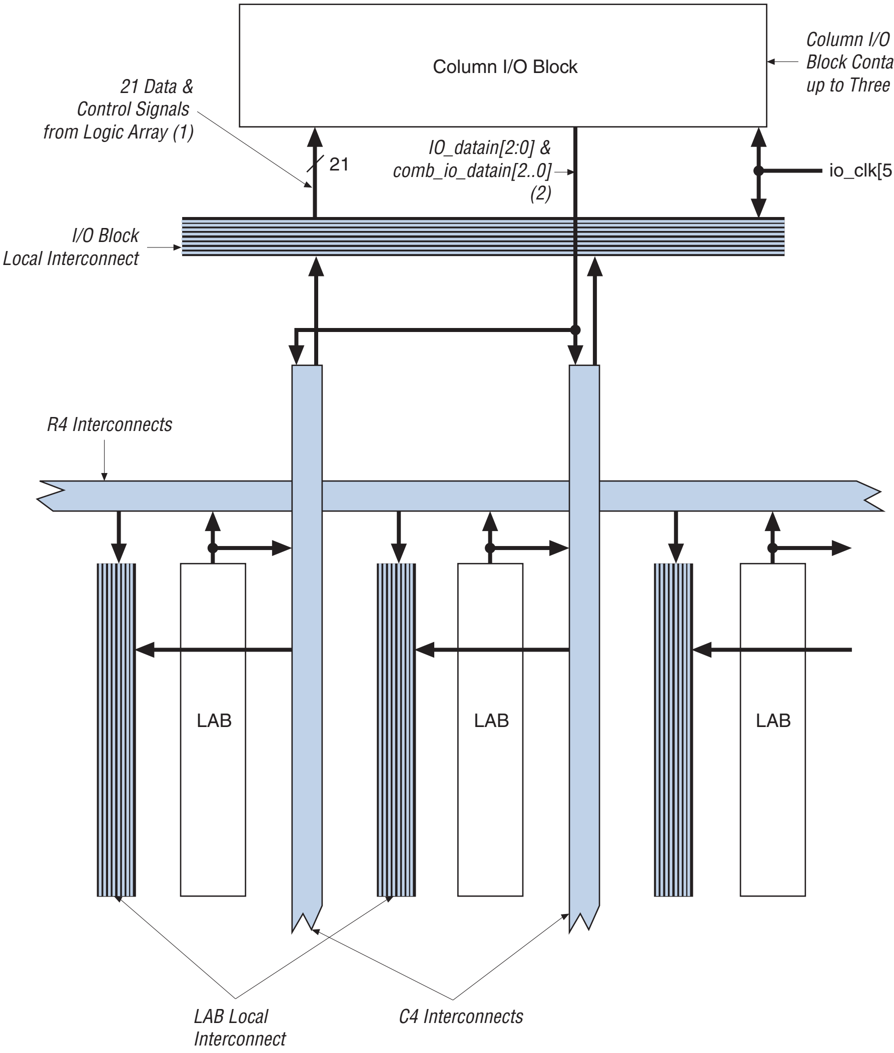


Notes to Figure 2–28:

(1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.

(2) Each of the three IOEs in the row I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

Figure 2–29. Column I/O Block Connection to the Interconnect



Notes to Figure 2–29:

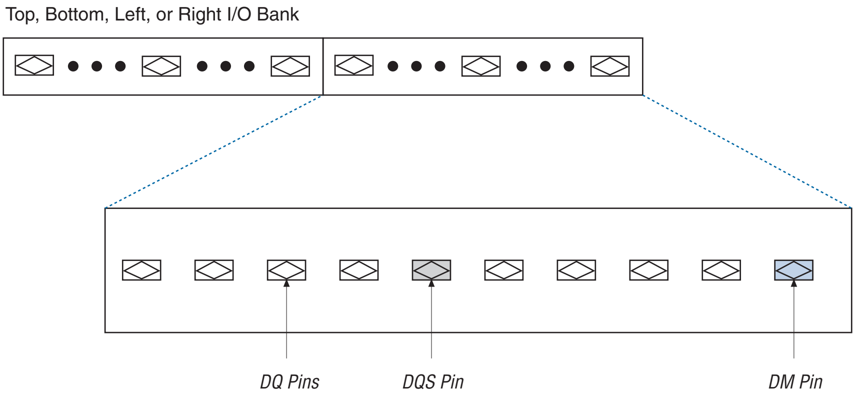
(1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.

(2) Each of the three IOEs in the column I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

output pins (`nSTATUS` and `CONF_DONE`) and all the JTAG pins in I/O bank 3 must operate at 2.5 V because the V_{CCIO} level of SSTL-2 is 2.5 V. I/O banks 1, 2, 3, and 4 support DQS signals with DQ bus modes of × 8.

For × 8 mode, there are up to eight groups of programmable DQS and DQ pins, I/O banks 1, 2, 3, and 4 each have two groups in the 324-pin and 400-pin FineLine BGA packages. Each group consists of one DQS pin, a set of eight DQ pins, and one DM pin (see Figure 2–33). Each DQS pin drives the set of eight DQ pins within that group.

Figure 2–33. Cyclone Device DQ and DQS Groups in ×8 Mode *Note (1)*



Note to Figure 2–33:

(1) Each DQ group consists of one DQS pin, eight DQ pins, and one DM pin.

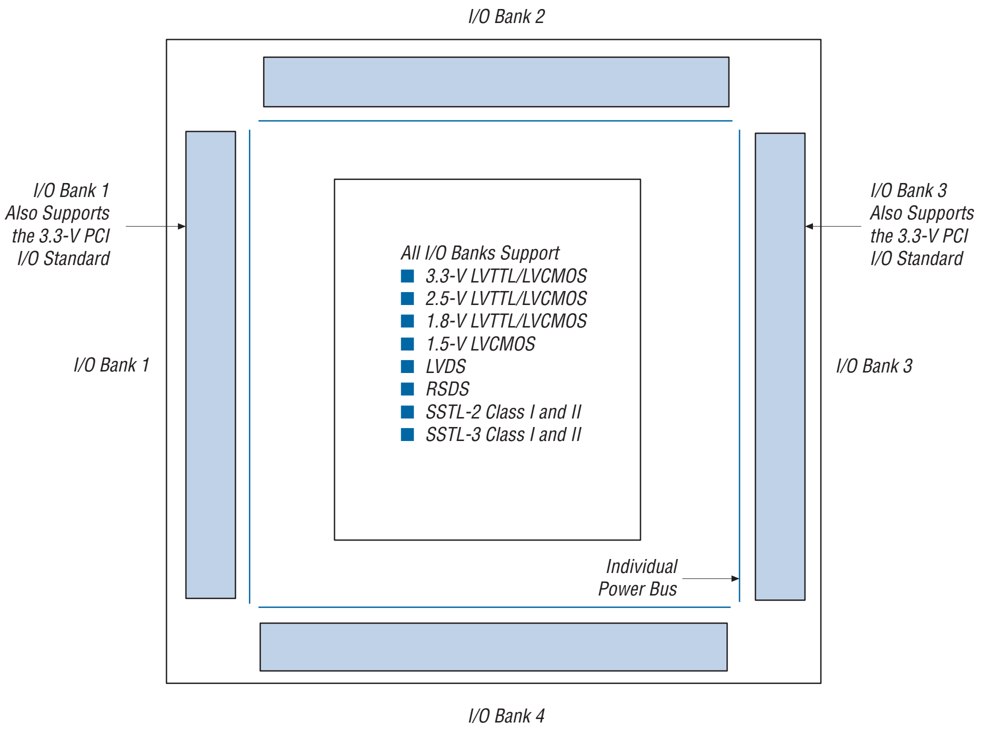
Table 2–10 shows the number of DQ pin groups per device.

Table 2–10. DQ Pin Groups (Part 1 of 2)

Device	Package	Number of × 8 DQ Pin Groups	Total DQ Pin Count
EP1C3	100-pin TQFP *(1)*	3	24
	144-pin TQFP	4	32
EP1C4	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

and DM pins to support a DDR SDRAM or FCRAM interface. I/O bank 1 can also support a DDR SDRAM or FCRAM interface, however, the configuration input pins in I/O bank 1 must operate at 2.5 V. I/O bank 3 can also support a DDR SDRAM or FCRAM interface, however, all the JTAG pins in I/O bank 3 must operate at 2.5 V.

Figure 2–35. Cyclone I/O Banks Notes (1), (2)



Notes to Figure 2–35:

(1) Figure 2–35 is a top view of the silicon die.

(2) Figure 2–35 is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard with different I/O voltages. Each bank also has dual-purpose `VREF` pins to support any one of the voltage-referenced standards (e.g., SSTL-3) independently. If an I/O bank does not use voltage-referenced standards, the V_{REF} pins are available as user I/O pins.

4. DC and Switching Characteristics

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Operating Conditions

Cyclone® devices are offered in both commercial, industrial, and extended temperature grades. However, industrial-grade and extended-temperature-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Cyclone devices.

Table 4–1. Cyclone Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_{CCA}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	BGA packages under bias	—	135	°C

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(5)*	–0.5	4.1	V

Table 4–10. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 × V_{CCIO}	V

Table 4–11. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.15	1.25	1.35	V
V_{IH}	High-level input voltage	—	V_{REF} + 0.18	—	3.0	V
V_{IL}	Low-level input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(11)*	V_{TT} + 0.57	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(11)*	—	—	V_{TT} – 0.57	V

Table 4–12. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.3	2.5	2.7	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.15	1.25	1.35	V
V_{IH}	High-level input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(11)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(11)*	—	—	V_{TT} – 0.76	V

Table 4–13. SSTL-3 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{TT}	Termination voltage	—	V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V

Table 4–16. Cyclone Device Capacitance *Note (14)*

Symbol	Parameter	Typical	Unit
C_{IO}	Input capacitance for user I/O pin	4.0	pF
C_{LVDS}	Input capacitance for dual-purpose LVDS/user I/O pin	4.7	pF
C_{VREF}	Input capacitance for dual-purpose V_{REF}/user I/O pin.	12.0	pF
C_{DPCLK}	Input capacitance for dual-purpose `DPCLK`/user I/O pin.	4.4	pF
C_{CLK}	Input capacitance for CLK pin.	4.7	pF

Notes to Tables 4–1 through 4–16:

(1) Refer to the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.

(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(7) V_I = ground, no load, no toggling inputs.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(9) R_{CONF} is the measured value of internal pull-up resistance when the I/O pin is tied directly to GND. R_{CONF} value will be lower if an external source drives the pin higher than V_{CCIO}.

(10) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

(11) Drive strength is programmable according to values in *Cyclone Architecture* chapter in the *Cyclone Device Handbook*.

(12) Overdrive is possible when a 1.5 V or 1.8 V and a 2.5 V or 3.3 V input signal feeds an input pin. Turn on “Allow voltage overdrive” for LVTTL/LVCMOS input pins in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combination. However, higher leakage current is expected.

(13) The Cyclone LVDS interface requires a resistor network outside of the transmitter channels.

(14) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

Table 4–52. Cyclone PLL Specifications (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
f_{OUT} (to global clock)	PLL output frequency (-6 speed grade)	15.625	405	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz
t_{OUT} DUTY	Duty cycle for external clock output (when set to 50%)	45.00	55	%
t_{JITTER} *(1)*	Period jitter for external clock output	—	±300 *(2)*	ps
t_{LOCK} *(3)*	Time required to lock from end of device configuration	10.00	100	µs
f_{VCO}	PLL internal VCO operating range	500.00	1,000	MHz
-	Minimum areset time	10	—	ns
N, G0, G1, E	Counter values	1	32	integer

Notes to Table 4–52:

(1) The t_{JITTER} specification for the `PLL[2..1]_OUT` pins are dependent on the I/O pins in its V_{CCIO} bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength or slow slew rate.

(2) $f_{OUT} \geq 100$ MHz. When the PLL external clock output frequency (f_{OUT}) is smaller than 100 MHz, the jitter specification is 60 mUI.

(3) $f_{IN/N}$ must be greater than 200 MHz to ensure correct lock detect circuit operation below –20 C. Otherwise, the PLL operates with the specified parameters under the specified conditions.

July 2003 v1.1	Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—