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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	291
Number of Logic Elements/Cells	2910
Total RAM Bits	59904
Number of I/O	104
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c3t144c7n

1. Introduction

C51001-1.5

Introduction

The Cyclone® field programmable gate array family is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 Kbits of RAM. With features like phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements, Cyclone devices are a cost-effective solution for data-path applications. Cyclone devices support various I/O standards, including LVDS at data rates up to 640 megabits per second (Mbps), and 66- and 33-MHz, 64- and 32-bit peripheral component interconnect (PCI), for interfacing with and supporting ASSP and ASIC devices. Altera also offers new low-cost serial configuration devices to configure Cyclone devices.

Features

The Cyclone device family offers the following features:

- 2,910 to 20,060 LEs, see Table 1–1
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66- and 33-MHz, 64- and 32-bit PCI standard
- High-speed (640 Mbps) LVDS I/O support
- Low-speed (311 Mbps) LVDS I/O support
- 311-Mbps RSDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz), FCRAM, and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) cores, including Altera® MegaCore® functions and Altera Megafunctions Partners Program (AMPP℠) megafunctions.

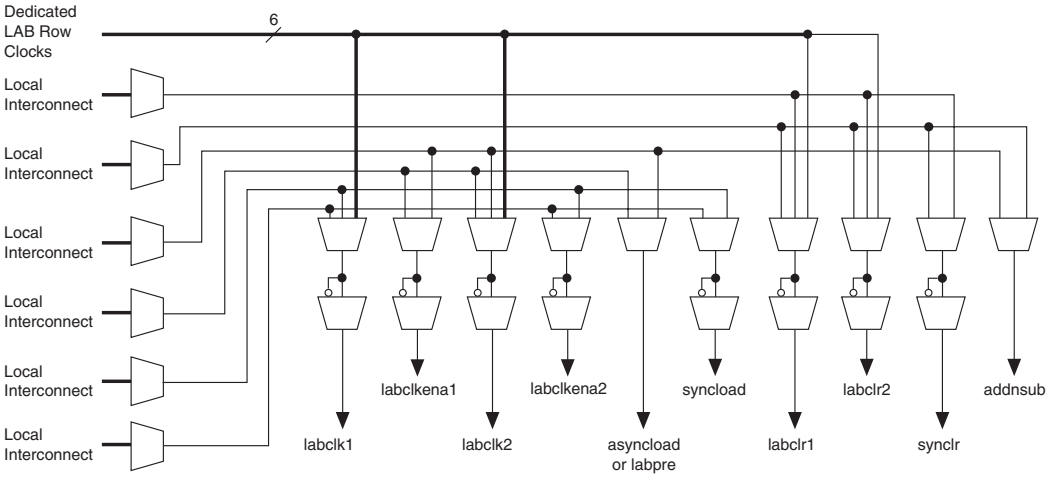
Table 1–1. Cyclone Device Features (Part 1 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
LEs	2,910	4,000	5,980	12,060	20,060
M4K RAM blocks (128 × 36 bits)	13	17	20	52	64

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

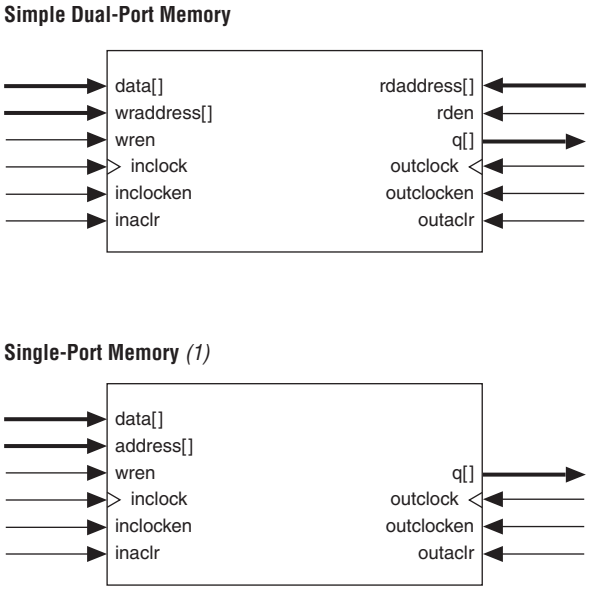
Table 2–2 shows the Cyclone device's routing scheme.

Table 2–2. Cyclone Device Routing Scheme

Source	Destination										
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	C4 Interconnect	LE	M4K RAM Block	PLL	Column IOE	Row IOE
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	✓
Direct Link Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	—	—	—
M4K RAM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
PLL	—	—	—	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

In addition to true dual-port memory, the M4K memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write. Single-port memory supports non-simultaneous reads and writes. Figure 2–13 shows these different M4K RAM memory port configurations.

Figure 2–13. Simple Dual-Port and Single-Port Memory Configurations



Note to Figure 2–13:

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

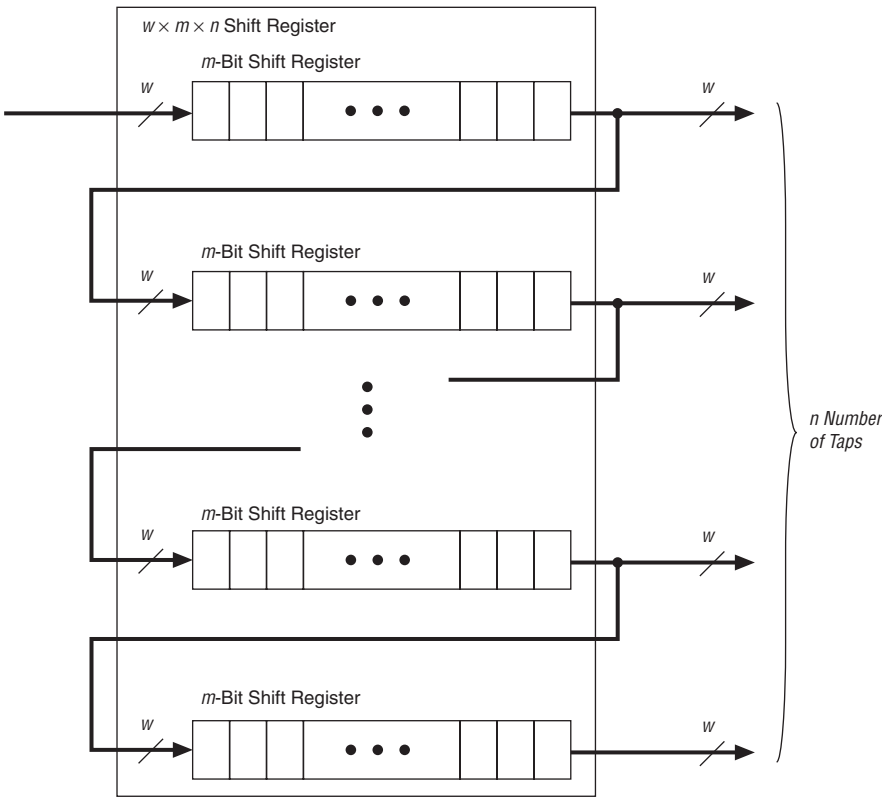
The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

The Cyclone memory architecture can implement fully synchronous RAM by registering both the input and output signals to the M4K RAM block. All M4K memory block inputs are registered, providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`wren`) signal derived from a global clock. In contrast, a circuit using asynchronous RAM must generate the RAM `wren` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `wren`

register outputs (number of taps n × width w) must be less than the maximum data width of the M4K RAM block (×36). To create larger shift registers, multiple memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 2–14 shows the M4K memory block in the shift register mode.

Figure 2–14. Shift Register Memory Configuration



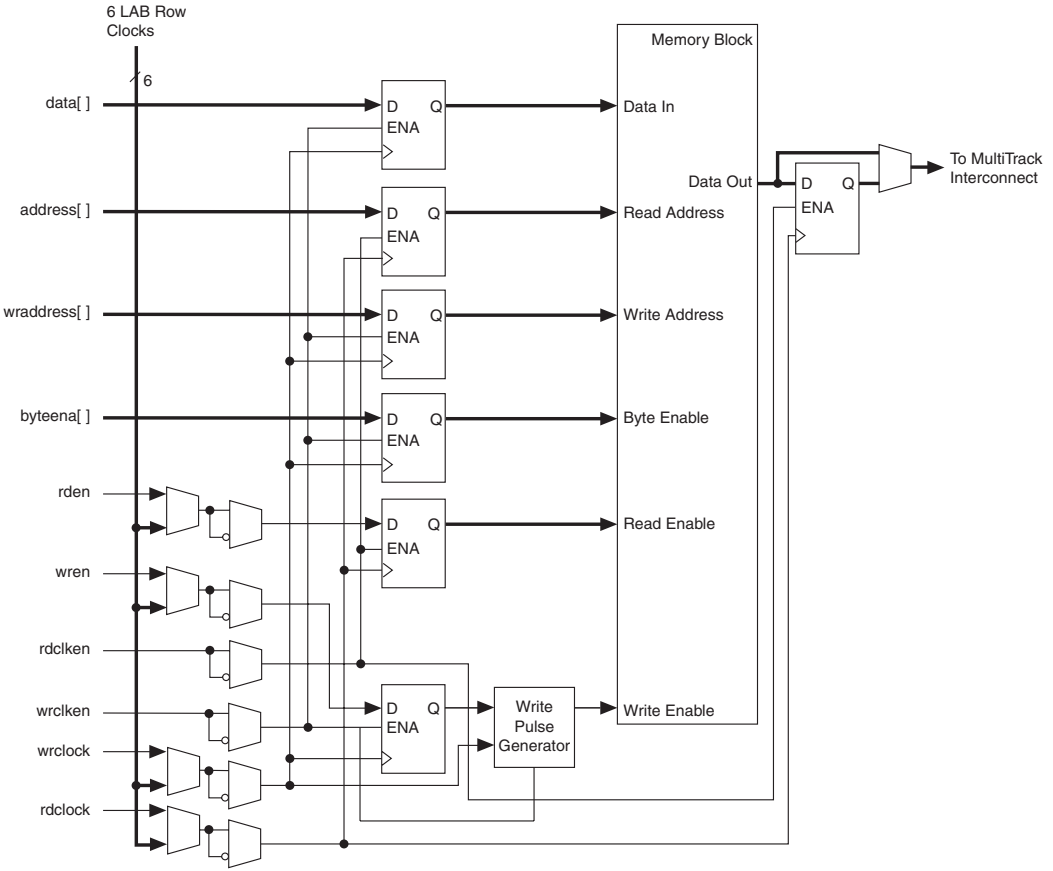
Memory Configuration Sizes

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration

Read/Write Clock Mode

The M4K memory blocks implement read/write clock mode for simple dual-port memory. You can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 2–20 shows a memory block in read/write clock mode.

Figure 2–20. Read/Write Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*

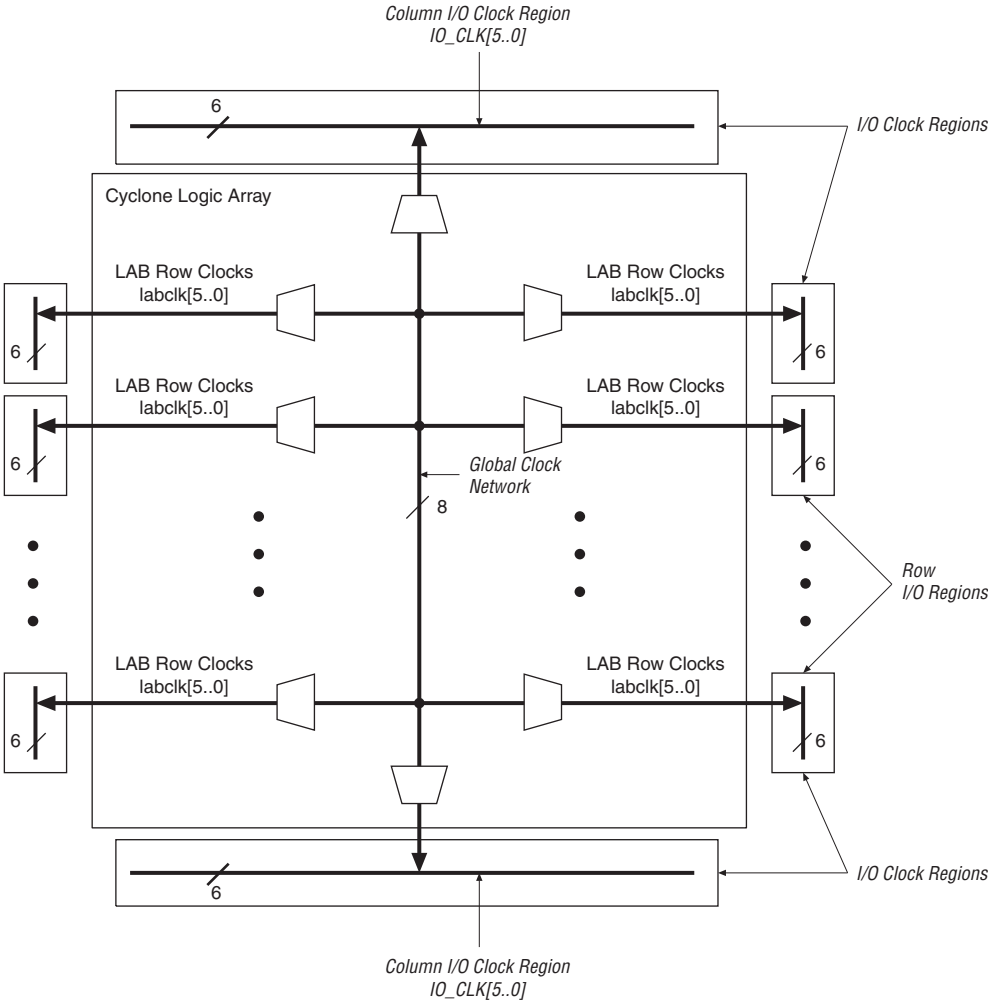


Notes to Figure 2–20:

(1) All registers shown except the rden register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Figure 2–24. I/O Clock Regions



PLLs

Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as outputs for differential I/O support. Cyclone devices contain two PLLs, except for the EP1C3 device, which contains one PLL.

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

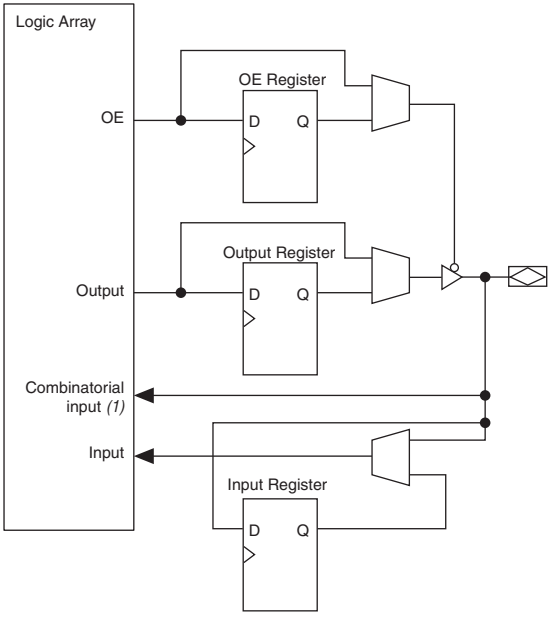
The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

Figure 2–27. Cyclone IOE Structure

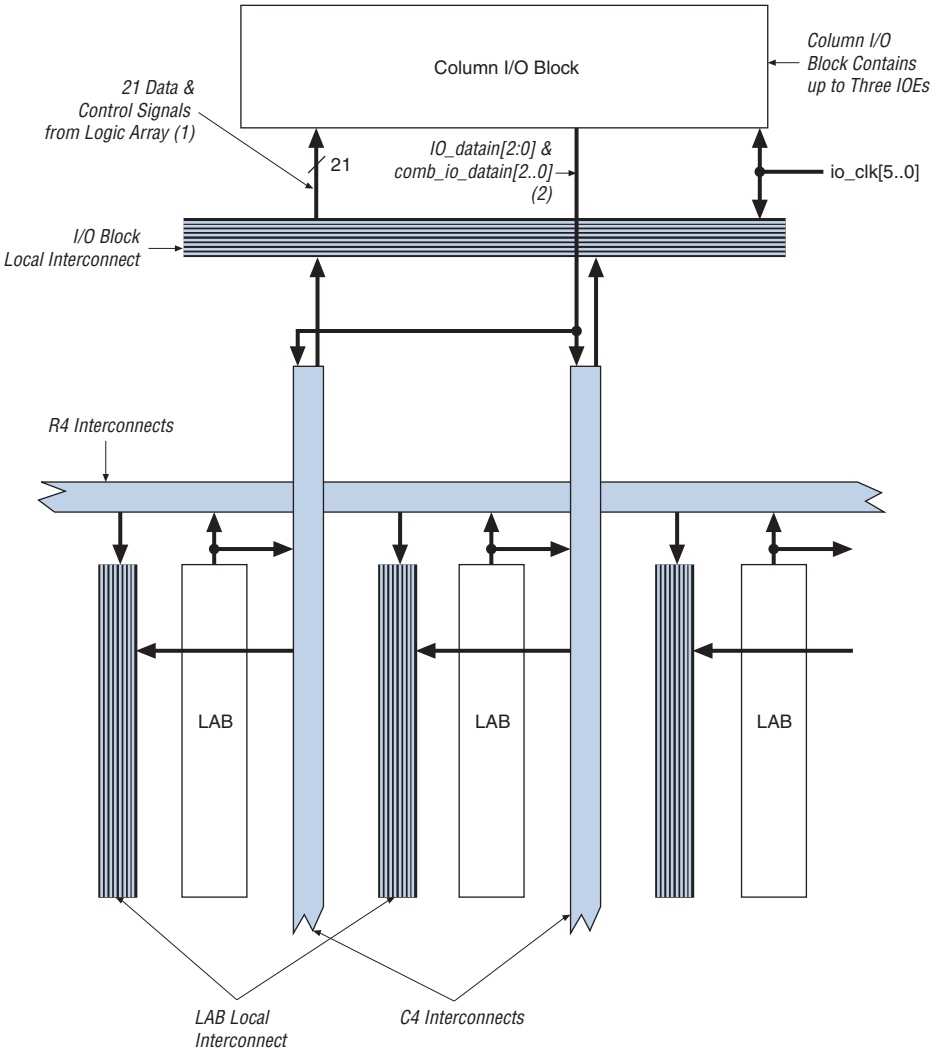


Note to Figure 2–27:

(1) There are two paths available for combinatorial inputs to the logic array. Each path contains a unique programmable delay chain.

The IOEs are located in I/O blocks around the periphery of the Cyclone device. There are up to three IOEs per row I/O block and up to three IOEs per column I/O block (column I/O blocks span two columns). The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–28 shows how a row I/O block connects to the logic array. Figure 2–29 shows how a column I/O block connects to the logic array.

Figure 2–29. Column I/O Block Connection to the Interconnect



Notes to Figure 2–29:

(1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.

(2) Each of the three IOEs in the column I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

The Cyclone device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone devices.

Table 3–2. Cyclone Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1C3	339
EP1C4	930
EP1C6	582
EP1C12	774
EP1C20	930

Table 3–3. 32-Bit Cyclone Device IDCODE

Device	IDCODE (32 bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1C3	0000	0010 0000 1000 0001	000 0110 1110	1
EP1C4	0000	0010 0000 1000 0101	000 0110 1110	1
EP1C6	0000	0010 0000 1000 0010	000 0110 1110	1
EP1C12	0000	0010 0000 1000 0011	000 0110 1110	1
EP1C20	0000	0010 0000 1000 0100	000 0110 1110	1

Notes to Table 3–3:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in Table 4–19.

Table 4–19. Clock Tree Maximum Performance Specification

Parameter	Definition	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock tree f_{MAX}	Maximum frequency that the clock tree can support for clocking registered logic	—	—	405	—	—	320	—	—	275	MHz

Table 4–20 shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
LE	16-to-1 multiplexer	—	21	—	—	405.00	320.00	275.00
	32-to-1 multiplexer	—	44	—	—	317.36	284.98	260.15
	16-bit counter	—	16	—	—	405.00	320.00	275.00
	64-bit counter *(1)*	—	66	—	—	208.99	181.98	160.75

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
M4K memory block	RAM 128 × 36 bit	Single port	—	4,608	1	256.00	222.67	197.01
	RAM 128 × 36 bit	Simple dual-port mode	—	4,608	1	255.95	222.67	196.97
	RAM 256 × 18 bit	True dual-port mode	—	4,608	1	255.95	222.67	196.97
	FIFO 128 × 36 bit	—	40	4,608	1	256.02	222.67	197.01
	Shift register 9 × 4 × 128	Shift register	11	4,536	1	255.95	222.67	196.97

Note to Table 4–20:
(1) The performance numbers for this function are from an EP1C6 device in a 240-pin PQFP package.

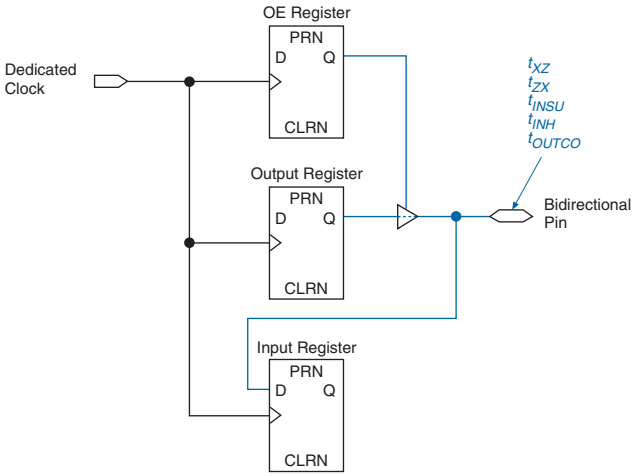
Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–21 through 4–24 describe the Cyclone device internal timing microparameters for LEs, IOEs, M4K memory structures, and MultiTrack interconnects.

Table 4–21. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Figure 4–2. External Timing in Cyclone Devices



All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–40 through 4–44.

Table 4–29 shows the external I/O timing parameters when using global clock networks.

Table 4–29. Cyclone Global Clock External I/O Timing Parameters *Notes (1), (2)* ***(Part 1 of 2)***

Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	—
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	—
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting	—
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting	—

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-3 class I	—	1,390	—	1,598	—	1,807	ps
SSTL-3 class II	—	989	—	1,137	—	1,285	ps
SSTL-2 class I	—	1,965	—	2,259	—	2,554	ps
SSTL-2 class II	—	1,692	—	1,945	—	2,199	ps
LVDS	—	802	—	922	—	1,042	ps

Note to Tables 4–40 through 4–45:
(1) EP1C3 devices do not support the PCI I/O standard.

Tables 4–46 through 4–47 show the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

Table 4–46. Cyclone IOE Programmable Delays on Column Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	155	—	178	—	201	ps
	Small	—	2,122	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	155	—	178	—	201	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	552	—	634	—	717	ps

Referenced Document

This chapter references the following documents:

- *Cyclone Architecture* chapter in the *Cyclone Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*

Document Revision History

Table 4–53 shows the revision history for this chapter.

Table 4–53. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.7	Minor textual and style changes. Added "Referenced Document" section.	—
January 2007 v1.6	• Added document revision history. • Added new row for V_{CCA} details in Table 4–1. • Updated R_{CONF} information in Table 4–3. • Added new *Note (12)* on voltage overdrive information to Table 4–7 and Table 4–8. • Updated *Note (9)* on R_{CONF} information to Table 4–3. • Updated information in "External I/O Delay Parameters" section. • Updated speed grade information in Table 4–46 and Table 4–47. • Updated LVDS information in Table 4–51.	—
August 2005 v1.5	Minor updates.	—
February 2005 v1.4	• Updated information on Undershoot voltage. Updated Table 4-2. • Updated Table 4-3. • Updated the undershoot voltage from 0.5 V to 2.0 V in Note 3 of Table 4-16. • Updated Table 4-17.	—
January 2004 v.1.3	• Added extended-temperature grade device information. Updated Table 4-2. • Updated I_{CC0} information in Table 4-3.	—
October 2003 v.1.2	• Added clock tree information in Table 4-19. • Finalized timing information for EP1C3 and EP1C12 devices. Updated timing information in Tables 4-25 through 4-26 and Tables 4-30 through 4-51. • Updated PLL specifications in Table 4-52.	—

5. Reference and Ordering Information

C51005-1.4

Software

Cyclone® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analysis, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

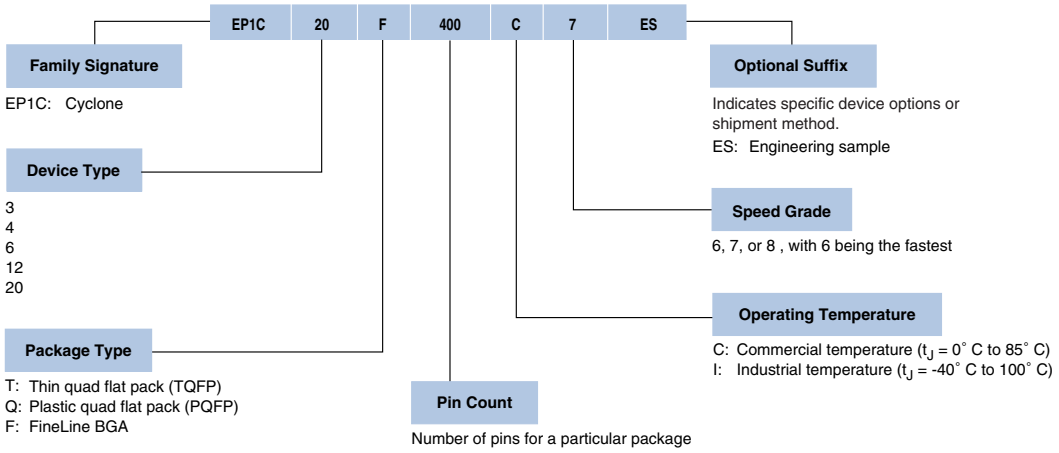
Device Pin-Outs

Device pin-outs for Cyclone devices are available on the Altera website (www.altera.com) and in the *Cyclone Device Handbook*.

Ordering Information

Figure 5–1 describes the ordering codes for Cyclone devices. For more information about a specific package, refer to the *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*.

Figure 5–1. Cyclone Device Packaging Ordering Information



Referenced Documents

This chapter references the following documents:

- *Package Information for Cyclone Devices* chapter in the *Cyclone Device Handbook*
- *Quartus II Handbook*

Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added "Referenced Documents" section.	—
January 2007 v1.3	Added document revision history.	—
August 2005 v1.2	Minor updates.	—