



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	291
Number of Logic Elements/Cells	2910
Total RAM Bits	59904
Number of I/O	104
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c3t144c8">https://www.e-xfl.com/product-detail/intel/ep1c3t144c8</a>



**Table 1–1. Cyclone Device Features (Part 2 of 2)**

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Total RAM bits	59,904	78,336	92,160	239,616	294,912
PLLs	1	2	2	2	2
Maximum user I/O pins (1)	104	301	185	249	301

**Note to Table 1–1:**

- (1) This parameter includes global clock pins.

Cyclone devices are available in quad flat pack (QFP) and space-saving FineLine® BGA packages (see Tables 1–2 through 1–3).

**Table 1–2. Cyclone Package Options and I/O Pin Counts**

Device	100-Pin TQFP (1)	144-Pin TQFP (1), (2)	240-Pin PQFP (1)	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
EP1C3	65	104	—	—	—	—
EP1C4	—	—	—	—	249	301
EP1C6	—	98	185	185	—	—
EP1C12	—	—	173	185	249	—
EP1C20	—	—	—	—	233	301

**Notes to Table 1–2:**

- (1) TQFP: thin quad flat pack.  
PQFP: plastic quad flat pack.
- (2) Cyclone devices support vertical migration within the same package (i.e., designers can migrate between the EP1C3 device in the 144-pin TQFP package and the EP1C6 device in the same package).

Vertical migration means you can migrate a design from one device to another that has the same dedicated pins, JTAG pins, and power pins, and are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must use the layout for the largest planned density in a package to provide the necessary power pins for migration.

For I/O pin migration across densities, cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list. If one device has power or ground pins, but these same pins are user I/O on a different device that is in the migration path, the Quartus II software ensures the pins are not used as user I/O in the Quartus II software. Ensure that these pins are connected

to the appropriate plane on the board. The Quartus II software reserves I/O pins as power pins as necessary for layout with the larger densities in the same package having more power pins.

**Table 1–3. Cyclone QFP and FineLine BGA Package Sizes**

Dimension	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0.5	0.5	0.5	1.0	1.0	1.0
Area (mm <sup>2</sup> )	256	484	1,024	289	361	441
Length × width (mm × mm)	16×16	22×22	34.6×34.6	17×17	19×19	21×21

## Document Revision History

Table 1–4 shows the revision history for this document.

**Table 1–4. Document Revision History**

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.5	Minor textual and style changes.	—
January 2007 v1.4	Added document revision history.	—
August 2005 v1.3	Minor updates.	—
October 2003 v1.2	Added 64-bit PCI support information.	—
September 2003 v1.1	<ul style="list-style-type: none"> <li>Updated LVDS data rates to 640 Mbps from 311 Mbps.</li> <li>Updated RSDS feature information.</li> </ul>	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

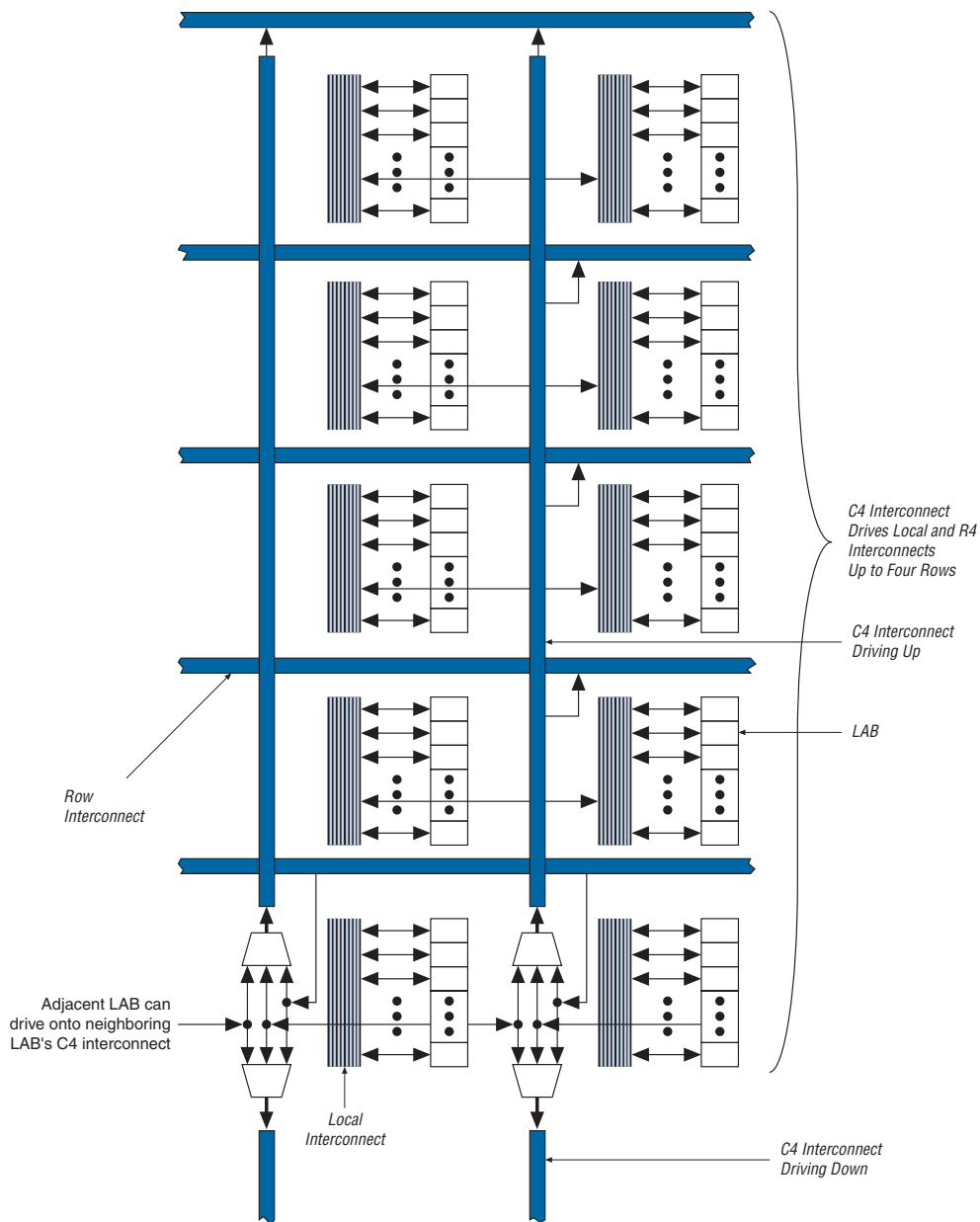


migrating through different device densities. Dedicated row interconnects route signals to and from LABs, PLLs, and M4K memory blocks within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left

The direct link interconnect allows a LAB or M4K memory block to drive into the local interconnect of its left and right neighbors. Only one side of a PLL block interfaces with direct link and row interconnects. The direct link interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, or two LABs and one M4K RAM block. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. [Figure 2–9](#) shows R4 interconnect connections from a LAB. R4 interconnects can drive and be driven by M4K memory blocks, PLLs, and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

**Figure 2–11. C4 Interconnect Connections** *Note (1)***Note to Figure 2–11:**

(1) Each C4 interconnect can drive either up or down four rows.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–2 shows the Cyclone device's routing scheme.

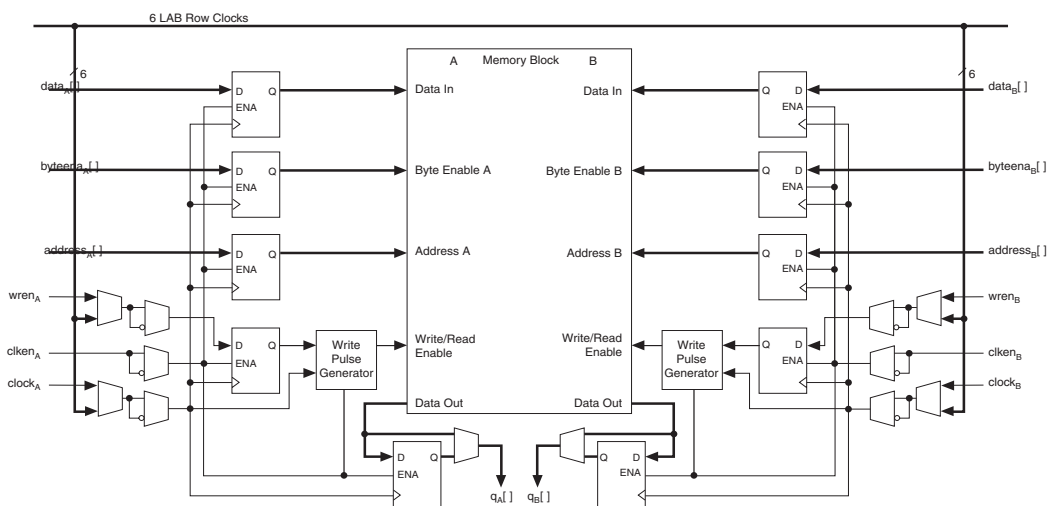
<b>Table 2–2. Cyclone Device Routing Scheme</b>											
<b>Source</b>	<b>Destination</b>										
	<b>LUT Chain</b>	<b>Register Chain</b>	<b>Local Interconnect</b>	<b>Direct Link Interconnect</b>	<b>R4 Interconnect</b>	<b>C4 Interconnect</b>	<b>LE</b>	<b>M4K RAM Block</b>	<b>PLL</b>	<b>Column IOE</b>	<b>Row IOE</b>
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	✓
Direct Link Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	—	—	—
M4K RAM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
PLL	—	—	—	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—



## Independent Clock Mode

The M4K memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–17 shows an M4K memory block in independent clock mode.

**Figure 2–17. Independent Clock Mode** Notes (1), (2)



Notes to Figure 2–17:

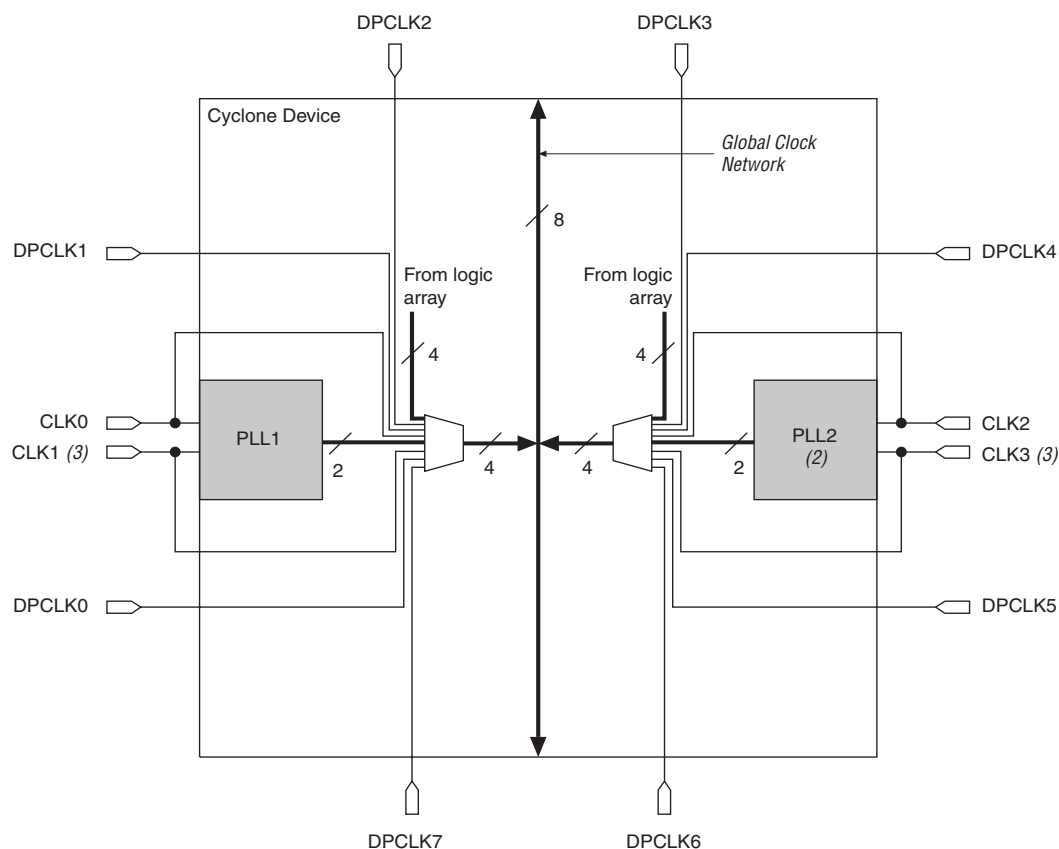
- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

## Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, wren, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–18 and 2–19 show the memory block in input/output clock mode.

The eight global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device—IOEs, LEs, and memory blocks. The global clock lines can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin, or DQS signals for DDR SDRAM or FCRAM interfaces. Internal logic can also drive the global clock network for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–22 shows the various sources that drive the global clock network.

**Figure 2–22. Global Clock Generation** *Note (1)*



**Notes to Figure 2–22:**

- (1) The EP1C3 device in the 100-pin TQFP package has five DPCLK pins (DPCLK2, DPCLK3, DPCLK4, DPCLK6, and DPCLK7).
- (2) EP1C3 devices only contain one PLL (PLL 1).
- (3) The EP1C3 device in the 100-pin TQFP package does not have dedicated clock pins CLK1 and CLK3.

## External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (CLK[3..0]) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See [Figure 2-25](#).

[Table 2-8](#) shows the I/O standards supported by PLL input and output pins.

<b>Table 2-8. PLL I/O Standards</b>		
<b>I/O Standard</b>	<b>CLK Input</b>	<b>EXTCLK Output</b>
3.3-V LVTTTL/LVCMOS	✓	✓
2.5-V LVTTTL/LVCMOS	✓	✓
1.8-V LVTTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

For more information on LVDS I/O support, refer to “[LVDS I/O Pins](#)” on [page 2-54](#).

## External Clock Outputs

Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these PLL\_OUT pins, the pins are available for use as general-purpose I/O pins. The PLL\_OUT pins support all I/O standards shown in [Table 2-8](#).

The external clock outputs do not have their own V<sub>CC</sub> and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

does not have dedicated clock output pins. The EP1C6 device in the 144-pin TQFP package only supports dedicated clock outputs from PLL 1.

## Clock Feedback

Cyclone PLLs have three modes for multiplication and/or phase shifting:

- Zero delay buffer mode—The external clock output pin is phase-aligned with the clock input pin for zero delay.
- Normal mode—If the design uses an internal PLL clock output, the normal mode compensates for the internal clock delay from the input clock pin to the IOE registers. The external clock output pin is phase shifted with respect to the clock input pin if connected in this mode. You defines which internal clock output from the PLL should be phase-aligned to compensate for internal clock delay.
- No compensation mode—In this mode, the PLL will not compensate for any clock networks.

## Phase Shifting

Cyclone PLLs have an advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 125 to 250 ps. The finest resolution equals one eighth of the VCO period. The VCO period is a function of the frequency input and the multiplication and division factors. Each clock output counter can choose a different phase of the VCO period from up to eight taps. You can use this clock output counter along with an initial setting on the post-scale counter to achieve a phase-shift range for the entire period of the output clock. The phase tap feedback to the m counter can shift all outputs to a single phase. The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entered.

## Lock Detect Signal

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. Therefore, you may need to gate the lock signal for use as a system-control signal. For correct operation of the lock circuit below  $-20^{\circ}\text{C}$ ,  $f_{\text{IN}/N} > 200\text{ MHz}$ .

Each I/O bank can support multiple standards with the same  $V_{CCIO}$  for input and output pins. For example, when  $V_{CCIO}$  is 3.3-V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

## LVDS I/O Pins

A subset of pins in all four I/O banks supports LVDS interfacing. These dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100- $\Omega$  termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry; therefore, internal logic performs serialization and deserialization functions.

Table 2–13 shows the total number of supported LVDS channels per device density.

<b>Table 2–13. Cyclone Device LVDS Channels</b>		
<b>Device</b>	<b>Pin Count</b>	<b>Number of LVDS Channels</b>
EP1C3	100	(1)
	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

**Note to Table 2–13:**

- (1) EP1C3 devices in the 100-pin TQFP package do not support the LVDS I/O standard.

## MultiVolt I/O Interface

The Cyclone architecture supports the MultiVolt I/O interface feature, which allows Cyclone devices in all packages to interface with systems of different supply voltages. The devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and four sets for I/O output drivers ( $V_{CCIO}$ ).

## Referenced Documents

This chapter references the following document:

- *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*

## Document Revision History

Table 2–15 shows the revision history for this chapter.

<b>Table 2–15. Document Revision History</b>		
<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2008 v1.6	Minor textual and style changes. Added “Referenced Documents” section.	—
January 2007 v1.5	<ul style="list-style-type: none"> <li>● Added document revision history.</li> <li>● Updated Figures 2–17, 2–18, 2–19, 2–20, 2–21, and 2–32.</li> </ul>	—
August 2005 v1.4	Minor updates.	—
February 2005 v1.3	<ul style="list-style-type: none"> <li>● Updated JTAG chain limits. Added test vector information.</li> <li>● Corrected Figure 2-12.</li> <li>● Added a note to Tables 2-17 through 2-21 regarding violating the setup or hold time.</li> </ul>	—
October 2003 v1.2	<ul style="list-style-type: none"> <li>● Updated phase shift information.</li> <li>● Added 64-bit PCI support information.</li> </ul>	—
September 2003 v1.1	Updated LVDS data rates to 640 Mbps from 311 Mbps.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Figure 3–1 shows the timing requirements for the JTAG signals.

**Figure 3–1. Cyclone JTAG Waveforms**

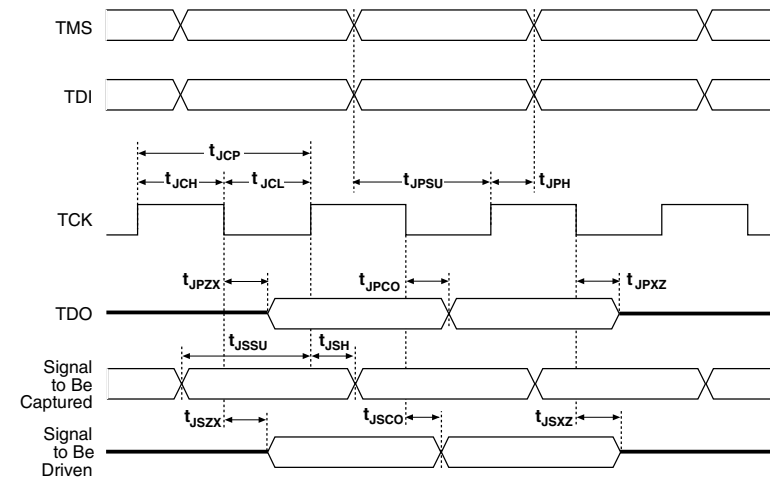


Table 3–4 shows the JTAG timing parameters and values for Cyclone devices.

<b>Table 3–4. Cyclone JTAG Timing Parameters and Values</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100	—	ns
$t_{JCH}$	TCK clock high time	50	—	ns
$t_{JCL}$	TCK clock low time	50	—	ns
$t_{JPSU}$	JTAG port setup time	20	—	ns
$t_{JPH}$	JTAG port hold time	45	—	ns
$t_{JPCO}$	JTAG port clock to output	—	25	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	25	ns
$t_{JSSU}$	Capture register setup time	20	—	ns
$t_{JSH}$	Capture register hold time	45	—	ns
$t_{JSCO}$	Update register clock to output	—	35	ns
$t_{JSZX}$	Update register high impedance to valid output	—	35	ns
$t_{JSXZ}$	Update register valid output to high impedance	—	35	ns

Multiple Cyclone devices can be configured in any of the three configuration schemes by connecting the configuration enable ( $nCE$ ) and configuration enable output ( $nCEO$ ) pins on each device.

**Table 3–5. Data Sources for Configuration**

Configuration Scheme	Data Source
Active serial	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster or ByteBlasterMV download cable, or serial data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file

## Referenced Documents

This chapter references the following document:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

## Document Revision History

Table 3–6 shows the revision history for this chapter.

**Table 3–6. Document Revision History**

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added “Referenced Documents” section.	—
January 2007 v1.3	<ul style="list-style-type: none"> <li>● Added document revision history.</li> <li>● Updated handpara note below Table 3–4.</li> </ul>	—
August 2005 V1.2	Minor updates.	—
February 2005 V1.1	Updated JTAG chain limits. Added information concerning test vectors.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—



**Table 4–20. Cyclone Device Performance**

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
M4K memory block	RAM 128 × 36 bit	Single port	—	4,608	1	256.00	222.67	197.01
	RAM 128 × 36 bit	Simple dual-port mode	—	4,608	1	255.95	222.67	196.97
	RAM 256 × 18 bit	True dual-port mode	—	4,608	1	255.95	222.67	196.97
	FIFO 128 × 36 bit	—	40	4,608	1	256.02	222.67	197.01
	Shift register 9 × 4 × 128	Shift register	11	4,536	1	255.95	222.67	196.97

*Note to Table 4–20:*

(1) The performance numbers for this function are from an EP1C6 device in a 240-pin PQFP package.

## Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–21 through 4–24 describe the Cyclone device internal timing microparameters for LEs, IOEs, M4K memory structures, and MultiTrack interconnects.

**Table 4–21. LE Internal Timing Microparameter Descriptions**

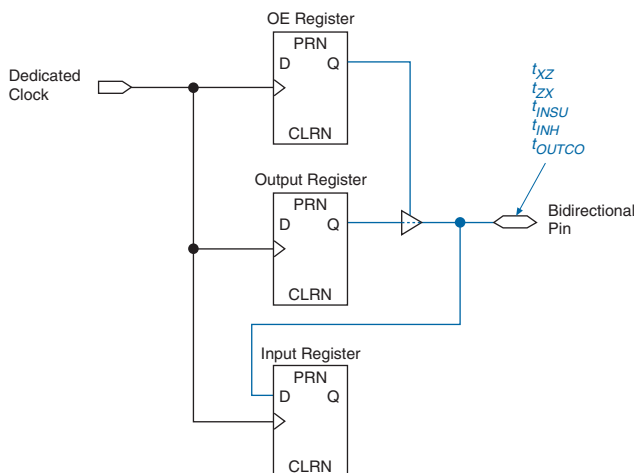
Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LE combinatorial LUT delay for data-in to data-out
$t_{CLR}$	Minimum clear pulse width
$t_{PRE}$	Minimum preset pulse width
$t_{CLKHL}$	Minimum clock high or low time

**Table 4–22. IOE Internal Timing Microparameter Descriptions**

Symbol	Parameter
$t_{SU}$	IOE input and output register setup time before clock
$t_H$	IOE input and output register hold time after clock
$t_{CO}$	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
$t_{CLR}$	Minimum clear pulse width
$t_{PRE}$	Minimum preset pulse width
$t_{CLKHL}$	Minimum clock high or low time

**Table 4–23. M4K Block Internal Timing Microparameter Descriptions**

Symbol	Parameter
$t_{M4KRC}$	Synchronous read cycle time
$t_{M4KWC}$	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
$t_{M4KBEH}$	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATAO1}$	Clock-to-output delay when using output registers
$t_{M4KDATAO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
$t_{M4KCLR}$	Minimum clear pulse width

**Figure 4–2. External Timing in Cyclone Devices**

All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in [Tables 4–40 through 4–44](#).

[Table 4–29](#) shows the external I/O timing parameters when using global clock networks.

<b>Table 4–29. Cyclone Global Clock External I/O Timing Parameters</b> <i>Notes (1), (2) (Part 1 of 2)</i>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{INSU}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	—
$t_{INH}$	Hold time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	—
$t_{OUTCO}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by CLK pin	$C_{LOAD} = 10 \text{ pF}$
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting	—
$t_{INHPLL}$	Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting	—

**Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)**

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-3 class I	—	1,390	—	1,598	—	1,807	ps
SSTL-3 class II	—	989	—	1,137	—	1,285	ps
SSTL-2 class I	—	1,965	—	2,259	—	2,554	ps
SSTL-2 class II	—	1,692	—	1,945	—	2,199	ps
LVDS	—	802	—	922	—	1,042	ps

Note to [Tables 4–40 through 4–45](#):

- (1) EP1C3 devices do not support the PCI I/O standard.

[Tables 4–46 through 4–47](#) show the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

**Table 4–46. Cyclone IOE Programmable Delays on Column Pins**

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	155	—	178	—	201	ps
	Small	—	2,122	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	155	—	178	—	201	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	552	—	634	—	717	ps

**Table 4–47. Cyclone IOE Programmable Delays on Row Pins**

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off	—	154	—	177	—	200	ps
	Small	—	2,212	—	2,543	—	2,875	ps
	Medium	—	2,639	—	3,034	—	3,430	ps
	Large	—	3,057	—	3,515	—	3,974	ps
	On	—	154	—	177	—	200	ps
Decrease input delay to input register	Off	—	0	—	0	—	0	ps
	On	—	3,057	—	3,515	—	3,974	ps
Increase delay to output pin	Off	—	0	—	0	—	0	ps
	On	—	556	—	639	—	722	ps

*Note to Table 4–47:*

- (1) EPC1C3 devices do not support the PCI I/O standard.

## Maximum Input and Output Clock Rates

Tables 4–48 and 4–49 show the maximum input clock rate for column and row pins in Cyclone devices.

**Table 4–48. Cyclone Maximum Input Clock Rate for Column Pins**

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVC MOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
LVDS	567	549	531	MHz