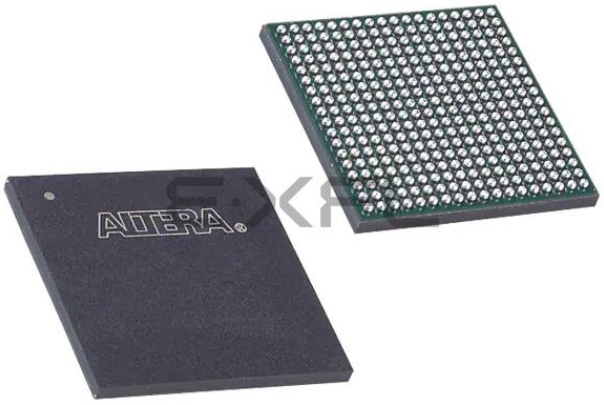


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	4000
Total RAM Bits	78336
Number of I/O	249
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c4f324c6n

Table 1–1. Cyclone Device Features (Part 2 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Total RAM bits	59,904	78,336	92,160	239,616	294,912
PLLs	1	2	2	2	2
Maximum user I/O pins *(1)*	104	301	185	249	301

Note to Table 1–1:
(1) This parameter includes global clock pins.

Cyclone devices are available in quad flat pack (QFP) and space-saving FineLine® BGA packages (see Tables 1–2 through 1–3).

Table 1–2. Cyclone Package Options and I/O Pin Counts

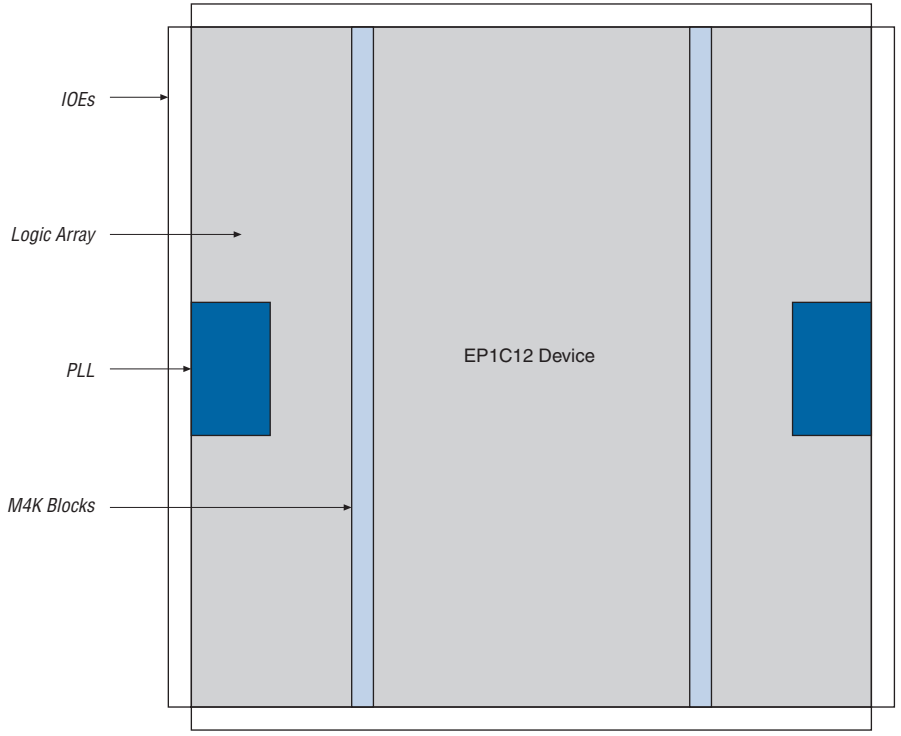
Device	100-Pin TQFP *(1)*	144-Pin TQFP *(1), (2)*	240-Pin PQFP *(1)*	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
EP1C3	65	104	—	—	—	—
EP1C4	—	—	—	—	249	301
EP1C6	—	98	185	185	—	—
EP1C12	—	—	173	185	249	—
EP1C20	—	—	—	—	233	301

Notes to Table 1–2:
(1) TQFP: thin quad flat pack.
PQFP: plastic quad flat pack.
(2) Cyclone devices support vertical migration within the same package (i.e., designers can migrate between the EP1C3 device in the 144-pin TQFP package and the EP1C6 device in the same package).

Vertical migration means you can migrate a design from one device to another that has the same dedicated pins, JTAG pins, and power pins, and are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must use the layout for the largest planned density in a package to provide the necessary power pins for migration.

For I/O pin migration across densities, cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list. If one device has power or ground pins, but these same pins are user I/O on a different device that is in the migration path,the Quartus II software ensures the pins are not used as user I/O in the Quartus II software. Ensure that these pins are connected

Figure 2–1. Cyclone EP1C12 Device Block Diagram



The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

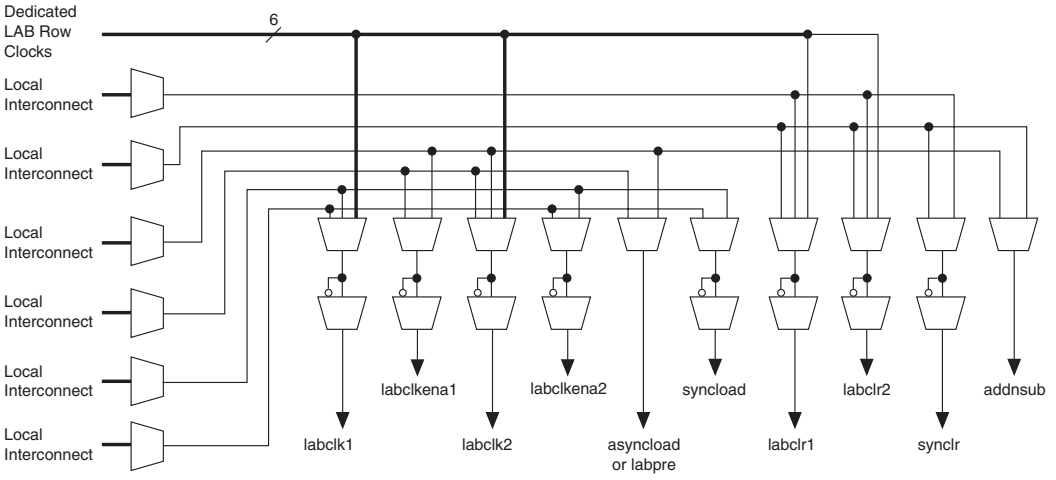
Table 2–1. Cyclone Device Resources

Device	M4K RAM		PLLs	LAB Columns	LAB Rows
	Columns	Blocks			
EP1C3	1	13	1	24	13
EP1C4	1	17	2	26	17
EP1C6	1	20	2	32	20
EP1C12	2	52	2	48	26
EP1C20	2	64	2	64	32

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to M4K memory blocks. A carry chain can continue as far as a full column.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Cyclone devices support simultaneous preset/ asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Cyclone devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

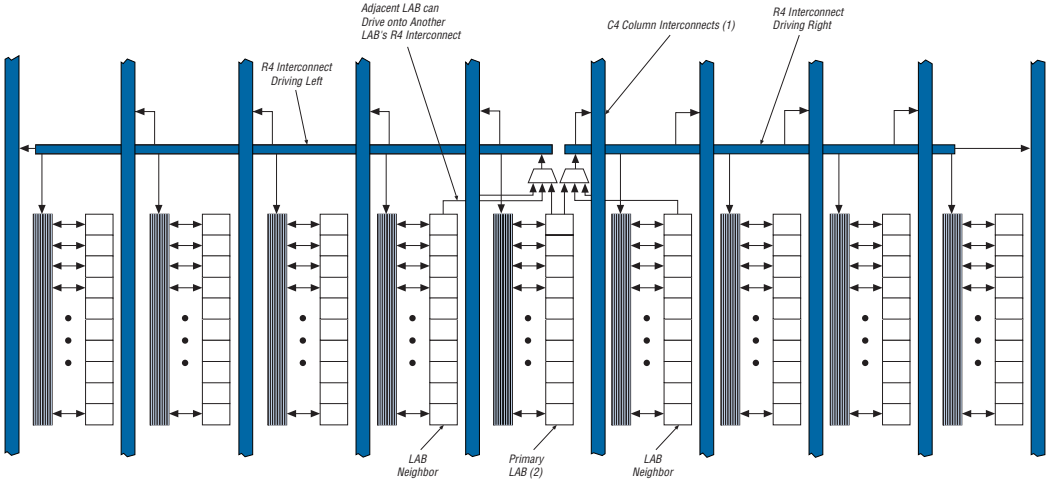
MultiTrack Interconnect

In the Cyclone architecture, connections between LEs, M4K memory blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when

Figure 2–9. R4 Interconnect Connections



Notes to Figure 2–9:
(1) C4 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, M4K memory blocks, and row and column IOEs. These column resources include:

- LUT chain interconnects within a LAB
- Register chain interconnects within a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction

Cyclone devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–2 shows the Cyclone device's routing scheme.

Table 2–2. Cyclone Device Routing Scheme

Source	Destination										
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	C4 Interconnect	LE	M4K RAM Block	PLL	Column IOE	Row IOE
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	✓
Direct Link Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	—	—	—
M4K RAM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
PLL	—	—	—	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Embedded Memory

The Cyclone embedded memory consists of columns of M4K memory blocks. EP1C3 and EP1C6 devices have one column of M4K blocks, while EP1C12 and EP1C20 devices have two columns (refer to Table 1–1 on page 1–1 for total RAM bits per density). Each M4K block can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. The M4K blocks support the following features:

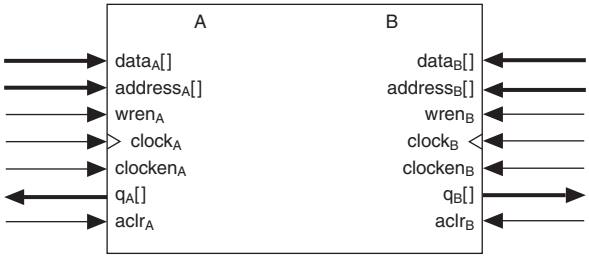
- 4,608 RAM bits
- 250 MHz performance
- True dual-port memory
- Simple dual-port memory
- Single-port memory
- Byte enable
- Parity bits
- Shift register
- FIFO buffer
- ROM
- Mixed clock mode

Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Memory Modes

The M4K memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 2–12 shows true dual-port memory.

Figure 2–12. True Dual-Port Memory Configuration



signal. The output registers can be bypassed. Pseudo-asynchronous reading is possible in the simple dual-port mode of M4K blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple M4K memory blocks. For example, two 256×16-bit RAM blocks can be combined to form a 256×32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words allowed. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

Parity Bit Support

The M4K blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. Byte enables are also available for data input masking during write operations.

Shift Register Support

You can configure M4K memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a $w \times m \times n$ shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n). The size of a $w \times m \times n$ shift register must be less than or equal to the maximum number of memory bits in the M4K block (4,608 bits). The total number of shift

is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)

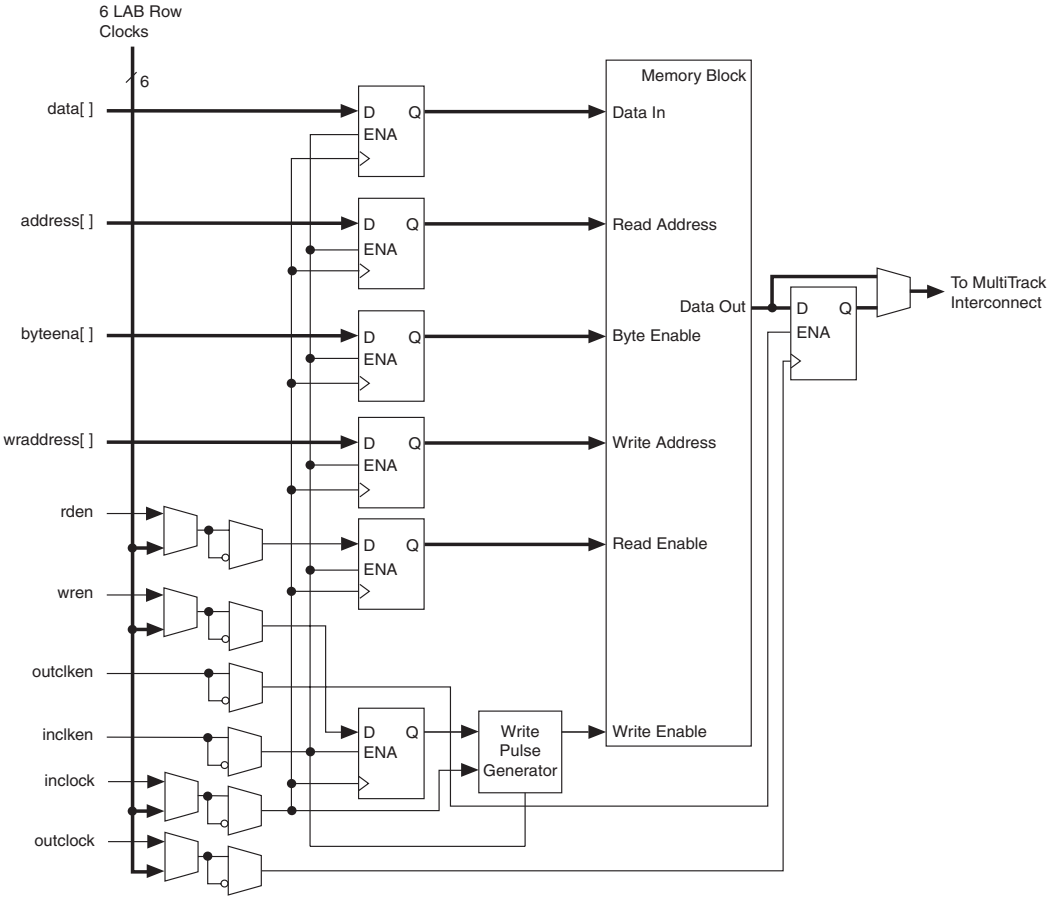
Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

Table 2–4. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 2–19. Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*



Notes to Figure 2–19:

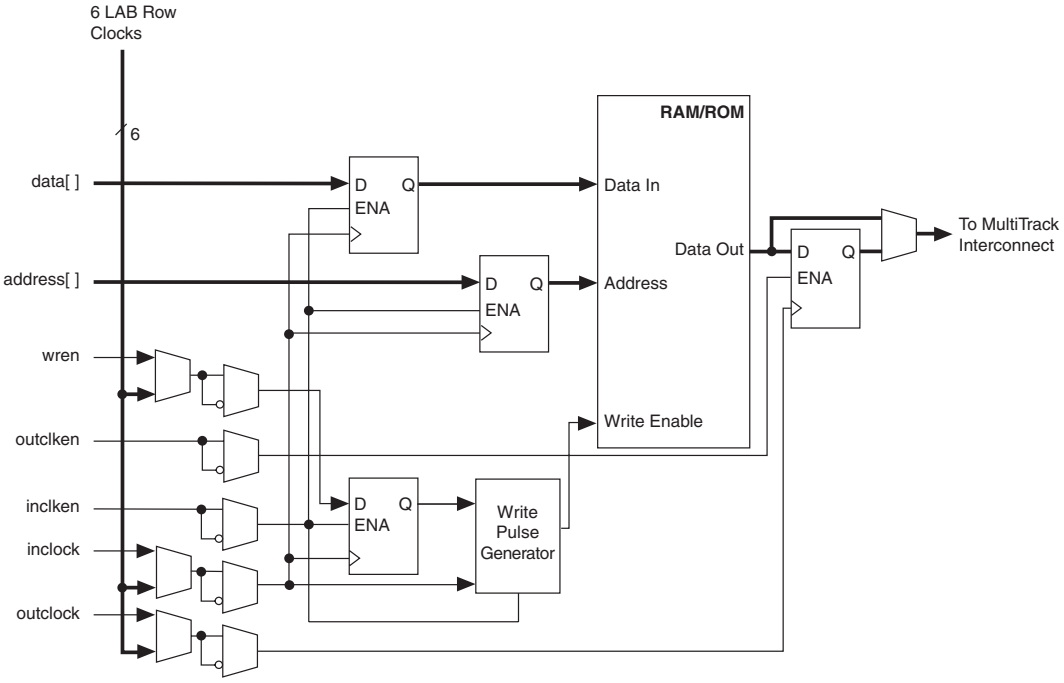
(1) All registers shown except the rden register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Single-Port Mode

The M4K memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–21. A single M4K memory block can support up to two single-port mode RAM blocks if each RAM block is less than or equal to 2K bits in size.

Figure 2–21. Single-Port Mode *Note (1)*



Note to Figure 2–21:

(1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Global Clock Network and Phase-Locked Loops

Cyclone devices provide a global clock network and up to two PLLs for a complete clock management solution.

Global Clock Network

There are four dedicated clock pins (`CLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network, as shown in Figure 2–22. PLL outputs, logic array, and dual-purpose clock (`DPCLK[7..0]`) pins can also drive the global clock network.

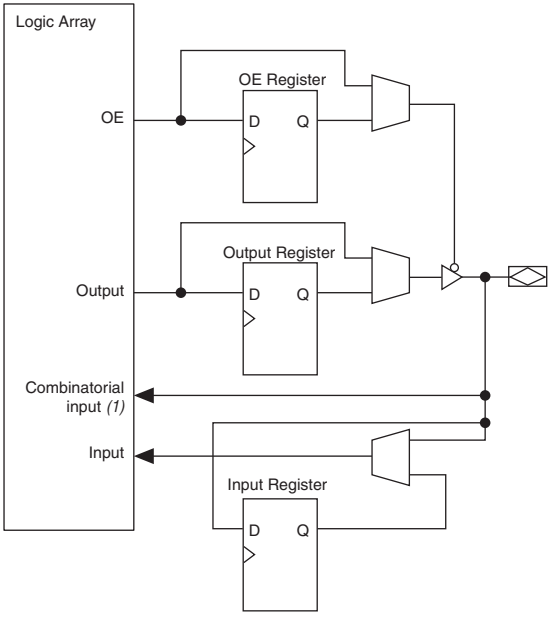
I/O Structure

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

Cyclone device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–27 shows the Cyclone IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. IOEs can be used as input, output, or bidirectional pins.

Figure 2–27. Cyclone IOE Structure



Note to Figure 2–27:

(1) There are two paths available for combinatorial inputs to the logic array. Each path contains a unique programmable delay chain.

The IOEs are located in I/O blocks around the periphery of the Cyclone device. There are up to three IOEs per row I/O block and up to three IOEs per column I/O block (column I/O blocks span two columns). The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–28 shows how a row I/O block connects to the logic array. Figure 2–29 shows how a column I/O block connects to the logic array.

3. Configuration and Testing

C51003-1.4

IEEE Std. 1149.1 (JTAG) Boundary Scan Support

All Cyclone® devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Cyclone devices can also use the JTAG port for configuration together with either the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Cyclone devices support reconfiguring the I/O standard settings on the IOE through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode. Designers can use this ability for JTAG testing before configuration when some of the Cyclone pins drive or receive from other devices on the board using voltage-referenced standards. Since the Cyclone device might not be configured before JTAG testing, the I/O pins might not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows designers to fully test I/O connection to other devices.

The JTAG pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The TDO pin voltage is determined by the V_{CCIO} of the bank where it resides. The bank V_{CCIO} selects whether the JTAG inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Cyclone devices also use the JTAG port to monitor the operation of the device with the SignalTap® II embedded logic analyzer. Cyclone devices support the JTAG instructions shown in Table 3–1.

Table 3–1. Cyclone JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 0000	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
		For extended-temperature use	–40	125	° C

Table 4–3. Cyclone Device DC Operating Conditions *Note (6)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10	—	10	µA
I_{CC0}	V_{CC} supply current (standby) (All M4K blocks in power-down mode) *(7)*	EP1C3	—	4	—	mA
		EP1C4	—	6	—	mA
		EP1C6	—	6	—	mA
		EP1C12	—	8	—	mA
		EP1C20	—	12	—	mA
R_{CONF} *(9)*	Value of I/O pin pull-up resistor before and during configuration	$V_I = 0$ V; $V_{CCI0} = 3.3$ V	15	25	50	kΩ
		$V_I = 0$ V; $V_{CCI0} = 2.5$ V	20	45	70	kΩ
		$V_I = 0$ V; $V_{CCI0} = 1.8$ V	30	65	100	kΩ
		$V_I = 0$ V; $V_{CCI0} = 1.5$ V	50	100	150	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	1	2	kΩ

Table 4–4. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	$I_{OH} = –4$ to –24 mA *(11)*	2.4	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ to 24 mA *(11)*	—	0.45	V

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA	—	0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1	—	V
		I_{OH} = –1 mA	2.0	—	V
		I_{OH} = –2 to –16 mA *(11)*	1.7	—	V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	—	0.2	V
		I_{OH} = 1 mA	—	0.4	V
		I_{OH} = 2 to 16 mA *(11)*	—	0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.65	1.95	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(12)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(11)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(11)*	—	0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.4	1.6	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3 *(12)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(11)*	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(11)*	—	0.25 × V_{CCIO}	V

Table 4–9. 2.5-V LVDS I/O Specifications *Note (13)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.5	2.625	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250	—	550	mV
Δ V_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω	—	—	50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
Δ V_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω	—	—	50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100	—	100	mV
V_{IN}	Receiver input voltage range	—	0.0	—	2.4	V
R_L	Receiver differential input resistor	—	90	100	110	Ω

Table 4–10. 3.3-V PCI Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.5	—	0.3 × V_{CCIO}	V

Power Consumption

Designers can use the Altera web Early Power Estimator to estimate the device power.

Cyclone devices require a certain amount of power-up current to successfully power up because of the nature of the leading-edge process on which they are fabricated. Table 4–17 shows the maximum power-up current required to power up a Cyclone device.

Table 4–17. Cyclone Maximum Power-Up Current (I_{CCINT}) Requirements (In-Rush Current)

Device	Commercial Specification	Industrial Specification	Unit
EP1C3	150	180	mA
EP1C4	150	180	mA
EP1C6	175	210	mA
EP1C12	300	360	mA
EP1C20	500	600	mA

Notes to Table 4–17:

(1) The Cyclone devices (except for the EP1C20 device) meet the power up specification for Mini PCI.

(2) The lot codes 9G0082 to 9G2999, or 9G3109 and later comply to the specifications in Table 4–17 and meet the Mini PCI specification. Lot codes appear at the top of the device.

(3) The lot codes 9H0004 to 9H29999, or 9H3014 and later comply to the specifications in this table and meet the Mini PCI specification. Lot codes appear at the top of the device.

Designers should select power supplies and regulators that can supply this amount of current when designing with Cyclone devices. This specification is for commercial operating conditions. Measurements were performed with an isolated Cyclone device on the board. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$$I = C\ (dV/dt)$$

The exact amount of current that is consumed varies according to the process, temperature, and power ramp rate. If the power supply or regulator can supply more current than required, the Cyclone device may consume more current than the maximum current specified in Table 4–17. However, the device does not require any more current to successfully power up than what is listed in Table 4–17.

The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time. The power-up current consumption drops when the V_{CCINT} supply reaches approximately 0.75 V. For example, if the V_{CCINT} rise time has a linear rise of 15 ms, the current consumption spike drops by 7.5 ms.

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–25 through 4–28 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–25. LE Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	29	—	33	—	37	—	ps
t_{H}	12	—	13	—	15	—	ps
t_{CO}	—	173	—	198	—	224	ps
t_{LUT}	—	454	—	522	—	590	ps
t_{CLR}	129	—	148	—	167	—	ps
t_{PRE}	129	—	148	—	167	—	ps
t_{CLKHL}	1,234	—	1,562	—	1,818	—	ps

Table 4–26. IOE Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	348	—	400	—	452	—	ps
t_{H}	0	—	0	—	0	—	ps
t_{CO}	—	511	—	587	—	664	ps
$t_{PIN2COMBOUT\_R}$	—	1,130	—	1,299	—	1,469	ps
$t_{PIN2COMBOUT\_C}$	—	1,135	—	1,305	—	1,475	ps
$t_{COMBIN2PIN\_R}$	—	2,627	—	3,021	—	3,415	ps
$t_{COMBIN2PIN\_C}$	—	2,615	—	3,007	—	3,399	ps
t_{CLR}	280	—	322	—	364	—	ps
t_{PRE}	280	—	322	—	364	—	ps
t_{CLKHL}	1,234	—	1,562	—	1,818	—	ps

July 2003 v1.1	Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—