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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	4000
Total RAM Bits	78336
Number of I/O	249
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c4f324c7

Introduction

The Cyclone® field programmable gate array family is based on a 1.5-V, 0.13-μm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 Kbits of RAM. With features like phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements, Cyclone devices are a cost-effective solution for data-path applications. Cyclone devices support various I/O standards, including LVDS at data rates up to 640 megabits per second (Mbps), and 66- and 33-MHz, 64- and 32-bit peripheral component interconnect (PCI), for interfacing with and supporting ASSP and ASIC devices. Altera also offers new low-cost serial configuration devices to configure Cyclone devices.

Features

The Cyclone device family offers the following features:

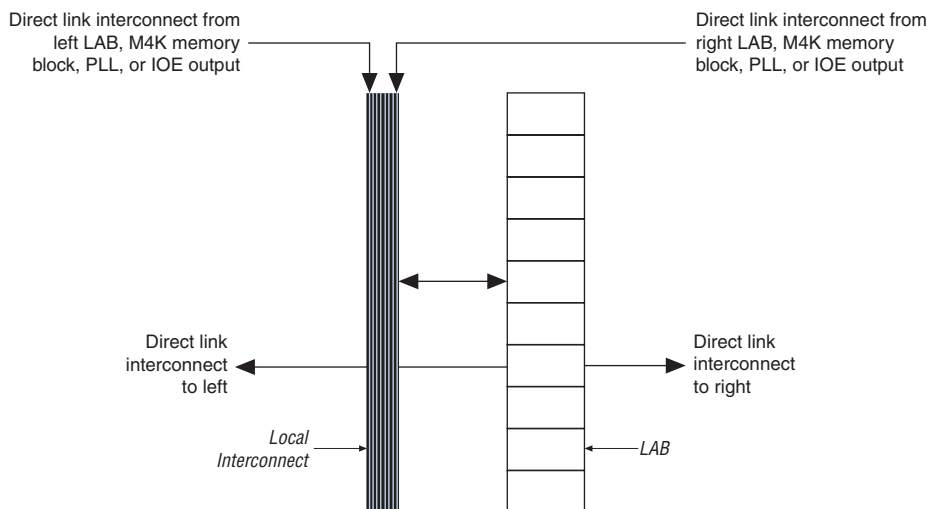
- 2,910 to 20,060 LEs, see [Table 1–1](#)
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66- and 33-MHz, 64- and 32-bit PCI standard
- High-speed (640 Mbps) LVDS I/O support
- Low-speed (311 Mbps) LVDS I/O support
- 311-Mbps RSDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz), FCRAM, and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) cores, including Altera® MegaCore® functions and Altera Megafunctions Partners Program (AMPPSM) megafunctions.

Table 1–1. Cyclone Device Features (Part 1 of 2)

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
LEs	2,910	4,000	5,980	12,060	20,060
M4K RAM blocks (128 × 36 bits)	13	17	20	52	64

performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

Figure 2–3. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

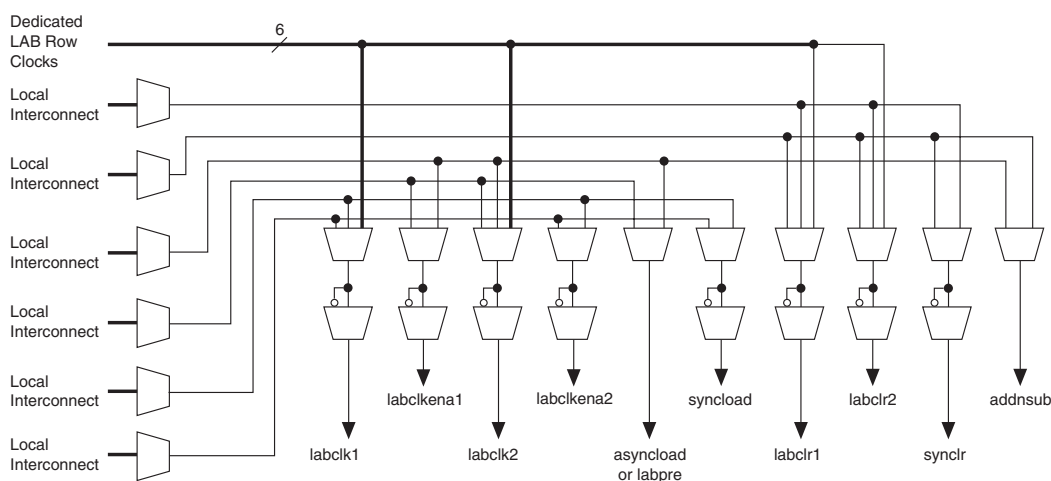
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labckena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. [Figure 2-4](#) shows the LAB control signal generation circuit.

Figure 2-4. LAB-Wide Control Signals

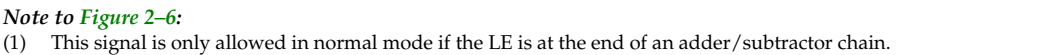


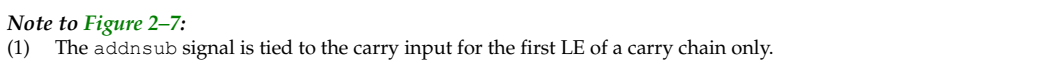
Logic Elements

The smallest unit of logic in the Cyclone architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by a LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See [Figure 2-5](#).

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see [Figure 2-6](#)). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.





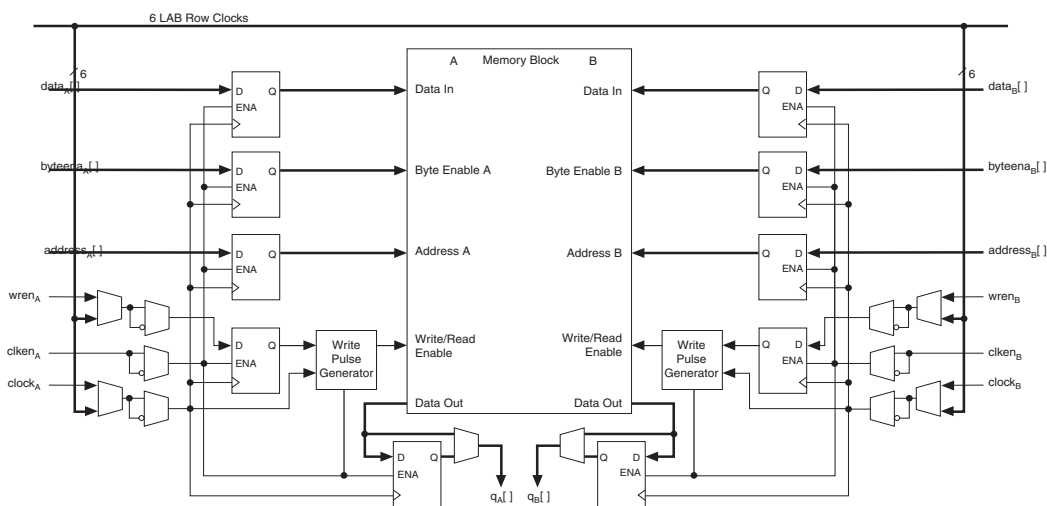
The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within a LAB.

Altera Corporation
May 2008

Independent Clock Mode

The M4K memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–17 shows an M4K memory block in independent clock mode.

Figure 2–17. Independent Clock Mode Notes (1), (2)



Notes to Figure 2–17:

- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, wren, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–18 and 2–19 show the memory block in input/output clock mode.

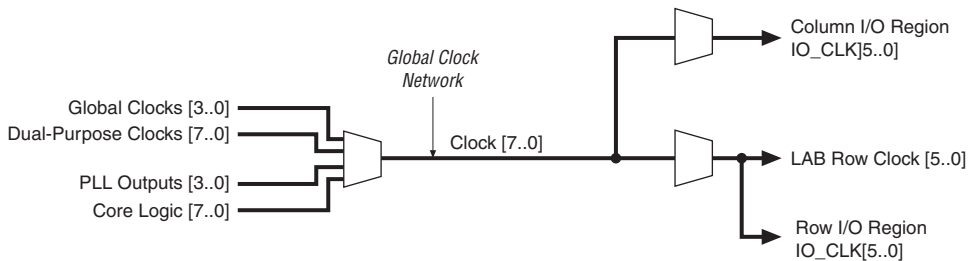
Dual-Purpose Clock Pins

Each Cyclone device except the EP1C3 device has eight dual-purpose clock pins, $DPCLK[7..0]$ (two on each I/O bank). EP1C3 devices have five $DPCLK$ pins in the 100-pin TQFP package. These dual-purpose pins can connect to the global clock network (see Figure 2–22) for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables, or protocol control signals such as $TRDY$ and $IRDY$ for PCI, or DQS signals for external memory interfaces.

Combined Resources

Each Cyclone device contains eight distinct dedicated clocking resources. The device uses multiplexers with these clocks to form six-bit buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. See Figure 2–23. Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

Figure 2–23. Global Clock Network Multiplexers



IOE clocks have row and column block regions. Six of the eight global clock resources feed to these row and column regions. Figure 2–24 shows the I/O clock regions.

External Clock Inputs

Each PLL supports single-ended or differential inputs for source-synchronous receivers or for general-purpose use. The dedicated clock pins (CLK[3..0]) feed the PLL inputs. These dual-purpose pins can also act as LVDS input pins. See [Figure 2-25](#).

[Table 2-8](#) shows the I/O standards supported by PLL input and output pins.

Table 2-8. PLL I/O Standards		
I/O Standard	CLK Input	EXTCLK Output
3.3-V LVTTL/LVCMOS	✓	✓
2.5-V LVTTL/LVCMOS	✓	✓
1.8-V LVTTL/LVCMOS	✓	✓
1.5-V LVCMOS	✓	✓
3.3-V PCI	✓	✓
LVDS	✓	✓
SSTL-2 class I	✓	✓
SSTL-2 class II	✓	✓
SSTL-3 class I	✓	✓
SSTL-3 class II	✓	✓
Differential SSTL-2	—	✓

For more information on LVDS I/O support, refer to “[LVDS I/O Pins](#)” on [page 2-54](#).

External Clock Outputs

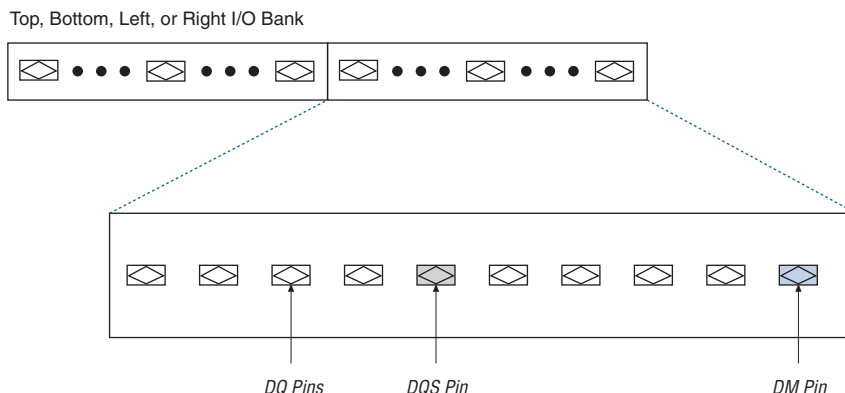
Each PLL supports one differential or one single-ended output for source-synchronous transmitters or for general-purpose external clocks. If the PLL does not use these PLL_OUT pins, the pins are available for use as general-purpose I/O pins. The PLL_OUT pins support all I/O standards shown in [Table 2-8](#).

The external clock outputs do not have their own V_{CC} and ground voltage supplies. Therefore, to minimize jitter, do not place switching I/O pins next to these output pins. The EP1C3 device in the 100-pin TQFP package

output pins (`nSTATUS` and `CONF_DONE`) and all the JTAG pins in I/O bank 3 must operate at 2.5 V because the V_{CCIO} level of SSTL-2 is 2.5 V. I/O banks 1, 2, 3, and 4 support DQS signals with DQ bus modes of $\times 8$.

For $\times 8$ mode, there are up to eight groups of programmable DQS and DQ pins, I/O banks 1, 2, 3, and 4 each have two groups in the 324-pin and 400-pin FineLine BGA packages. Each group consists of one DQS pin, a set of eight DQ pins, and one DM pin (see Figure 2–33). Each DQS pin drives the set of eight DQ pins within that group.

Figure 2–33. Cyclone Device DQ and DQS Groups in $\times 8$ Mode *Note (1)*



Note to Figure 2–33:

- (1) Each DQ group consists of one DQS pin, eight DQ pins, and one DM pin.

Table 2–10 shows the number of DQ pin groups per device.

Table 2–10. DQ Pin Groups (Part 1 of 2)			
Device	Package	Number of $\times 8$ DQ Pin Groups	Total DQ Pin Count
EP1C3	100-pin TQFP (1)	3	24
	144-pin TQFP	4	32
EP1C4	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 2–11 shows the possible settings for the I/O standards with drive strength control.

Table 2–11. Programmable Drive Strength <i>Note (1)</i>	
I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
LVTTL (3.3 V)	4
	8
	12
	16
	24(2)
LVCMOS (3.3 V)	2
	4
	8
	12(2)
LVTTL (2.5 V)	2
	8
	12
	16(2)
LVTTL (1.8 V)	2
	8
	12(2)
LVCMOS (1.5 V)	2
	4
	8(2)

Notes to Table 2–11:

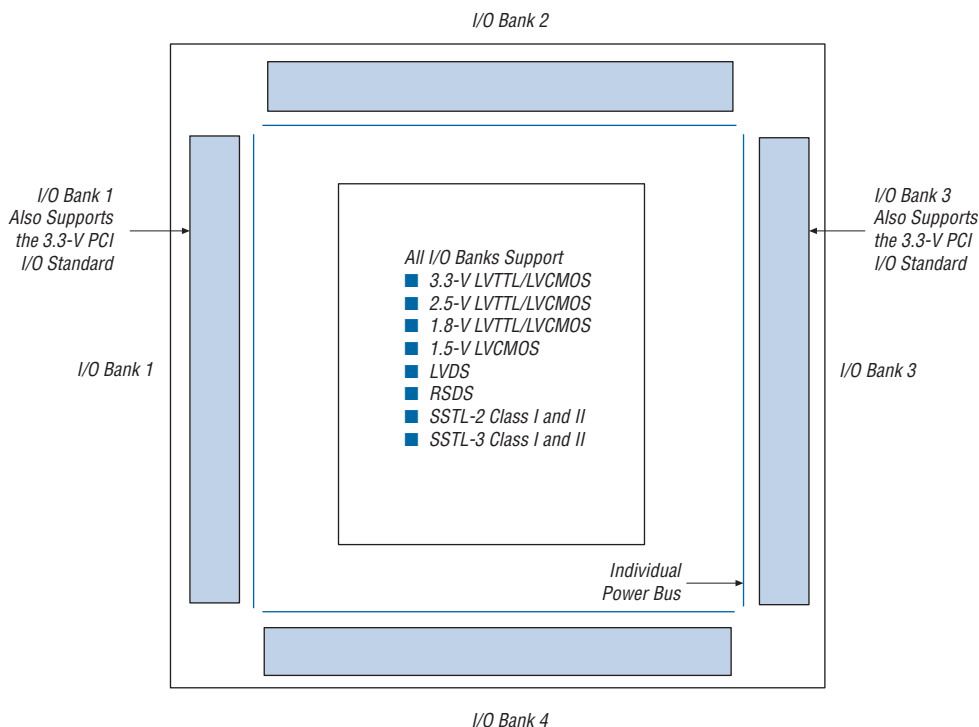
- (1) SSTL-3 class I and II, SSTL-2 class I and II, and 3.3-V PCI I/O Standards do not support programmable drive strength.
- (2) This is the default current strength setting in the Quartus II software.

Open-Drain Output

Cyclone devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

and DM pins to support a DDR SDRAM or FCRAM interface. I/O bank 1 can also support a DDR SDRAM or FCRAM interface, however, the configuration input pins in I/O bank 1 must operate at 2.5 V. I/O bank 3 can also support a DDR SDRAM or FCRAM interface, however, all the JTAG pins in I/O bank 3 must operate at 2.5 V.

Figure 2–35. Cyclone I/O Banks Notes (1), (2)



Notes to Figure 2–35:

- (1) Figure 2–35 is a top view of the silicon die.
- (2) Figure 2–35 is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has its own V_{CCIO} pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard with different I/O voltages. Each bank also has dual-purpose V_{REF} pins to support any one of the voltage-referenced standards (e.g., SSTL-3) independently. If an I/O bank does not use voltage-referenced standards, the V_{REF} pins are available as user I/O pins.

The Cyclone V_{CCINT} pins must always be connected to a 1.5-V power supply. If the V_{CCINT} level is 1.5 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The V_{CCIO} pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when V_{CCIO} pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V or 5.0-V systems. Table 2–14 summarizes Cyclone MultiVolt I/O support.

Table 2–14. Cyclone MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ (2)	✓ (2)	—	✓	—	—	—	—
1.8	✓	✓	✓ (2)	✓ (2)	—	✓ (3)	✓	—	—	—
2.5	—	—	✓	✓	—	✓ (5)	✓ (5)	✓	—	—
3.3	—	—	✓ (4)	✓	✓ (6)	✓ (7)	✓ (7)	✓ (7)	✓	✓ (8)

Notes to Table 2–14:

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO} .
- (2) When V_{CCIO} = 1.5-V or 1.8-V and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected. Turn on **Allow voltage overdrive for LVTTL / LVCMOS input pins** in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combinations.
- (3) When V_{CCIO} = 1.8-V, a Cyclone device can drive a 1.5-V device with 1.8-V tolerant inputs.
- (4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected.
- (5) When V_{CCIO} = 2.5-V, a Cyclone device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
- (6) Cyclone devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.
- (7) When V_{CCIO} = 3.3-V, a Cyclone device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
- (8) When V_{CCIO} = 3.3-V, a Cyclone device can drive a device with 5.0-V LVTTL inputs but not 5.0-V LVCMOS inputs.

Power Sequencing and Hot Socketing

Because Cyclone devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into Cyclone devices before and during power up without damaging the device. In addition, Cyclone devices do not drive out during power up. Once operating conditions are reached and the device is configured, Cyclone devices operate as specified by the user.



Cyclone devices must be within the first 8 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone devices are in the 9th or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.



For more information on JTAG, refer to the following documents:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

SignalTap II Embedded Logic Analyzer

Cyclone devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. A designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Cyclone architecture are configured with CMOS SRAM elements. Altera FPGAs are reconfigurable and every device is tested with a high coverage production test program so the designer does not have to perform fault testing and can instead focus on simulation and design verification.

Cyclone devices are configured at system power-up with data stored in an Altera configuration device or provided by a system controller. The Cyclone device's optimized interface allows the device to act as controller in an active serial configuration scheme with the new low-cost serial configuration device. Cyclone devices can be configured in under 120 ms using serial data at 20 MHz. The serial configuration device can be programmed via the ByteBlaster II download cable, the Altera Programming Unit (APU), or third-party programmers.

In addition to the new low-cost serial configuration device, Altera offers in-system programmability (ISP)-capable configuration devices that can configure Cyclone devices via a serial data stream. The interface also enables microprocessors to treat Cyclone devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy. After a Cyclone device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Operating Conditions

Cyclone® devices are offered in both commercial, industrial, and extended temperature grades. However, industrial-grade and extended-temperature-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Cyclone devices.

Table 4–1. Cyclone Device Absolute Maximum Ratings Notes (1), (2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCINT}	Supply voltage	With respect to ground (3)	–0.5	2.4	V
V _{CCIO}			–0.5	4.6	V
V _{CCA}	Supply voltage	With respect to ground (3)	–0.5	2.4	V
V _I	DC input voltage		–0.5	4.6	V
I _{OUT}	DC output current, per pin		–25	25	mA
T _{STG}	Storage temperature	No bias	–65	150	°C
T _{AMB}	Ambient temperature	Under bias	–65	135	°C
T _J	Junction temperature	BGA packages under bias	—	135	°C

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(4)	1.425	1.575	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4)	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	(4)	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	(4)	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	(4)	1.4	1.6	V
V _I	Input voltage	(3), (5)	–0.5	4.1	V

Power Consumption

Designers can use the Altera web Early Power Estimator to estimate the device power.

Cyclone devices require a certain amount of power-up current to successfully power up because of the nature of the leading-edge process on which they are fabricated. Table 4–17 shows the maximum power-up current required to power up a Cyclone device.

Table 4–17. Cyclone Maximum Power-Up Current (I_{CCINT}) Requirements (In-Rush Current)

Device	Commercial Specification	Industrial Specification	Unit
EP1C3	150	180	mA
EP1C4	150	180	mA
EP1C6	175	210	mA
EP1C12	300	360	mA
EP1C20	500	600	mA

Notes to Table 4–17:

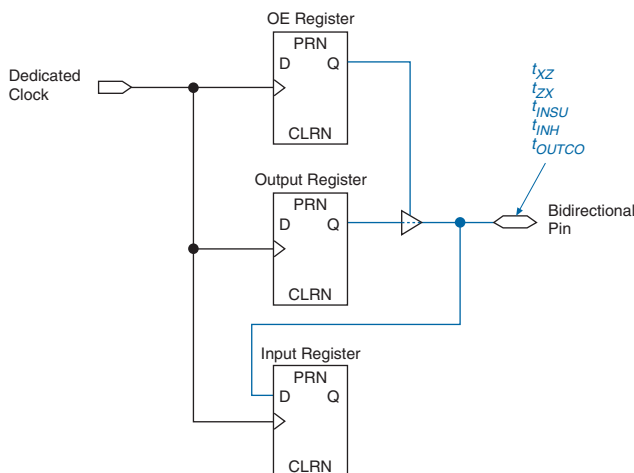
- (1) The Cyclone devices (except for the EP1C20 device) meet the power up specification for Mini PCI.
- (2) The lot codes 9G0082 to 9G2999, or 9G3109 and later comply to the specifications in Table 4–17 and meet the Mini PCI specification. Lot codes appear at the top of the device.
- (3) The lot codes 9H0004 to 9H2999, or 9H3014 and later comply to the specifications in this table and meet the Mini PCI specification. Lot codes appear at the top of the device.

Designers should select power supplies and regulators that can supply this amount of current when designing with Cyclone devices. This specification is for commercial operating conditions. Measurements were performed with an isolated Cyclone device on the board. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$$I = C (dV/dt)$$

The exact amount of current that is consumed varies according to the process, temperature, and power ramp rate. If the power supply or regulator can supply more current than required, the Cyclone device may consume more current than the maximum current specified in Table 4–17. However, the device does not require any more current to successfully power up than what is listed in Table 4–17.

The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time. The power-up current consumption drops when the V_{CCINT} supply reaches approximately 0.75 V. For example, if the V_{CCINT} rise time has a linear rise of 15 ms, the current consumption spike drops by 7.5 ms.

Figure 4–2. External Timing in Cyclone Devices

All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in [Tables 4–40 through 4–44](#).

[Table 4–29](#) shows the external I/O timing parameters when using global clock networks.

Table 4–29. Cyclone Global Clock External I/O Timing Parameters <i>Notes (1), (2) (Part 1 of 2)</i>		
Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	—
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	—
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by CLK pin	$C_{LOAD} = 10 \text{ pF}$
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting	—
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting	—

Tables 4–32 through 4–33 show the external timing parameters on column and row pins for EP1C4 devices.

Table 4–32. EP1C4 Column Pin Global Clock External I/O Timing Parameters *Note (1)*

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.471	—	2.841	—	3.210	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.937	2.000	4.526	2.000	5.119	ns
t_{INSUPLL}	1.471	—	1.690	—	1.910	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCOPLL}	0.500	2.080	0.500	2.392	0.500	2.705	ns

Table 4–33. EP1C4 Row Pin Global Clock External I/O Timing Parameters *Note (1)*

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.600	—	2.990	—	3.379	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.991	2.000	4.388	2.000	5.189	ns
t_{INSUPLL}	1.300	—	1.494	—	1.689	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCOPLL}	0.500	2.234	0.500	2.569	0.500	2.905	ns

Note to Tables 4–32 and 4–33:

(1) Contact Altera Applications for EP1C4 device timing parameters.

Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.8-V LVTTTL	2 mA	—	1,290	—	1,483	—	1,677	ps
	8 mA	—	4	—	4	—	5	ps
	12 mA	—	–208	—	–240	—	–271	ps
1.5-V LVTTTL	2 mA	—	2,288	—	2,631	—	2,974	ps
	4 mA	—	608	—	699	—	790	ps
	8 mA	—	292	—	335	—	379	ps
3.3-V PCI (1)		—	–877	—	–1,009	—	–1,141	ps
SSTL-3 class I		—	–410	—	–472	—	–533	ps
SSTL-3 class II		—	–811	—	–933	—	–1,055	ps
SSTL-2 class I		—	–485	—	–558	—	–631	ps
SSTL-2 class II		—	–758	—	–872	—	–986	ps
LVDS		—	–998	—	–1,148	—	–1,298	ps

Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	1,800	—	2,070	—	2,340	ps
	4 mA	—	1,311	—	1,507	—	1,704	ps
	8 mA	—	945	—	1,086	—	1,228	ps
	12 mA	—	807	—	928	—	1,049	ps
3.3-V LVTTTL	4 mA	—	1,831	—	2,105	—	2,380	ps
	8 mA	—	1,484	—	1,705	—	1,928	ps
	12 mA	—	973	—	1,118	—	1,264	ps
	16 mA	—	1,012	—	1,163	—	1,315	ps
	24 mA	—	838	—	963	—	1,089	ps
2.5-V LVTTTL	2 mA	—	2,747	—	3,158	—	3,570	ps
	8 mA	—	1,757	—	2,019	—	2,283	ps
	12 mA	—	1,763	—	2,026	—	2,291	ps
	16 mA	—	1,623	—	1,865	—	2,109	ps
1.8-V LVTTTL	2 mA	—	5,506	—	6,331	—	7,157	ps
	8 mA	—	4,220	—	4,852	—	5,485	ps
	12 mA	—	4,008	—	4,608	—	5,209	ps

Table 4–51. Cyclone Maximum Output Clock Rate for Row Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	296	285	273	MHz
2.5 V	381	366	349	MHz
1.8 V	286	277	267	MHz
1.5 V	219	208	195	MHz
LVC MOS	367	356	343	MHz
SSTL-3 class I	169	166	162	MHz
SSTL-3 class II	160	151	146	MHz
SSTL-2 class I	160	151	142	MHz
SSTL-2 class II	131	123	115	MHz
3.3-V PCI (1)	66	66	66	MHz
LVDS	320	303	275	MHz

Note to [Tables 4–50 through 4–51](#):

- (1) EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

PLL Timing

[Table 4–52](#) describes the Cyclone FPGA PLL specifications.

Table 4–52. Cyclone PLL Specifications (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{IN}	Input frequency (-6 speed grade)	15.625	464	MHz
	Input frequency (-7 speed grade)	15.625	428	MHz
	Input frequency (-8 speed grade)	15.625	387	MHz
f_{IN} DUTY	Input clock duty cycle	40.00	60	%
t_{IN} JITTER	Input clock period jitter	—	± 200	ps
f_{OUT_EXT} (external PLL clock output)	PLL output frequency (-6 speed grade)	15.625	320	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz

Referenced Document

This chapter references the following documents:

- *Cyclone Architecture* chapter in the *Cyclone Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*

Document Revision History

Table 4–53 shows the revision history for this chapter.

Table 4–53. Document Revision History		
Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.7	Minor textual and style changes. Added “Referenced Document” section.	—
January 2007 v1.6	<ul style="list-style-type: none"> Added document revision history. Added new row for V_{CCA} details in Table 4–1. Updated R_{CONF} information in Table 4–3. Added new <i>Note (12)</i> on voltage overdrive information to Table 4–7 and Table 4–8. Updated <i>Note (9)</i> on R_{CONF} information to Table 4–3. Updated information in “External I/O Delay Parameters” section. Updated speed grade information in Table 4–46 and Table 4–47. Updated LVDS information in Table 4–51. 	—
August 2005 v1.5	Minor updates.	—
February 2005 v1.4	<ul style="list-style-type: none"> Updated information on Undershoot voltage. Updated Table 4-2. Updated Table 4-3. Updated the undershoot voltage from 0.5 V to 2.0 V in Note 3 of Table 4-16. Updated Table 4-17. 	—
January 2004 v1.3	<ul style="list-style-type: none"> Added extended-temperature grade device information. Updated Table 4-2. Updated I_{CC0} information in Table 4-3. 	—
October 2003 v1.2	<ul style="list-style-type: none"> Added clock tree information in Table 4-19. Finalized timing information for EP1C3 and EP1C12 devices. Updated timing information in Tables 4-25 through 4-26 and Tables 4-30 through 4-51. Updated PLL specifications in Table 4-52. 	—