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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

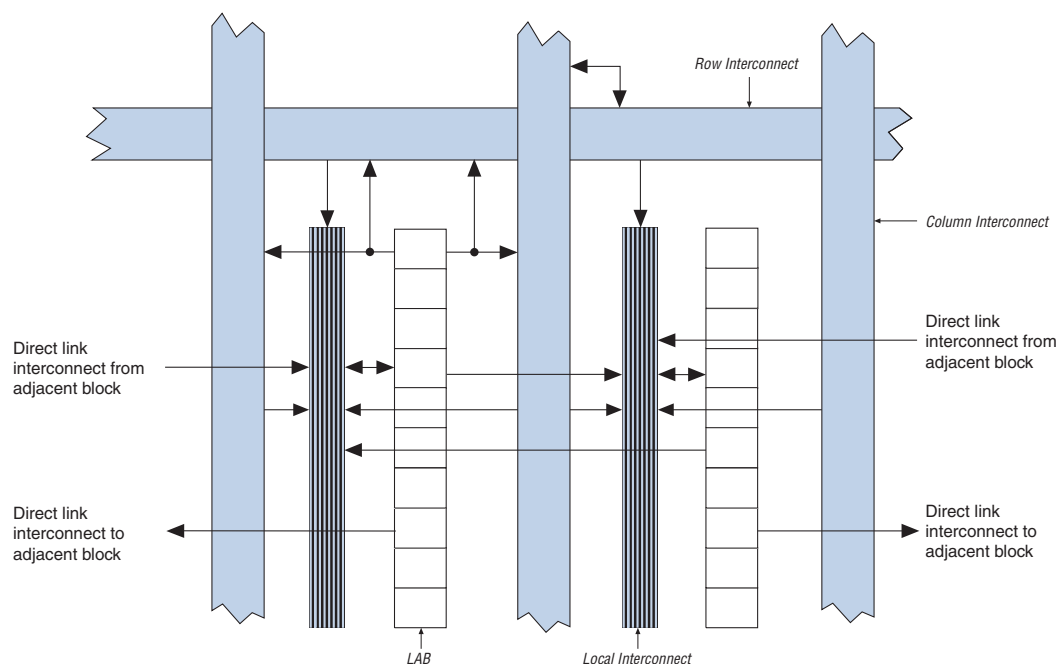
Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	4000
Total RAM Bits	78336
Number of I/O	249
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1c4f324c8">https://www.e-xfl.com/product-detail/intel/ep1c4f324c8</a>



## Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, look-up table (LUT) chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within a LAB. The Quartus® II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2-2 details the Cyclone LAB.

**Figure 2-2. Cyclone LAB Structure**



### LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, and M4K RAM blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher



The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to M4K memory blocks. A carry chain can continue as far as a full column.

### *Clear and Preset Logic Control*

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Cyclone devices support simultaneous preset/ asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Cyclone devices provide a chip-wide reset pin (DEV\_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

## **MultiTrack Interconnect**

In the Cyclone architecture, connections between LEs, M4K memory blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when



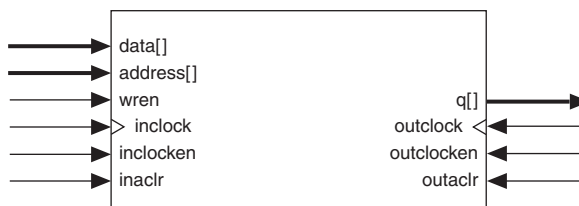
In addition to true dual-port memory, the M4K memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write. Single-port memory supports non-simultaneous reads and writes. Figure 2–13 shows these different M4K RAM memory port configurations.

**Figure 2–13. Simple Dual-Port and Single-Port Memory Configurations**

**Simple Dual-Port Memory**



**Single-Port Memory (1)**



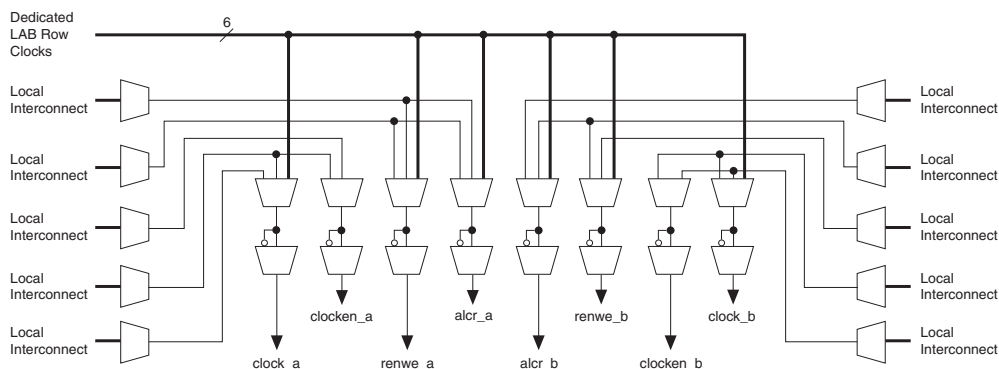
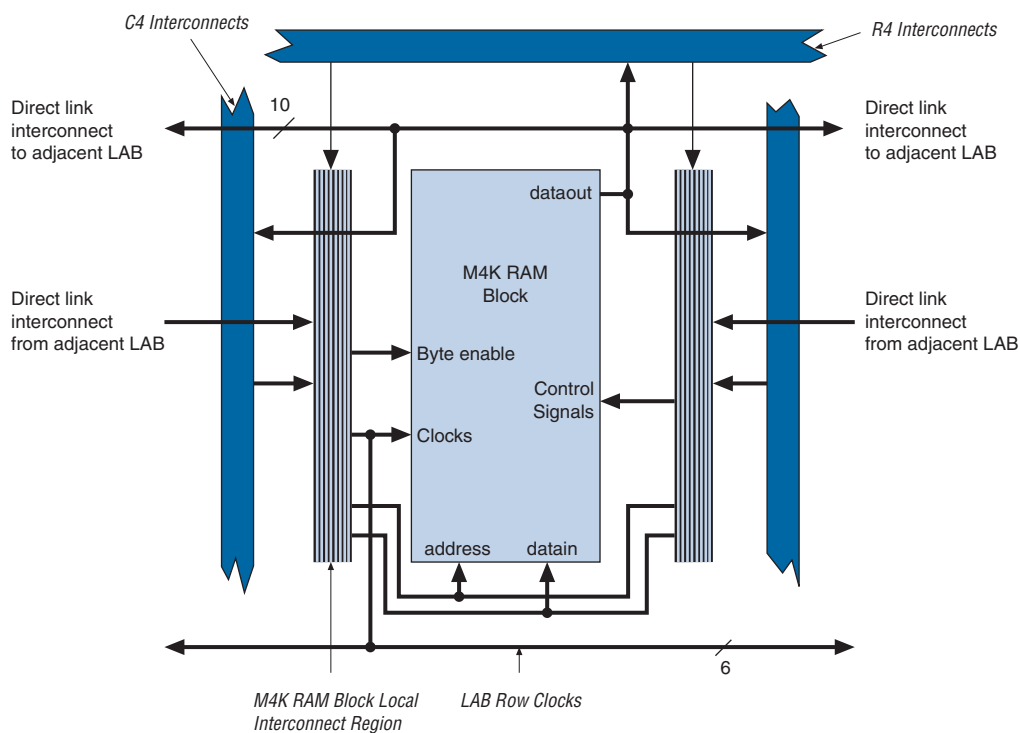
**Note to Figure 2–13:**

- (1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in  $\times 1$  mode at port A and read out in  $\times 16$  mode from port B.

The Cyclone memory architecture can implement fully synchronous RAM by registering both the input and output signals to the M4K RAM block. All M4K memory block inputs are registered, providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`wren`) signal derived from a global clock. In contrast, a circuit using asynchronous RAM must generate the RAM `wren` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `wren`



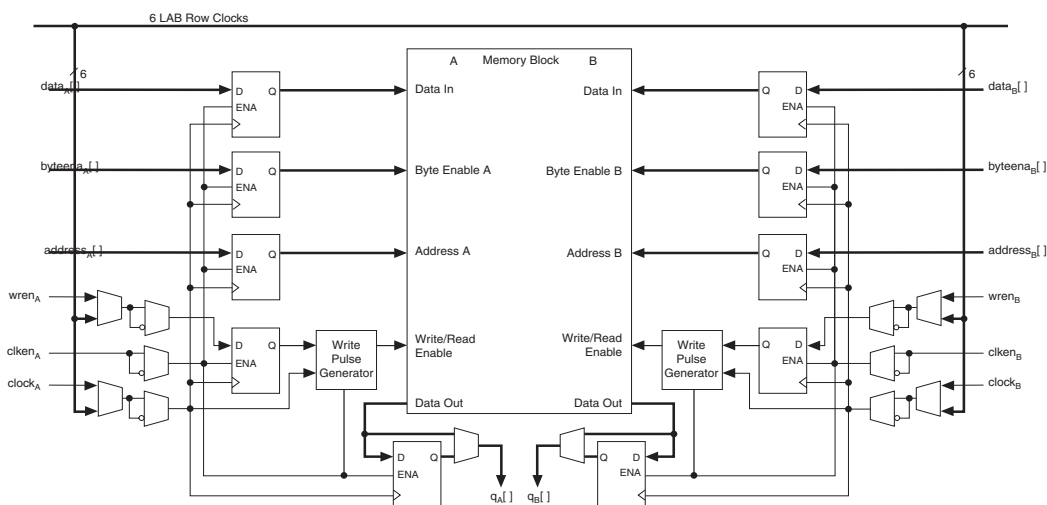
**Figure 2–15. M4K RAM Block Control Signals****Figure 2–16. M4K RAM Block LAB Row Interface**



## Independent Clock Mode

The M4K memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–17 shows an M4K memory block in independent clock mode.

**Figure 2–17. Independent Clock Mode** Notes (1), (2)



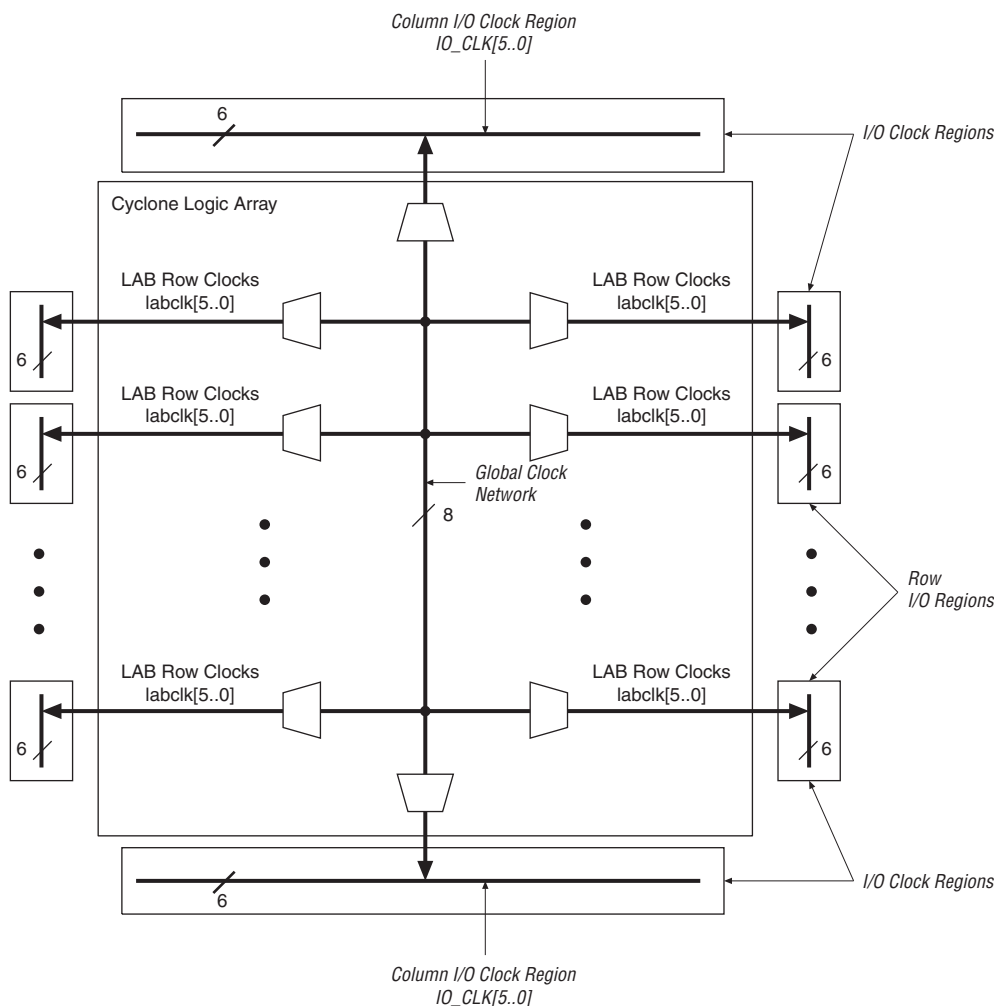
Notes to Figure 2–17:

- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

## Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, wren, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–18 and 2–19 show the memory block in input/output clock mode.



**Figure 2–24. I/O Clock Regions**

## PLLs

Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as outputs for differential I/O support. Cyclone devices contain two PLLs, except for the EP1C3 device, which contains one PLL.



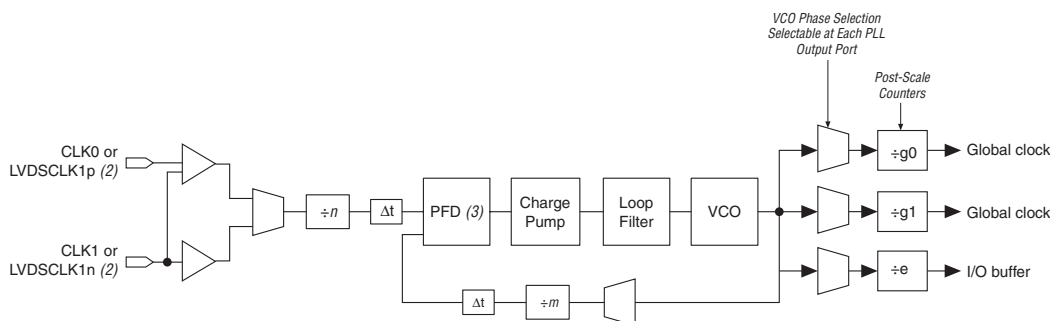
Table 2–6 shows the PLL features in Cyclone devices. Figure 2–25 shows a Cyclone PLL.

<b>Table 2–6. Cyclone PLL Features</b>	
<b>Feature</b>	<b>PLL Support</b>
Clock multiplication and division	$m/(n \times \text{post-scale counter})$ (1)
Phase shift	Down to 125-ps increments (2), (3)
Programmable duty cycle	Yes
Number of internal clock outputs	2
Number of external clock outputs	One differential or one single-ended (4)

**Notes to Table 2–6:**

- (1) The  $m$  counter ranges from 2 to 32. The  $n$  counter and the post-scale counters range from 1 to 32.
- (2) The smallest phase shift is determined by the voltage-controlled oscillator (VCO) period divided by 8.
- (3) For degree increments, Cyclone devices can shift all output frequencies in increments of 45°. Smaller degree increments are possible depending on the frequency and divide parameters.
- (4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

**Figure 2–25. Cyclone PLL**      *Note (1)*



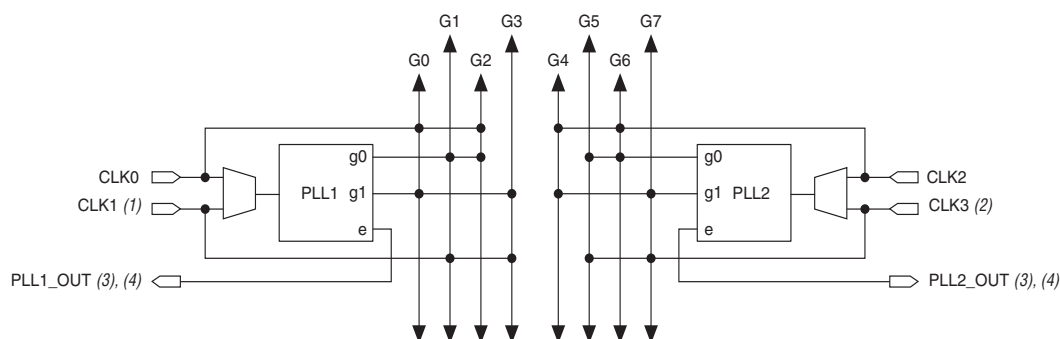
**Notes to Figure 2–25:**

- (1) The EP1C3 device in the 100-pin TQFP package does not support external outputs or LVDS inputs. The EP1C6 device in the 144-pin TQFP package does not support external output from PLL2.
- (2) LVDS input is supported via the secondary function of the dedicated clock pins. For PLL 1, the CLK0 pin's secondary function is LVDSCLK1p and the CLK1 pin's secondary function is LVDSCLK1n. For PLL 2, the CLK2 pin's secondary function is LVDSCLK2p and the CLK3 pin's secondary function is LVDSCLK2n.
- (3) PFD: phase frequency detector.



Figure 2–26 shows the PLL global clock connections.

**Figure 2–26. Cyclone PLL Global Clock Connections**



**Notes to Figure 2–26:**

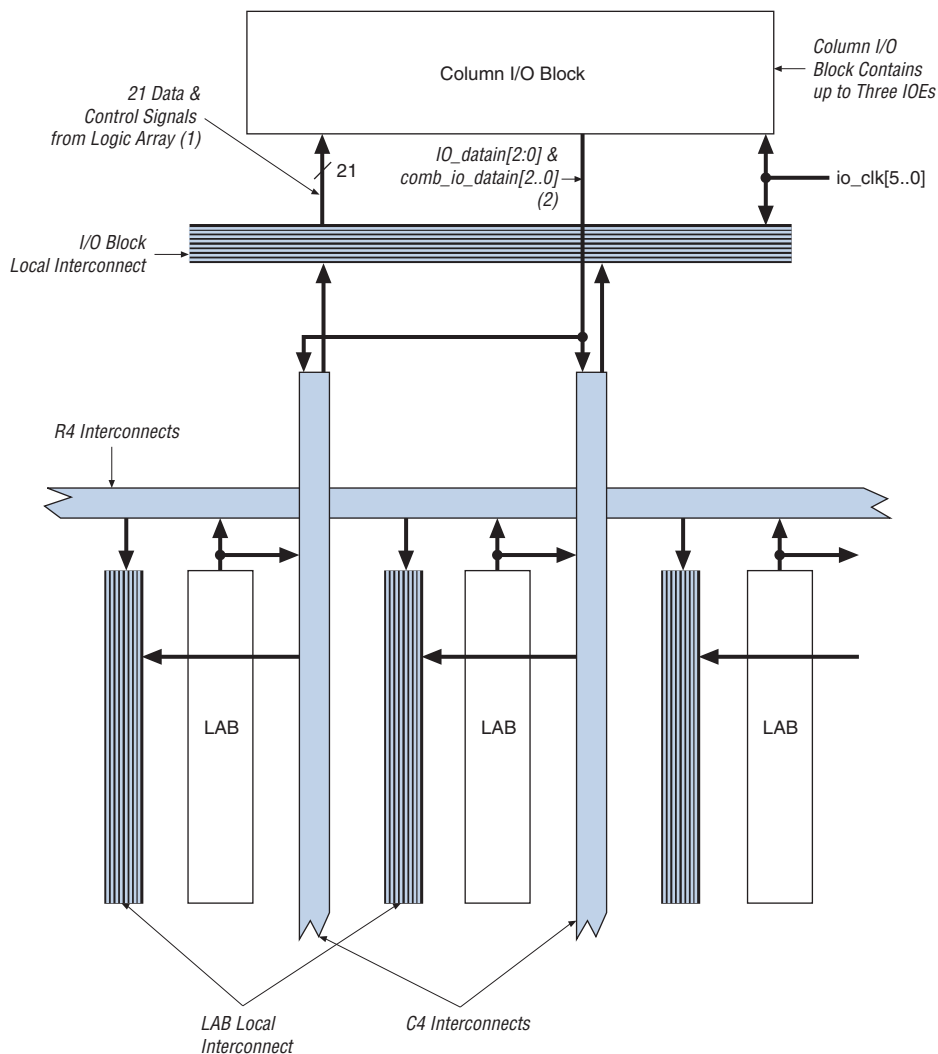
- (1) PLL 1 supports one single-ended or LVDS input via pins CLK0 and CLK1.
- (2) PLL2 supports one single-ended or LVDS input via pins CLK2 and CLK3.
- (3) PLL1\_OUT and PLL2\_OUT support single-ended or LVDS output. If external output is not required, these pins are available as regular user I/O pins.
- (4) The EP1C3 device in the 100-pin TQFP package does not support external clock output. The EP1C6 device in the 144-pin TQFP package does not support external clock output from PLL2.

Table 2–7 shows the global clock network sources available in Cyclone devices.

**Table 2–7. Global Clock Network Sources (Part 1 of 2)**

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
PLL Counter Output	PLL1 G0	—	✓	✓	—	—	—	—	—
	PLL1 G1	✓	—	—	✓	—	—	—	—
	PLL2 G0 (1)	—	—	—	—	—	✓	✓	—
	PLL2 G1 (1)	—	—	—	—	✓	—	—	✓
Dedicated Clock Input Pins	CLK0	✓	—	✓	—	—	—	—	—
	CLK1 (2)	—	✓	—	✓	—	—	—	—
	CLK2	—	—	—	—	✓	—	✓	—
	CLK3 (2)	—	—	—	—	—	✓	—	✓



**Figure 2–29. Column I/O Block Connection to the Interconnect****Notes to Figure 2–29:**

- (1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.
- (2) Each of the three IOEs in the column I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.



to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Table 2–9 shows the programmable delays for Cyclone devices.

<b>Table 2–9. Cyclone Programmable Delay Chain</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to logic array delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Output pin delay	Increase delay to output pin

There are two paths in the IOE for a combinatorial input to reach the logic array. Each of the two paths can have a different delay. This allows you adjust delays from the pin to internal LE registers that reside in two different areas of the device. The designer sets the two combinatorial input delays by selecting different delays for two different paths under the **Decrease input delay to internal cells** logic option in the Quartus II software. When the input signal requires two different delays for the combinatorial input, the input register in the IOE is no longer available.

The IOE registers in Cyclone devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

## External RAM Interfacing

Cyclone devices support DDR SDRAM and FCRAM interfaces at up to 133 MHz through dedicated circuitry.

## DDR SDRAM and FCRAM

Cyclone devices have dedicated circuitry for interfacing with DDR SDRAM. All I/O banks support DDR SDRAM and FCRAM I/O pins. However, the configuration input pins in bank 1 must operate at 2.5 V because the SSTL-2  $V_{CCIO}$  level is 2.5 V. Additionally, the configuration



<b>Table 2–10. DQ Pin Groups (Part 2 of 2)</b>			
<b>Device</b>	<b>Package</b>	<b>Number of × 8 DQ Pin Groups</b>	<b>Total DQ Pin Count</b>
EP1C6	144-pin TQFP	4	32
	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
EP1C12	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
	324-pin FineLine BGA	8	64
EP1C20	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

**Note to Table 2–10:**

- (1) EP1C3 devices in the 100-pin TQFP package do not have any DQ pin groups in I/O bank 1.

A programmable delay chain on each DQS pin allows for either a 90° phase shift (for DDR SDRAM), or a 72° phase shift (for FCRAM) which automatically center-aligns input DQS synchronization signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal clocks DQ signals on internal LE registers.

These DQS delay elements combine with the PLL's clocking and phase shift ability to provide a complete hardware solution for interfacing to high-speed memory.

The clock phase shift allows the PLL to clock the DQ output enable and output paths. The designer should use the following guidelines to meet 133 MHz performance for DDR SDRAM and FCRAM interfaces:

- The DQS signal must be in the middle of the DQ group it clocks
- Resynchronize the incoming data to the logic array clock using successive LE registers or FIFO buffers
- LE registers must be placed in the LAB adjacent to the DQ I/O pin column it is fed by

Figure 2–34 illustrates DDR SDRAM and FCRAM interfacing from the I/O through the dedicated circuitry to the logic array.



The output buffer for each Cyclone device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTTL and LVCMOS standards have several levels of drive strength that the designer can control. STTL-3 class I and II, and STTL-2 class I and II support a minimum setting, the lowest drive strength that guarantees the  $I_{OH}/I_{OL}$



## Slew-Rate Control

The output buffer for each Cyclone device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

## Bus Hold

Each Cyclone device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than  $V_{CCIO}$  to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 k $\Omega$  to pull the signal level to the last-driven state. [Table 4-15 on page 4-6](#) gives the specific sustaining current for each  $V_{CCIO}$  voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

## Programmable Pull-Up Resistor

Each Cyclone device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor (typically 25 k $\Omega$ ) holds the output to the  $V_{CCIO}$  level of the output pin's bank. Dedicated clock pins do not have the optional programmable pull-up resistor.



## Referenced Documents

This chapter references the following document:

- *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*

## Document Revision History

Table 2–15 shows the revision history for this chapter.

<b>Table 2–15. Document Revision History</b>		
<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2008 v1.6	Minor textual and style changes. Added “ <a href="#">Referenced Documents</a> ” section.	—
January 2007 v1.5	<ul style="list-style-type: none"> <li>● Added document revision history.</li> <li>● Updated <a href="#">Figures 2–17, 2–18, 2–19, 2–20, 2–21, and 2–32</a>.</li> </ul>	—
August 2005 v1.4	Minor updates.	—
February 2005 v1.3	<ul style="list-style-type: none"> <li>● Updated JTAG chain limits. Added test vector information.</li> <li>● Corrected Figure 2-12.</li> <li>● Added a note to Tables 2-17 through 2-21 regarding violating the setup or hold time.</li> </ul>	—
October 2003 v1.2	<ul style="list-style-type: none"> <li>● Updated phase shift information.</li> <li>● Added 64-bit PCI support information.</li> </ul>	—
September 2003 v1.1	Updated LVDS data rates to 640 Mbps from 311 Mbps.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—



**Table 4–5. LVCMOS Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	3.0	3.6	V
$V_{IH}$	High-level input voltage	—	1.7	4.1	V
$V_{IL}$	Low-level input voltage	—	–0.5	0.7	V
$V_{OH}$	High-level output voltage	$V_{CCIO} = 3.0$ , $I_{OH} = -0.1$ mA	$V_{CCIO} - 0.2$	—	V
$V_{OL}$	Low-level output voltage	$V_{CCIO} = 3.0$ , $I_{OL} = 0.1$ mA	—	0.2	V

**Table 4–6. 2.5-V I/O Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	2.375	2.625	V
$V_{IH}$	High-level input voltage	—	1.7	4.1	V
$V_{IL}$	Low-level input voltage	—	–0.5	0.7	V
$V_{OH}$	High-level output voltage	$I_{OH} = -0.1$ mA	2.1	—	V
		$I_{OH} = -1$ mA	2.0	—	V
		$I_{OH} = -2$ to $-16$ mA (11)	1.7	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 0.1$ mA	—	0.2	V
		$I_{OH} = 1$ mA	—	0.4	V
		$I_{OH} = 2$ to $16$ mA (11)	—	0.7	V

**Table 4–7. 1.8-V I/O Specifications**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	1.65	1.95	V
$V_{IH}$	High-level input voltage	—	$0.65 \times V_{CCIO}$	2.25 (12)	V
$V_{IL}$	Low-level input voltage	—	–0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -2$ to $-8$ mA (11)	$V_{CCIO} - 0.45$	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2$ to $8$ mA (11)	—	0.45	V



**Table 4–10. 3.3-V PCI Specifications (Part 2 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{OH}$	High-level output voltage	$I_{OUT} = -500 \mu A$	$0.9 \times V_{CCIO}$	—	—	V
$V_{OL}$	Low-level output voltage	$I_{OUT} = 1,500 \mu A$	—	—	$0.1 \times V_{CCIO}$	V

**Table 4–11. SSTL-2 Class I Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	2.375	2.5	2.625	V
$V_{TT}$	Termination voltage	—	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
$V_{REF}$	Reference voltage	—	1.15	1.25	1.35	V
$V_{IH}$	High-level input voltage	—	$V_{REF} + 0.18$	—	3.0	V
$V_{IL}$	Low-level input voltage	—	–0.3	—	$V_{REF} - 0.18$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -8.1 \text{ mA}$ (11)	$V_{TT} + 0.57$	—	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 8.1 \text{ mA}$ (11)	—	—	$V_{TT} - 0.57$	V

**Table 4–12. SSTL-2 Class II Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	2.3	2.5	2.7	V
$V_{TT}$	Termination voltage	—	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
$V_{REF}$	Reference voltage	—	1.15	1.25	1.35	V
$V_{IH}$	High-level input voltage	—	$V_{REF} + 0.18$	—	$V_{CCIO} + 0.3$	V
$V_{IL}$	Low-level input voltage	—	–0.3	—	$V_{REF} - 0.18$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -16.4 \text{ mA}$ (11)	$V_{TT} + 0.76$	—	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 16.4 \text{ mA}$ (11)	—	—	$V_{TT} - 0.76$	V

**Table 4–13. SSTL-3 Class I Specifications (Part 1 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	3.0	3.3	3.6	V
$V_{TT}$	Termination voltage	—	$V_{REF} - 0.05$	$V_{REF}$	$V_{REF} + 0.05$	V



**Table 4–13. SSTL-3 Class I Specifications (Part 2 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{REF}$	Reference voltage	—	1.3	1.5	1.7	V
$V_{IH}$	High-level input voltage	—	$V_{REF} + 0.2$	—	$V_{CCIO} + 0.3$	V
$V_{IL}$	Low-level input voltage	—	–0.3	—	$V_{REF} - 0.2$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -8 \text{ mA}$ (11)	$V_{TT} + 0.6$	—	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ (11)	—	—	$V_{TT} - 0.6$	V

**Table 4–14. SSTL-3 Class II Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage	—	3.0	3.3	3.6	V
$V_{TT}$	Termination voltage	—	$V_{REF} - 0.05$	$V_{REF}$	$V_{REF} + 0.05$	V
$V_{REF}$	Reference voltage	—	1.3	1.5	1.7	V
$V_{IH}$	High-level input voltage	—	$V_{REF} + 0.2$	—	$V_{CCIO} + 0.3$	V
$V_{IL}$	Low-level input voltage	—	–0.3	—	$V_{REF} - 0.2$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -16 \text{ mA}$ (11)	$V_{TT} + 0.8$	—	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 16 \text{ mA}$ (11)	—	—	$V_{TT} - 0.8$	V

**Table 4–15. Bus Hold Parameters**

Parameter	Conditions	V <sub>CCIO</sub> Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	—	—	30	—	50	—	70	—	μA
High sustaining current	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	—	—	–30	—	–50	—	–70	—	μA
Low overdrive current	0 V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	—	—	200	—	300	—	500	μA
High overdrive current	0 V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	—	—	–200	—	–300	—	–500	μA



**Table 4–22. IOE Internal Timing Microparameter Descriptions**

Symbol	Parameter
$t_{SU}$	IOE input and output register setup time before clock
$t_H$	IOE input and output register hold time after clock
$t_{CO}$	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
$t_{CLR}$	Minimum clear pulse width
$t_{PRE}$	Minimum preset pulse width
$t_{CLKHL}$	Minimum clock high or low time

**Table 4–23. M4K Block Internal Timing Microparameter Descriptions**

Symbol	Parameter
$t_{M4KRC}$	Synchronous read cycle time
$t_{M4KWC}$	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
$t_{M4KBEH}$	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATAO1}$	Clock-to-output delay when using output registers
$t_{M4KDATAO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
$t_{M4KCLR}$	Minimum clear pulse width



**Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTTL	2 mA	—	329	—	378	—	427	ps
	8 mA	—	–661	—	–761	—	–860	ps
	12 mA	—	–655	—	–754	—	–852	ps
	16 mA	—	–795	—	–915	—	–1034	ps
1.8-V LVTTTL	2 mA	—	4	—	4	—	5	ps
	8 mA	—	–208	—	–240	—	–271	ps
	12 mA	—	–208	—	–240	—	–271	ps
1.5-V LVTTTL	2 mA	—	2,288	—	2,631	—	2,974	ps
	4 mA	—	608	—	699	—	790	ps
	8 mA	—	292	—	335	—	379	ps
SSTL-3 class I		—	–410	—	–472	—	–533	ps
SSTL-3 class II		—	–811	—	–933	—	–1,055	ps
SSTL-2 class I		—	–485	—	–558	—	–631	ps
SSTL-2 class II		—	–758	—	–872	—	–986	ps
LVDS		—	–998	—	–1,148	—	–1,298	ps

**Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)**

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	0	—	0	—	0	ps
	4 mA	—	–489	—	–563	—	–636	ps
	8 mA	—	–855	—	–984	—	–1,112	ps
	12 mA	—	–993	—	–1,142	—	–1,291	ps
3.3-V LVTTTL	4 mA	—	0	—	0	—	0	ps
	8 mA	—	–347	—	–400	—	–452	ps
	12 mA	—	–858	—	–987	—	–1,116	ps
	16 mA	—	–819	—	–942	—	–1,065	ps
	24 mA	—	–993	—	–1,142	—	–1,291	ps
2.5-V LVTTTL	2 mA	—	329	—	378	—	427	ps
	8 mA	—	–661	—	–761	—	–860	ps
	12 mA	—	–655	—	–754	—	–852	ps
	16 mA	—	–795	—	–915	—	–1,034	ps



## Referenced Document

This chapter references the following documents:

- *Cyclone Architecture* chapter in the *Cyclone Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*

## Document Revision History

Table 4–53 shows the revision history for this chapter.

<b>Table 4–53. Document Revision History</b>		
<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2008 v1.7	Minor textual and style changes. Added “Referenced Document” section.	—
January 2007 v1.6	<ul style="list-style-type: none"> <li>Added document revision history.</li> <li>Added new row for <math>V_{CCA}</math> details in Table 4–1.</li> <li>Updated <math>R_{CONF}</math> information in Table 4–3.</li> <li>Added new <i>Note (12)</i> on voltage overdrive information to Table 4–7 and Table 4–8.</li> <li>Updated <i>Note (9)</i> on <math>R_{CONF}</math> information to Table 4–3.</li> <li>Updated information in “External I/O Delay Parameters” section.</li> <li>Updated speed grade information in Table 4–46 and Table 4–47.</li> <li>Updated LVDS information in Table 4–51.</li> </ul>	—
August 2005 v1.5	Minor updates.	—
February 2005 v1.4	<ul style="list-style-type: none"> <li>Updated information on Undershoot voltage. Updated Table 4-2.</li> <li>Updated Table 4-3.</li> <li>Updated the undershoot voltage from 0.5 V to 2.0 V in Note 3 of Table 4-16.</li> <li>Updated Table 4-17.</li> </ul>	—
January 2004 v1.3	<ul style="list-style-type: none"> <li>Added extended-temperature grade device information. Updated Table 4-2.</li> <li>Updated <math>I_{CC0}</math> information in Table 4-3.</li> </ul>	—
October 2003 v1.2	<ul style="list-style-type: none"> <li>Added clock tree information in Table 4-19.</li> <li>Finalized timing information for EP1C3 and EP1C12 devices. Updated timing information in Tables 4-25 through 4-26 and Tables 4-30 through 4-51.</li> <li>Updated PLL specifications in Table 4-52.</li> </ul>	—