# Intel - EP1C4F400C7N Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

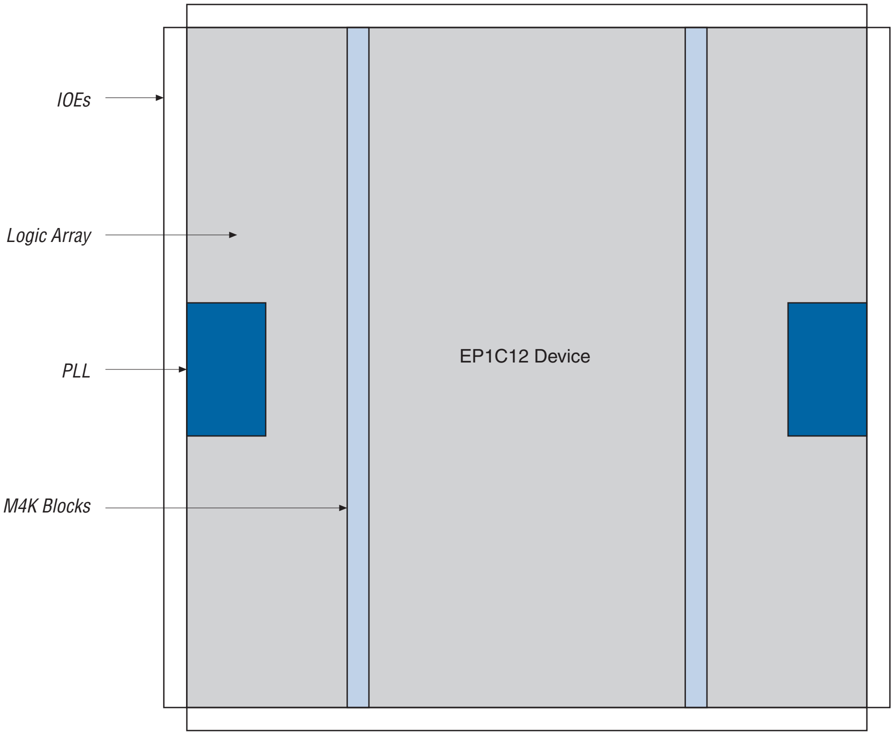
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 400 |
| Number of Logic Elements/Cells | 4000 |
| Total RAM Bits | 78336 |
| Number of I/O | 301 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 400-BGA |
| Supplier Device Package | 400-FBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1c4f400c7n |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

*Figure 2–1. Cyclone EP1C12 Device Block Diagram*



The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

*Table 2–1. Cyclone Device Resources*

| Device | M4K RAM | | PLLs | LAB Columns | LAB Rows |
|---|---|---|---|---|---|
| | Columns | Blocks | | | |
| EP1C3 | 1 | 13 | 1 | 24 | 13 |
| EP1C4 | 1 | 17 | 2 | 26 | 17 |
| EP1C6 | 1 | 20 | 2 | 32 | 20 |
| EP1C12 | 2 | 52 | 2 | 48 | 26 |
| EP1C20 | 2 | 64 | 2 | 64 | 32 |

### *Dynamic Arithmetic Mode*

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in Figure 2–7, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry-in0
```

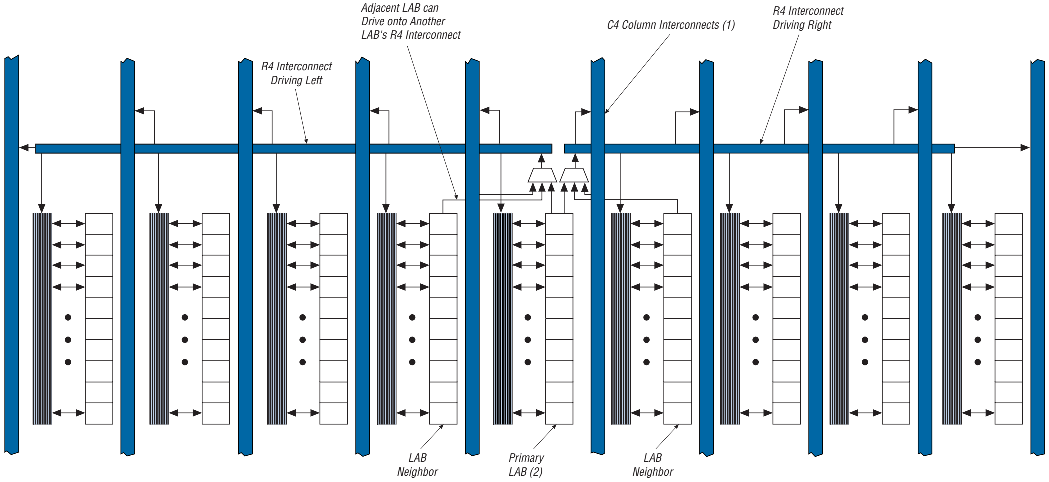
or

```
data1 + data2 + carry-in1
```

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

*Figure 2–9. R4 Interconnect Connections*



*Notes to Figure 2–9:*

(1) C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, M4K memory blocks, and row and column IOEs. These column resources include:

- LUT chain interconnects within a LAB
- Register chain interconnects within a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction

Cyclone devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

## Byte Enables

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2–5 summarizes the byte selection.

*Table 2–5. Byte Enable for M4K Blocks* *Notes (1), (2)*

| byteena[3..0] | datain ×18 | datain ×36 |
|---|---|---|
| [0] = 1 | [8..0] | [8..0] |
| [1] = 1 | [17..9] | [17..9] |
| [2] = 1 | — | [26..18] |
| [3] = 1 | — | [35..27] |

*Notes to Table 2–5:*

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

## Control Signals and M4K Interface

The M4K blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–15.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2–16 shows the M4K block to logic array interface.

*Figure 2–15. M4K RAM Block Control Signals*

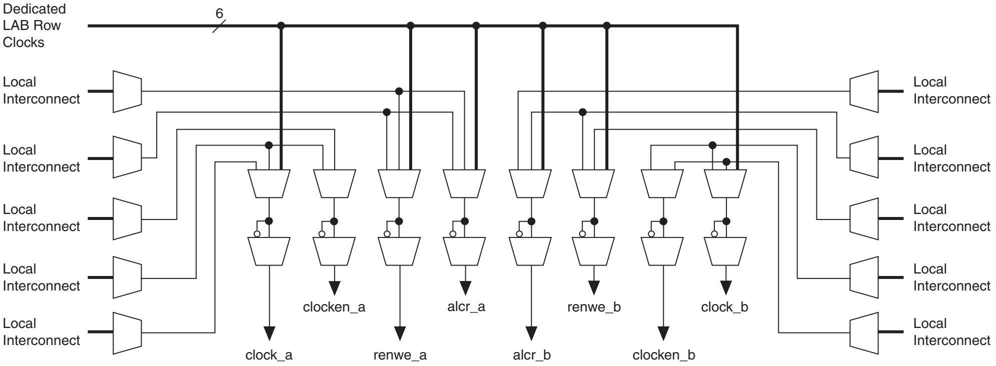
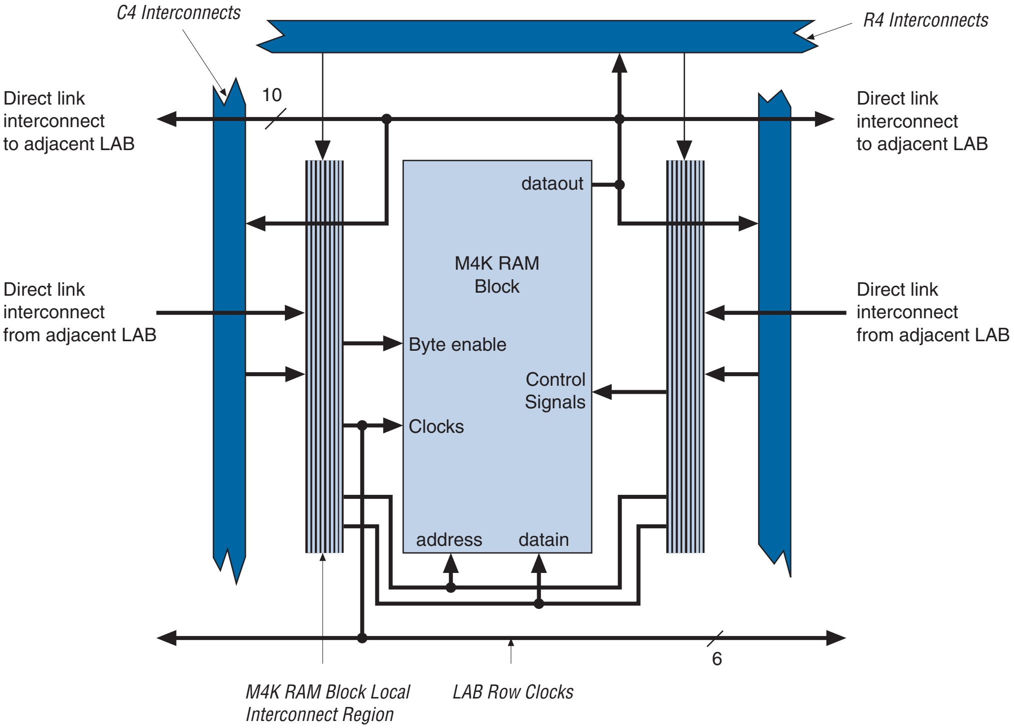


*Figure 2–16. M4K RAM Block LAB Row Interface*



## Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

## Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

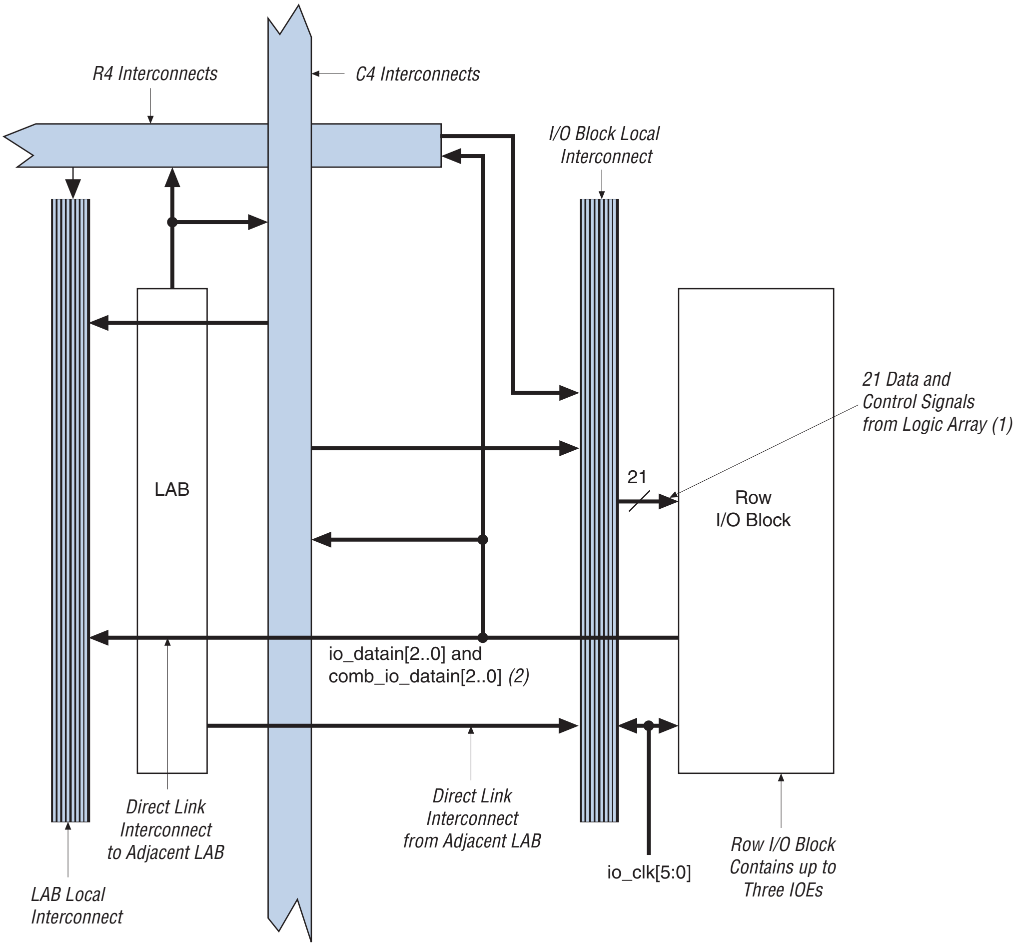
The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

*Figure 2–28. Row I/O Block Connection to the Interconnect*



*Notes to Figure 2–28:*

(1) The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.

(2) Each of the three IOEs in the row I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

Figure 3–1 shows the timing requirements for the JTAG signals.

*Figure 3–1. Cyclone JTAG Waveforms*

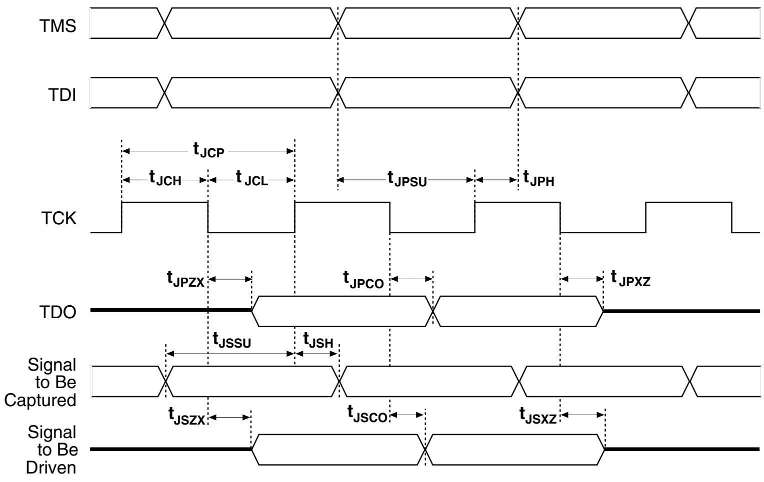


Table 3–4 shows the JTAG timing parameters and values for Cyclone devices.

*Table 3–4. Cyclone JTAG Timing Parameters and Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | `TCK` clock period | 100 | — | ns |
| $t_{JCH}$ | `TCK` clock high time | 50 | — | ns |
| $t_{JCL}$ | `TCK` clock low time | 50 | — | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | — | ns |
| $t_{JSH}$ | Capture register hold time | 45 | — | ns |
| $t_{JSCO}$ | Update register clock to output | — | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | — | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | — | 35 | ns |

## Operating Modes

The Cyclone architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Cyclone devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to $V_{CCIO}$ before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the $V_{CCIO}$ of the bank where the pins reside. The bank $V_{CCIO}$ selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

## Configuration Schemes

Designers can load the configuration data for a Cyclone device with one of three configuration schemes (see Table 3–5), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone device. A low-cost configuration device can automatically configure a Cyclone device at system power-up.

## Power Consumption

Designers can use the Altera web Early Power Estimator to estimate the device power.

Cyclone devices require a certain amount of power-up current to successfully power up because of the nature of the leading-edge process on which they are fabricated. Table 4–17 shows the maximum power-up current required to power up a Cyclone device.

*Table 4–17. Cyclone Maximum Power-Up Current ($I_{CCINT}$) Requirements (In-Rush Current)*

| Device | Commercial Specification | Industrial Specification | Unit |
|---|---|---|---|
| EP1C3 | 150 | 180 | mA |
| EP1C4 | 150 | 180 | mA |
| EP1C6 | 175 | 210 | mA |
| EP1C12 | 300 | 360 | mA |
| EP1C20 | 500 | 600 | mA |

*Notes to Table 4–17:*

(1) The Cyclone devices (except for the EP1C20 device) meet the power up specification for Mini PCI.

(2) The lot codes 9G0082 to 9G2999, or 9G3109 and later comply to the specifications in Table 4–17 and meet the Mini PCI specification. Lot codes appear at the top of the device.

(3) The lot codes 9H0004 to 9H29999, or 9H3014 and later comply to the specifications in this table and meet the Mini PCI specification. Lot codes appear at the top of the device.

Designers should select power supplies and regulators that can supply this amount of current when designing with Cyclone devices. This specification is for commercial operating conditions. Measurements were performed with an isolated Cyclone device on the board. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$$I = C\,(dV/dt)$$

The exact amount of current that is consumed varies according to the process, temperature, and power ramp rate. If the power supply or regulator can supply more current than required, the Cyclone device may consume more current than the maximum current specified in Table 4–17. However, the device does not require any more current to successfully power up than what is listed in Table 4–17.

The duration of the $I_{CCINT}$ power-up requirement depends on the $V_{CCINT}$ voltage supply rise time. The power-up current consumption drops when the $V_{CCINT}$ supply reaches approximately 0.75 V. For example, if the $V_{CCINT}$ rise time has a linear rise of 15 ms, the current consumption spike drops by 7.5 ms.

Typically, the user-mode current during device operation is lower than the power-up current in Table 4–17. Altera recommends using the Cyclone Power Calculator, available on the Altera web site, to estimate the user-mode $I_{CCINT}$ consumption and then select power supplies or regulators based on the higher value.

# Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

## Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–18 shows the status of the Cyclone device timing models.

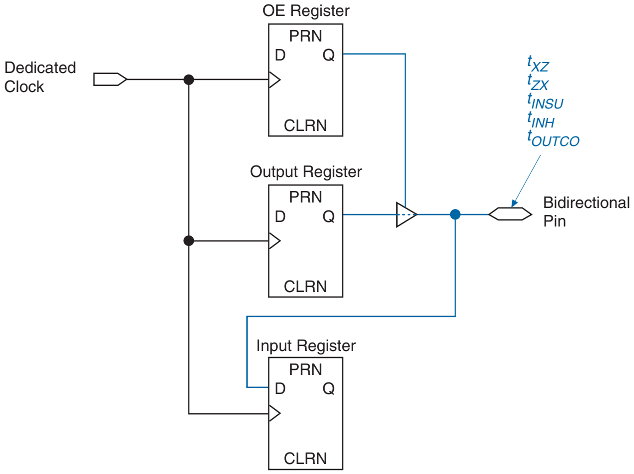
Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

*Table 4–18. Cyclone Device Timing Model Status*

| Device | Preliminary | Final |
|---|---|---|
| EP1C3 | — | ✓ |
| EP1C4 | — | ✓ |
| EP1C6 | — | ✓ |
| EP1C12 | — | ✓ |
| EP1C20 | — | ✓ |

*Figure 4–2. External Timing in Cyclone Devices*



All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–40 through 4–44.

Table 4–29 shows the external I/O timing parameters when using global clock networks.

***Table 4–29. Cyclone Global Clock External I/O Timing Parameters*** *Notes (1), (2)* ***(Part 1 of 2)***

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSU}$ | Setup time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin | — |
| $t_{INH}$ | Hold time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin | — |
| $t_{OUTCO}$ | Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{INSUPLL}$ | Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting | — |
| $t_{INHPLL}$ | Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting | — |

Tables 4–34 through 4–35 show the external timing parameters on column and row pins for EP1C6 devices.

*Table 4–34. EP1C6 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.691 | — | 3.094 | — | 3.496 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.917 | 2.000 | 4.503 | 2.000 | 5.093 | ns |
| $t_{INSUPLL}$ | 1.513 | — | 1.739 | — | 1.964 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.038 | 0.500 | 2.343 | 0.500 | 2.651 | ns |

*Table 4–35. EP1C6 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.774 | — | 3.190 | — | 3.605 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.817 | 2.000 | 4.388 | 2.000 | 4.963 | ns |
| $t_{INSUPLL}$ | 1.596 | — | 1.835 | — | 2.073 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 1.938 | 0.500 | 2.228 | 0.500 | 2.521 | ns |

Tables 4–36 through 4–37 show the external timing parameters on column and row pins for EP1C12 devices.

*Table 4–36. EP1C12 Column Pin Global Clock External I/O Timing Parameters (Part 1 of 2)*

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.510 | — | 2.885 | — | 3.259 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $tO_{UTCO}$ | 2.000 | 3.798 | 2.000 | 4.367 | 2.000 | 4.940 | ns |
| $t_{INSUPLL}$ | 1.588 | — | 1.824 | — | 2.061 | — | ns |

*Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 2 of 2)*

| I/O Standard | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| SSTL-2 class II | | –278 | — | –320 | — | –362 | ps |
| LVDS | | –261 | — | –301 | — | –340 | ps |

*Table 4–41. Cyclone I/O Standard Row Pin Input Delay Adders*

| I/O Standard | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| LVCMOS | — | 0 | — | 0 | — | 0 | ps |
| 3.3-V LVTTL | — | 0 | — | 0 | — | 0 | ps |
| 2.5-V LVTTL | — | 27 | — | 31 | — | 35 | ps |
| 1.8-V LVTTL | — | 182 | — | 209 | — | 236 | ps |
| 1.5-V LVTTL | — | 278 | — | 319 | — | 361 | ps |
| 3.3-V PCI *(1)* | — | 0 | — | 0 | — | 0 | ps |
| SSTL-3 class I | — | –250 | — | –288 | — | –325 | ps |
| SSTL-3 class II | — | –250 | — | –288 | — | –325 | ps |
| SSTL-2 class I | — | –278 | — | –320 | — | –362 | ps |
| SSTL-2 class II | — | –278 | — | –320 | — | –362 | ps |
| LVDS | — | –261 | — | –301 | — | –340 | ps |

*Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)*

| Standard | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | — | 0 | — | 0 | — | 0 | ps |
| | 4 mA | — | –489 | — | –563 | — | –636 | ps |
| | 8 mA | — | –855 | — | –984 | — | –1,112 | ps |
| | 12 mA | — | –993 | — | –1,142 | — | –1,291 | ps |
| 3.3-V LVTTL | 4 mA | — | 0 | — | 0 | — | 0 | ps |
| | 8 mA | — | –347 | — | –400 | — | –452 | ps |
| | 12 mA | — | –858 | — | –987 | — | –1,116 | ps |
| | 16 mA | — | –819 | — | –942 | — | –1,065 | ps |
| | 24 mA | — | –993 | — | –1,142 | — | –1,291 | ps |

*Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)*

| I/O Standard | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| 1.5-V LVTTL | 2 mA | — | 6,789 | — | 7,807 | — | 8,825 | ps |
| | 4 mA | — | 5,109 | — | 5,875 | — | 6,641 | ps |
| | 8 mA | — | 4,793 | — | 5,511 | — | 6,230 | ps |
| SSTL-3 class I | | — | 1,390 | — | 1,598 | — | 1,807 | ps |
| SSTL-3 class II | | — | 989 | — | 1,137 | — | 1,285 | ps |
| SSTL-2 class I | | — | 1,965 | — | 2,259 | — | 2,554 | ps |
| SSTL-2 class II | | — | 1,692 | — | 1,945 | — | 2,199 | ps |
| LVDS | | — | 802 | — | 922 | — | 1,042 | ps |

*Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 1 of 2)*

| I/O Standard | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | — | 1,800 | — | 2,070 | — | 2,340 | ps |
| | 4 mA | — | 1,311 | — | 1,507 | — | 1,704 | ps |
| | 8 mA | — | 945 | — | 1,086 | — | 1,228 | ps |
| | 12 mA | — | 807 | — | 928 | — | 1,049 | ps |
| 3.3-V LVTTL | 4 mA | — | 1,831 | — | 2,105 | — | 2,380 | ps |
| | 8 mA | — | 1,484 | — | 1,705 | — | 1,928 | ps |
| | 12 mA | — | 973 | — | 1,118 | — | 1,264 | ps |
| | 16 mA | — | 1,012 | — | 1,163 | — | 1,315 | ps |
| | 24 mA | — | 838 | — | 963 | — | 1,089 | ps |
| 2.5-V LVTTL | 2 mA | — | 2,747 | — | 3,158 | — | 3,570 | ps |
| | 8 mA | — | 1,757 | — | 2,019 | — | 2,283 | ps |
| | 12 mA | — | 1,763 | — | 2,026 | — | 2,291 | ps |
| | 16 mA | — | 1,623 | — | 1,865 | — | 2,109 | ps |
| 1.8-V LVTTL | 2 mA | — | 5,506 | — | 6,331 | — | 7,157 | ps |
| | 8 mA | — | 4,220 | — | 4,852 | — | 5,485 | ps |
| | 12 mA | — | 4,008 | — | 4,608 | — | 5,209 | ps |
| 1.5-V LVTTL | 2 mA | — | 6,789 | — | 7,807 | — | 8,825 | ps |
| | 4 mA | — | 5,109 | — | 5,875 | — | 6,641 | ps |
| | 8 mA | — | 4,793 | — | 5,511 | — | 6,230 | ps |
| 3.3-V PCI | | — | 923 | — | 1,061 | — | 1,199 | ps |

**Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)**

| I/O Standard | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| SSTL-3 class I | — | 1,390 | — | 1,598 | — | 1,807 | ps |
| SSTL-3 class II | — | 989 | — | 1,137 | — | 1,285 | ps |
| SSTL-2 class I | — | 1,965 | — | 2,259 | — | 2,554 | ps |
| SSTL-2 class II | — | 1,692 | — | 1,945 | — | 2,199 | ps |
| LVDS | — | 802 | — | 922 | — | 1,042 | ps |

*Note to Tables 4–40 through 4–45:*

(1) EP1C3 devices do not support the PCI I/O standard.

Tables 4–46 through 4–47 show the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

**Table 4–46. Cyclone IOE Programmable Delays on Column Pins**

| Parameter | Setting | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Decrease input delay to internal cells | Off | — | 155 | — | 178 | — | 201 | ps |
| | Small | — | 2,122 | — | 2,543 | — | 2,875 | ps |
| | Medium | — | 2,639 | — | 3,034 | — | 3,430 | ps |
| | Large | — | 3,057 | — | 3,515 | — | 3,974 | ps |
| | On | — | 155 | — | 178 | — | 201 | ps |
| Decrease input delay to input register | Off | — | 0 | — | 0 | — | 0 | ps |
| | On | — | 3,057 | — | 3,515 | — | 3,974 | ps |
| Increase delay to output pin | Off | — | 0 | — | 0 | — | 0 | ps |
| | On | — | 552 | — | 634 | — | 717 | ps |

## Referenced Document

This chapter references the following documents:

- *Cyclone Architecture* chapter in the *Cyclone Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*

## Document Revision History

Table 4–53 shows the revision history for this chapter.

*Table 4–53. Document Revision History*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| May 2008<br>v1.7 | Minor textual and style changes. Added "Referenced Document" section. | — |
| January 2007<br>v1.6 | Added document revision history.<br>Added new row for $V_{CCA}$ details in Table 4–1.<br>Updated $R_{CONF}$ information in Table 4–3.<br>Added new *Note (12)* on voltage overdrive information to Table 4–7 and Table 4–8.<br>Updated *Note (9)* on $R_{CONF}$ information to Table 4–3.<br>Updated information in "External I/O Delay Parameters" section.<br>Updated speed grade information in Table 4–46 and Table 4–47.<br>Updated LVDS information in Table 4–51. | — |
| August 2005<br>v1.5 | Minor updates. | — |
| February 2005<br>v1.4 | Updated information on Undershoot voltage. Updated Table 4-2.<br>Updated Table 4-3.<br>Updated the undershoot voltage from 0.5 V to 2.0 V in Note 3 of Table 4-16.<br>Updated Table 4-17. | — |
| January 2004<br>v.1.3 | Added extended-temperature grade device information. Updated Table 4-2.<br>Updated $I_{CC0}$ information in Table 4-3. | — |
| October 2003<br>v.1.2 | Added clock tree information in Table 4-19.<br>Finalized timing information for EP1C3 and EP1C12 devices. Updated timing information in Tables 4-25 through 4-26 and Tables 4-30 through 4-51.<br>Updated PLL specifications in Table 4-52. | — |