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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

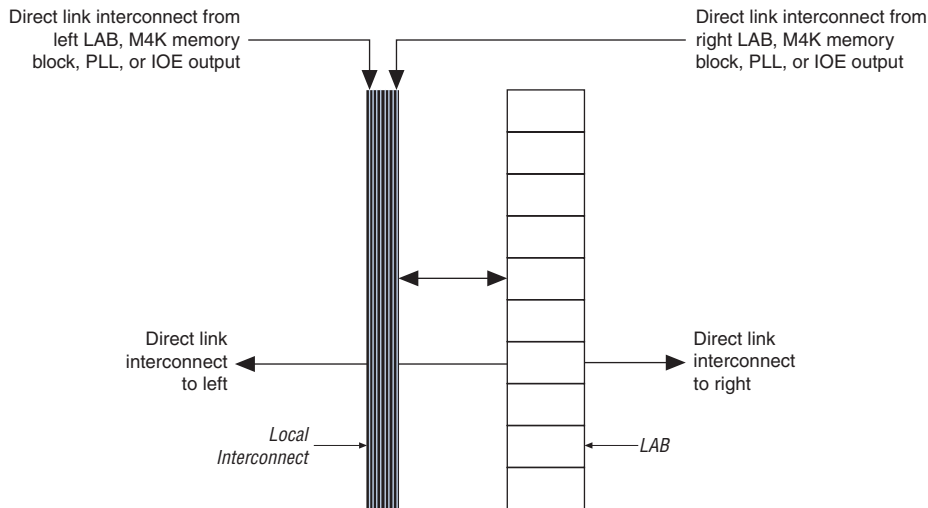
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	4000
Total RAM Bits	78336
Number of I/O	301
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c4f400i7

performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

Figure 2–3. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within a LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows a LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. [“MultiTrack Interconnect” on page 2–12](#) for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either $A + B$ or $A - B$. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The Cyclone LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in [Figure 2-7](#), the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

$$\text{data1} + \text{data2} + \text{carry-in0}$$

or

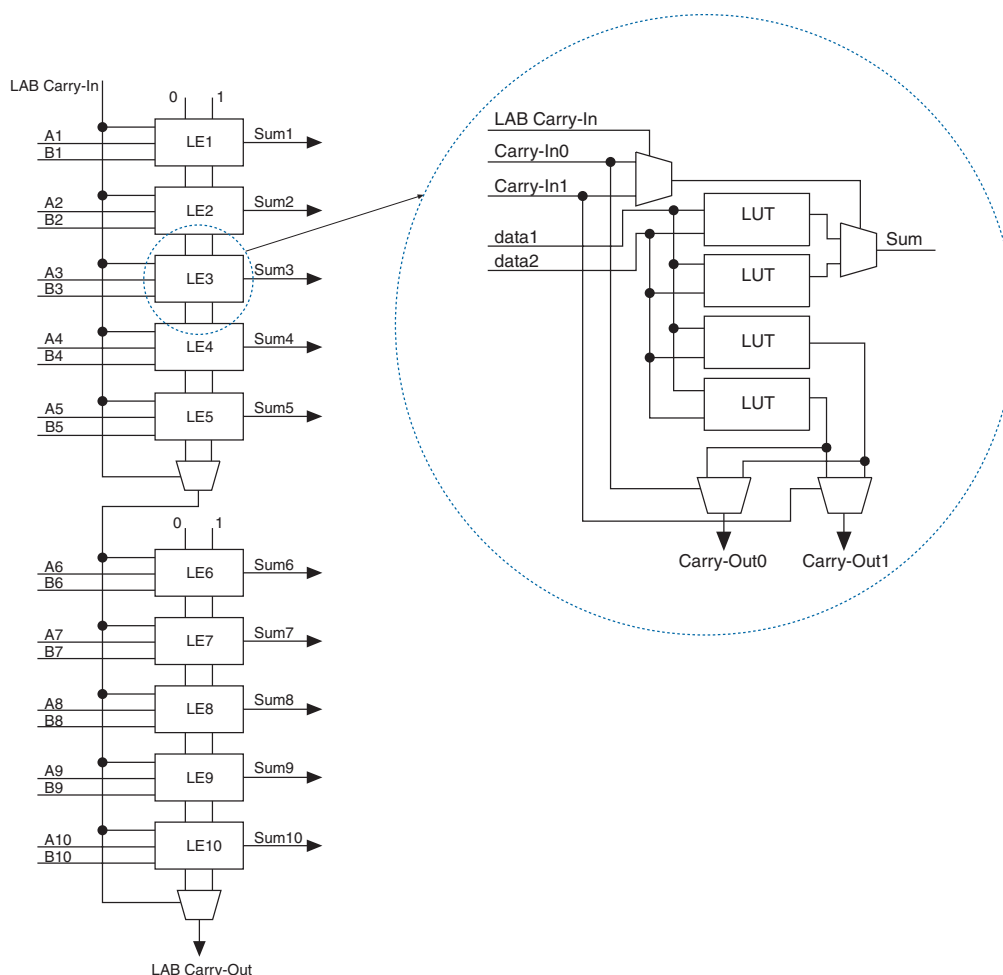
$$\text{data1} + \text{data2} + \text{carry-in1}$$

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8 shows the carry-select circuitry in a LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. A LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, *carry-in0* or *carry-in1*, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

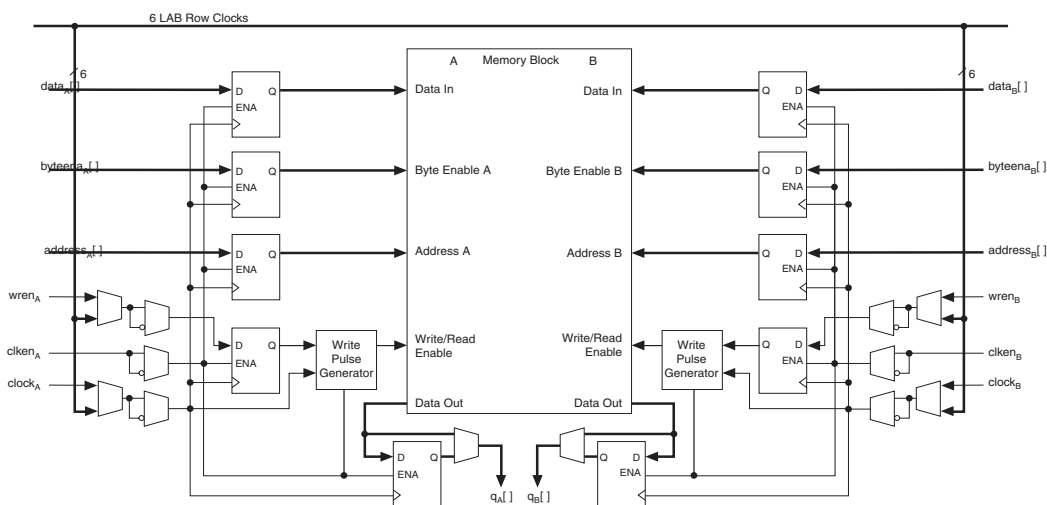
Figure 2–8. Carry Select Chain



Independent Clock Mode

The M4K memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–17 shows an M4K memory block in independent clock mode.

Figure 2–17. Independent Clock Mode Notes (1), (2)

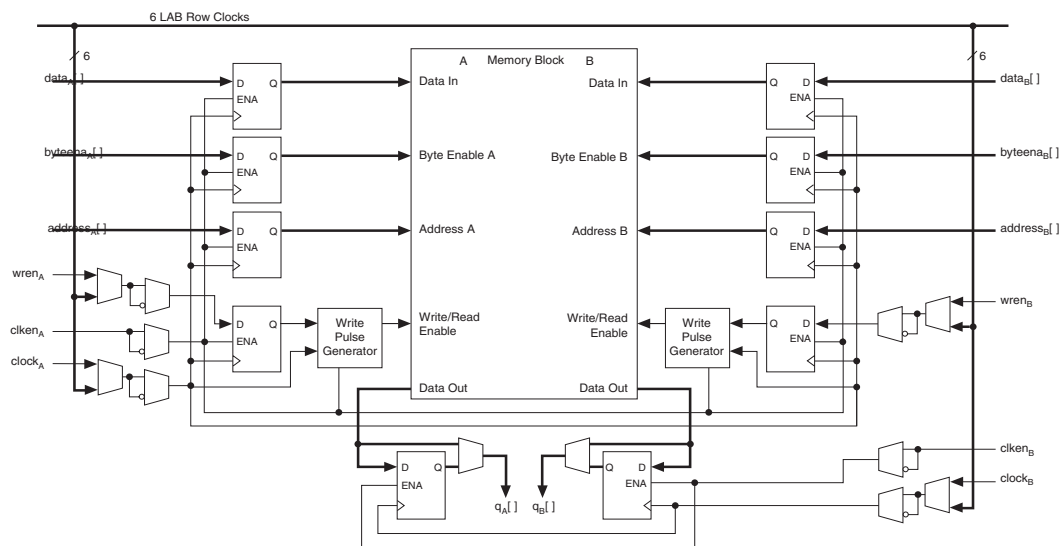


Notes to Figure 2–17:

- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Input/Output Clock Mode

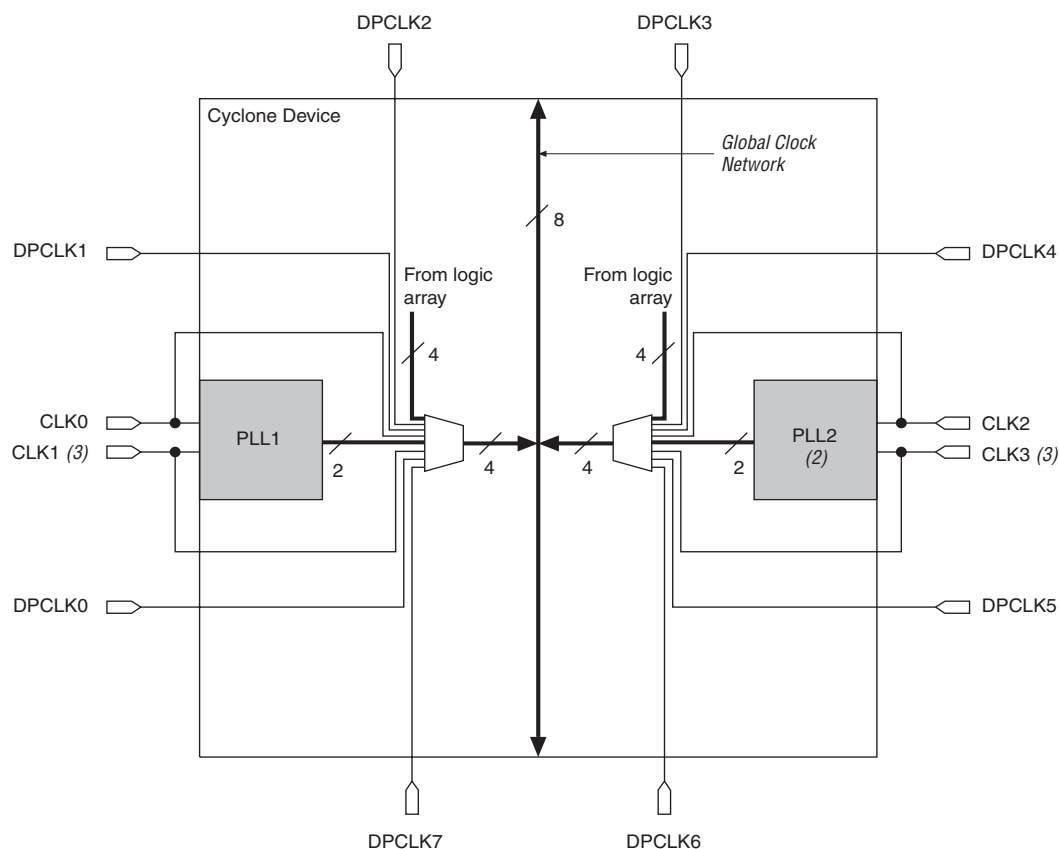
Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, wren, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–18 and 2–19 show the memory block in input/output clock mode.

Figure 2–18. Input/Output Clock Mode in True Dual-Port Mode *Notes (1), (2)***Notes to Figure 2–18:**

- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

The eight global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device—IOEs, LEs, and memory blocks. The global clock lines can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin, or DQS signals for DDR SDRAM or FCRAM interfaces. Internal logic can also drive the global clock network for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–22 shows the various sources that drive the global clock network.

Figure 2–22. Global Clock Generation *Note (1)*



Notes to Figure 2–22:

- (1) The EP1C3 device in the 100-pin TQFP package has five DPCLK pins (DPCLK2, DPCLK3, DPCLK4, DPCLK6, and DPCLK7).
- (2) EP1C3 devices only contain one PLL (PLL 1).
- (3) The EP1C3 device in the 100-pin TQFP package does not have dedicated clock pins CLK1 and CLK3.

Table 2–7. Global Clock Network Sources (Part 2 of 2)

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
Dual-Purpose Clock Pins	DPCLK0 (3)	—	—	—	✓	—	—	—	—
	DPCLK1 (3)	—	—	✓	—	—	—	—	—
	DPCLK2	✓	—	—	—	—	—	—	—
	DPCLK3	—	—	—	—	✓	—	—	—
	DPCLK4	—	—	—	—	—	—	✓	—
	DPCLK5 (3)	—	—	—	—	—	—	—	✓
	DPCLK6	—	—	—	—	—	✓	—	—
	DPCLK7	—	✓	—	—	—	—	—	—

Notes to Table 2–7:

- (1) EP1C3 devices only have one PLL (PLL 1).
- (2) EP1C3 devices in the 100-pin TQFP package do not have dedicated clock pins CLK1 and CLK3.
- (3) EP1C3 devices in the 100-pin TQFP package do not have the DPCLK0, DPCLK1, or DPCLK5 pins.

Clock Multiplication and Division

Cyclone PLLs provide clock synthesis for PLL output ports using $m/(n \times \text{post scale counter})$ scaling factors. The input clock is divided by a pre-scale divider, n , and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter to divide down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least-common multiple in the VCO's range).

Each PLL has one pre-scale divider, n , that can range in value from 1 to 32. Each PLL also has one multiply divider, m , that can range in value from 2 to 32. Global clock outputs have two post scale G dividers for global clock outputs, and external clock outputs have an E divider for external clock output, both ranging from 1 to 32. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

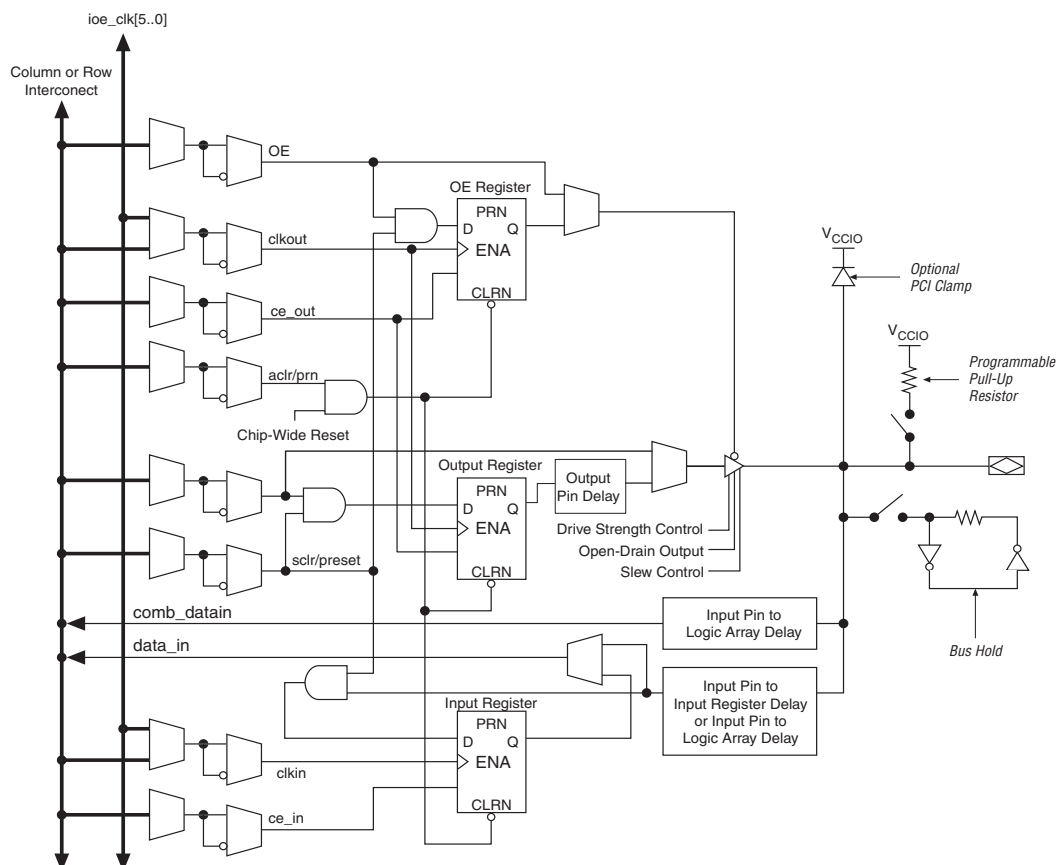
I/O Structure

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

Cyclone device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer.

Figure 2–27 shows the Cyclone IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. IOEs can be used as input, output, or bidirectional pins.

Figure 2–32. Cyclone IOE in Bidirectional I/O Configuration

The Cyclone device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays

Operating Modes

The Cyclone architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Cyclone devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the V_{CCIO} of the bank where the pins reside. The bank V_{CCIO} selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Configuration Schemes

Designers can load the configuration data for a Cyclone device with one of three configuration schemes (see [Table 3–5](#)), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone device. A low-cost configuration device can automatically configure a Cyclone device at system power-up.

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0$, $I_{OH} = -0.1$ mA	$V_{CCIO} - 0.2$	—	V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0$, $I_{OL} = 0.1$ mA	—	0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	$I_{OH} = -0.1$ mA	2.1	—	V
		$I_{OH} = -1$ mA	2.0	—	V
		$I_{OH} = -2$ to -16 mA (11)	1.7	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 0.1$ mA	—	0.2	V
		$I_{OH} = 1$ mA	—	0.4	V
		$I_{OH} = 2$ to 16 mA (11)	—	0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.65	1.95	V
V_{IH}	High-level input voltage	—	$0.65 \times V_{CCIO}$	2.25 (12)	V
V_{IL}	Low-level input voltage	—	–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2$ to -8 mA (11)	$V_{CCIO} - 0.45$	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ to 8 mA (11)	—	0.45	V

Typically, the user-mode current during device operation is lower than the power-up current in Table 4–17. Altera recommends using the Cyclone Power Calculator, available on the Altera web site, to estimate the user-mode I_{CCINT} consumption and then select power supplies or regulators based on the higher value.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–18 shows the status of the Cyclone device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–18. Cyclone Device Timing Model Status

Device	Preliminary	Final
EP1C3	—	✓
EP1C4	—	✓
EP1C6	—	✓
EP1C12	—	✓
EP1C20	—	✓

Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in [Table 4–19](#).

Table 4–19. Clock Tree Maximum Performance Specification

Parameter	Definition	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock tree f_{MAX}	Maximum frequency that the clock tree can support for clocking registered logic	—	—	405	—	—	320	—	—	275	MHz

[Table 4–20](#) shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
LE	16-to-1 multiplexer	—	21	—	—	405.00	320.00	275.00
	32-to-1 multiplexer	—	44	—	—	317.36	284.98	260.15
	16-bit counter	—	16	—	—	405.00	320.00	275.00
	64-bit counter (1)	—	66	—	—	208.99	181.98	160.75

Table 4–20. Cyclone Device Performance

Resource Used	Design Size and Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
M4K memory block	RAM 128 × 36 bit	Single port	—	4,608	1	256.00	222.67	197.01
	RAM 128 × 36 bit	Simple dual-port mode	—	4,608	1	255.95	222.67	196.97
	RAM 256 × 18 bit	True dual-port mode	—	4,608	1	255.95	222.67	196.97
	FIFO 128 × 36 bit	—	40	4,608	1	256.02	222.67	197.01
	Shift register 9 × 4 × 128	Shift register	11	4,536	1	255.95	222.67	196.97

Note to Table 4–20:

(1) The performance numbers for this function are from an EP1C6 device in a 240-pin PQFP package.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–21 through 4–24 describe the Cyclone device internal timing microparameters for LEs, IOEs, M4K memory structures, and MultiTrack interconnects.

Table 4–21. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–29. Cyclone Global Clock External I/O Timing Parameters Notes (1), (2) (Part 2 of 2)

Symbol	Parameter	Conditions
t_{OUTCOPLL}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock enhanced PLL with default phase setting	$C_{\text{LOAD}} = 10 \text{ pF}$

Notes to Table 4–29:

- (1) These timing parameters are sample-tested only.
- (2) These timing parameters are for IOE pins using a 3.3-V LVTTTL, 24-mA setting. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–30 through 4–31 show the external timing parameters on column and row pins for EP1C3 devices.

Table 4–30. EP1C3 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.085	—	3.547	—	4.009	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	4.073	2.000	4.682	2.000	5.295	ns
t_{INSUPLL}	1.795	—	2.063	—	2.332	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCOPLL}	0.500	2.306	0.500	2.651	0.500	2.998	ns

Table 4–31. EP1C3 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.157	—	3.630	—	4.103	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.984	2.000	4.580	2.000	5.180	ns
t_{INSUPLL}	1.867	—	2.146	—	2.426	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCOPLL}	0.500	2.217	0.500	2.549	0.500	2.883	ns

Tables 4–34 through 4–35 show the external timing parameters on column and row pins for EP1C6 devices.

Table 4–34. EP1C6 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.691	—	3.094	—	3.496	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.917	2.000	4.503	2.000	5.093	ns
t_{INSUPLL}	1.513	—	1.739	—	1.964	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCOPLL}	0.500	2.038	0.500	2.343	0.500	2.651	ns

Table 4–35. EP1C6 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.774	—	3.190	—	3.605	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.817	2.000	4.388	2.000	4.963	ns
t_{INSUPLL}	1.596	—	1.835	—	2.073	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCOPLL}	0.500	1.938	0.500	2.228	0.500	2.521	ns

Tables 4–36 through 4–37 show the external timing parameters on column and row pins for EP1C12 devices.

Table 4–36. EP1C12 Column Pin Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.510	—	2.885	—	3.259	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.798	2.000	4.367	2.000	4.940	ns
t_{INSUPLL}	1.588	—	1.824	—	2.061	—	ns

Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.5-V LVTTTL	2 mA	—	6,789	—	7,807	—	8,825	ps
	4 mA	—	5,109	—	5,875	—	6,641	ps
	8 mA	—	4,793	—	5,511	—	6,230	ps
SSTL-3 class I		—	1,390	—	1,598	—	1,807	ps
SSTL-3 class II		—	989	—	1,137	—	1,285	ps
SSTL-2 class I		—	1,965	—	2,259	—	2,554	ps
SSTL-2 class II		—	1,692	—	1,945	—	2,199	ps
LVDS		—	802	—	922	—	1,042	ps

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 1 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	1,800	—	2,070	—	2,340	ps
	4 mA	—	1,311	—	1,507	—	1,704	ps
	8 mA	—	945	—	1,086	—	1,228	ps
	12 mA	—	807	—	928	—	1,049	ps
3.3-V LVTTTL	4 mA	—	1,831	—	2,105	—	2,380	ps
	8 mA	—	1,484	—	1,705	—	1,928	ps
	12 mA	—	973	—	1,118	—	1,264	ps
	16 mA	—	1,012	—	1,163	—	1,315	ps
	24 mA	—	838	—	963	—	1,089	ps
2.5-V LVTTTL	2 mA	—	2,747	—	3,158	—	3,570	ps
	8 mA	—	1,757	—	2,019	—	2,283	ps
	12 mA	—	1,763	—	2,026	—	2,291	ps
	16 mA	—	1,623	—	1,865	—	2,109	ps
1.8-V LVTTTL	2 mA	—	5,506	—	6,331	—	7,157	ps
	8 mA	—	4,220	—	4,852	—	5,485	ps
	12 mA	—	4,008	—	4,608	—	5,209	ps
1.5-V LVTTTL	2 mA	—	6,789	—	7,807	—	8,825	ps
	4 mA	—	5,109	—	5,875	—	6,641	ps
	8 mA	—	4,793	—	5,511	—	6,230	ps
3.3-V PCI		—	923	—	1,061	—	1,199	ps

Referenced Document

This chapter references the following documents:

- *Cyclone Architecture* chapter in the *Cyclone Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*

Document Revision History

Table 4–53 shows the revision history for this chapter.

Table 4–53. Document Revision History		
Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.7	Minor textual and style changes. Added “Referenced Document” section.	—
January 2007 v1.6	<ul style="list-style-type: none"> Added document revision history. Added new row for V_{CCA} details in Table 4–1. Updated R_{CONF} information in Table 4–3. Added new <i>Note (12)</i> on voltage overdrive information to Table 4–7 and Table 4–8. Updated <i>Note (9)</i> on R_{CONF} information to Table 4–3. Updated information in “External I/O Delay Parameters” section. Updated speed grade information in Table 4–46 and Table 4–47. Updated LVDS information in Table 4–51. 	—
August 2005 v1.5	Minor updates.	—
February 2005 v1.4	<ul style="list-style-type: none"> Updated information on Undershoot voltage. Updated Table 4-2. Updated Table 4-3. Updated the undershoot voltage from 0.5 V to 2.0 V in Note 3 of Table 4-16. Updated Table 4-17. 	—
January 2004 v.1.3	<ul style="list-style-type: none"> Added extended-temperature grade device information. Updated Table 4-2. Updated I_{CC0} information in Table 4-3. 	—
October 2003 v.1.2	<ul style="list-style-type: none"> Added clock tree information in Table 4-19. Finalized timing information for EP1C3 and EP1C12 devices. Updated timing information in Tables 4-25 through 4-26 and Tables 4-30 through 4-51. Updated PLL specifications in Table 4-52. 	—

July 2003 v1.1	Updated timing information. Timing finalized for EP1C6 and EP1C20 devices. Updated performance information. Added PLL Timing section.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—