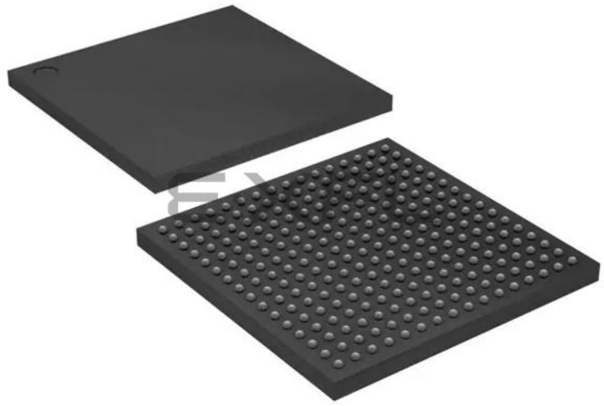
Intel - EP1C6F256I7N Datasheet



Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	598
Number of Logic Elements/Cells	5980
Total RAM Bits	92160
Number of I/O	185
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1c6f256i7n

to the appropriate plane on the board. The Quartus II software reserves I/O pins as power pins as necessary for layout with the larger densities in the same package having more power pins.

Table 1–3. Cyclone QFP and FineLine BGA Package Sizes

Dimension	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0.5	0.5	0.5	1.0	1.0	1.0
Area (mm^2)	256	484	1,024	289	361	441
Length × width (mm × mm)	16×16	22×22	34.6×34.6	17×17	19×19	21×21

Document Revision History

Table 1–4 shows the revision history for this document.

Table 1–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.5	Minor textual and style changes.	—
January 2007 v1.4	Added document revision history.	—
August 2005 v1.3	Minor updates.	—
October 2003 v1.2	Added 64-bit PCI support information.	—
September 2003 v1.1	● Updated LVDS data rates to 640 Mbps from 311 Mbps. ● Updated RSDS feature information.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

2. Cyclone Architecture

C51002-1.6

Functional Description

Cyclone® devices contain a two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varying speeds provide signal interconnects between LABs and embedded memory blocks.

The logic array consists of LABs, with 10 LEs in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. Cyclone devices range between 2,910 to 20,060 LEs.

M4K RAM blocks are true dual-port memory blocks with 4K bits of memory plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 250 MHz. These blocks are grouped into columns across the device in between certain LABs. Cyclone devices offer between 60 to 288 Kbits of embedded RAM.

Each Cyclone device I/O pin is fed by an I/O element (IOE) located at the ends of LAB rows and columns around the periphery of the device. I/O pins support various single-ended and differential I/O standards, such as the 66- and 33-MHz, 64- and 32-bit PCI standard and the LVDS I/O standard at up to 640 Mbps. Each IOE contains a bidirectional I/O buffer and three registers for registering input, output, and output-enable signals. Dual-purpose DQS, DQ, and DM pins along with delay chains (used to phase-align DDR signals) provide interface support with external memory devices such as DDR SDRAM, and FCRAM devices at up to 133 MHz (266 Mbps).

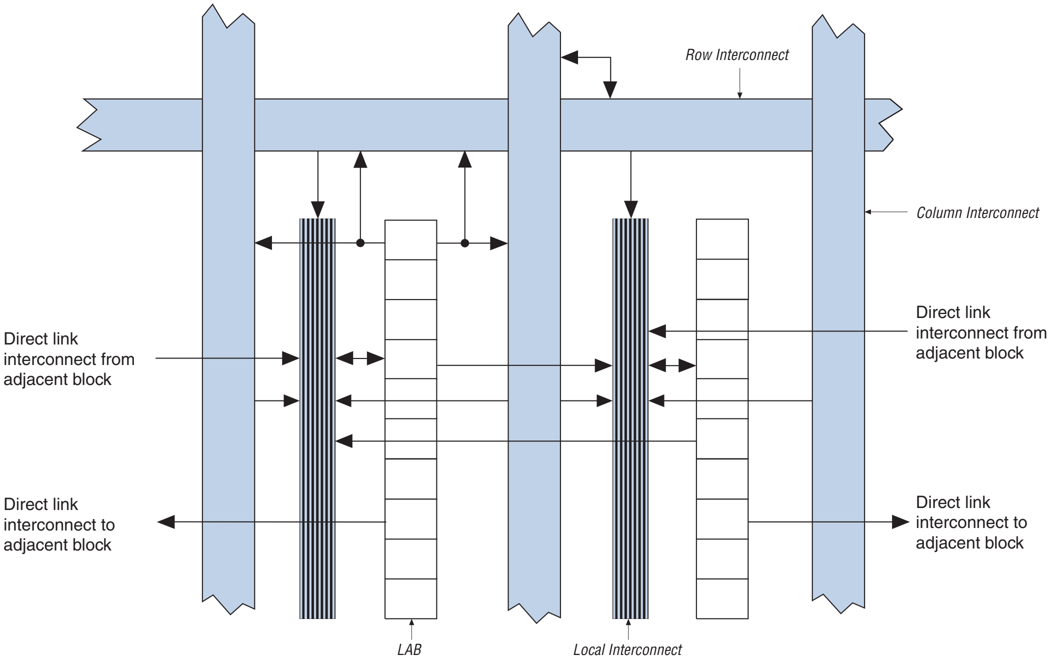
Cyclone devices provide a global clock network and up to two PLLs. The global clock network consists of eight global clock lines that drive throughout the entire device. The global clock network can provide clocks for all resources within the device, such as IOEs, LEs, and memory blocks. The global clock lines can also be used for control signals. Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as external outputs for high-speed differential I/O support.

Figure 2–1 shows a diagram of the Cyclone EP1C12 device.

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, look-up table (LUT) chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within a LAB. The Quartus® II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 details the Cyclone LAB.

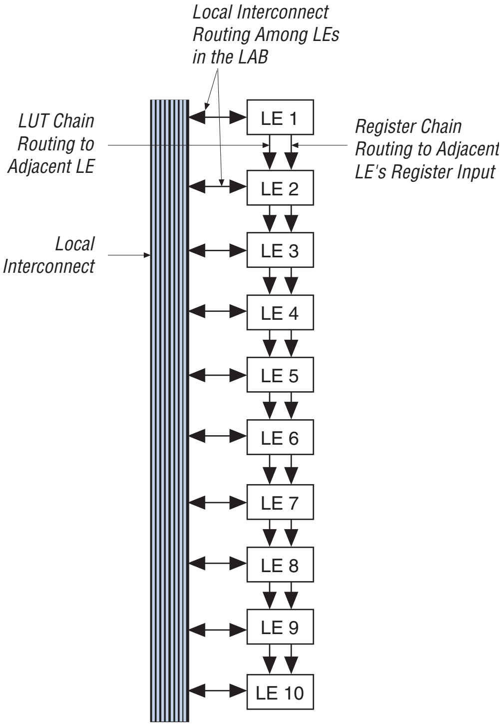
Figure 2–2. Cyclone LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, and M4K RAM blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher

Figure 2–10. LUT Chain and Register Chain Interconnects



The C4 interconnects span four LABs or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–11 shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including PLLs, M4K memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., M4K memory or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–2 shows the Cyclone device's routing scheme.

Table 2–2. Cyclone Device Routing Scheme

Source	Destination										
	LUT Chain	**Register Chain**	**Local Interconnect**	**Direct Link Interconnect**	**R4 Interconnect**	**C4 Interconnect**	**LE**	**M4K RAM Block**	**PLL**	**Column IOE**	**Row IOE**
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	✓
Direct Link Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	—	—	—
M4K RAM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
PLL	—	—	—	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

signal. The output registers can be bypassed. Pseudo-asynchronous reading is possible in the simple dual-port mode of M4K blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple M4K memory blocks. For example, two 256×16-bit RAM blocks can be combined to form a 256×32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words allowed. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

Parity Bit Support

The M4K blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. Byte enables are also available for data input masking during write operations.

Shift Register Support

You can configure M4K memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a $w \times m \times n$ shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n). The size of a $w \times m \times n$ shift register must be less than or equal to the maximum number of memory bits in the M4K block (4,608 bits). The total number of shift is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–3 and 2–4 summarize the possible M4K RAM block configurations.

Table 2–3. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓	—	—	—
2K × 2	✓	✓	✓	✓	✓	✓	—	—	—
1K × 4	✓	✓	✓	✓	✓	✓	—	—	—
512 × 8	✓	✓	✓	✓	✓	✓	—	—	—
256 × 16	✓	✓	✓	✓	✓	✓	—	—	—
128 × 32	✓	✓	✓	✓	✓	✓	—	—	—
512 × 9	—	—	—	—	—	—	✓	✓	✓
256 × 18	—	—	—	—	—	—	✓	✓	✓
128 × 36	—	—	—	—	—	—	✓	✓	✓

Table 2–4. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓	—	—
2K × 2	✓	✓	✓	✓	✓	—	—
1K × 4	✓	✓	✓	✓	✓	—	—
512 × 8	✓	✓	✓	✓	✓	—	—
256 × 16	✓	✓	✓	✓	✓	—	—
512 × 9	—	—	—	—	—	✓	✓
256 × 18	—	—	—	—	—	✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 2–15. M4K RAM Block Control Signals

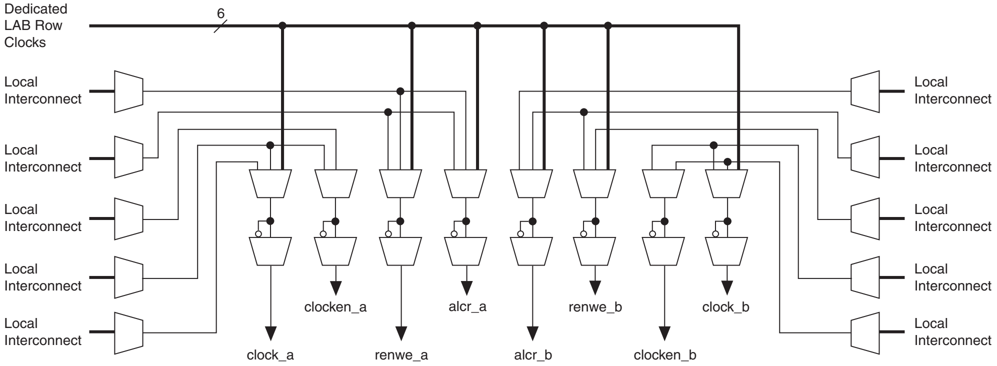


Figure 2–16. M4K RAM Block LAB Row Interface

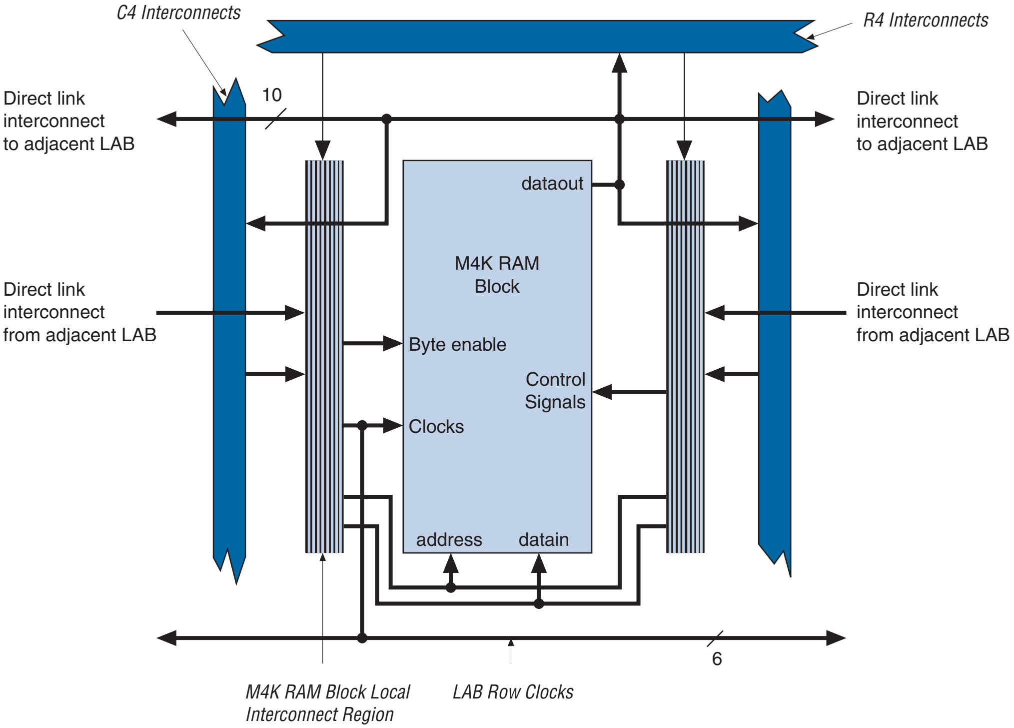


Table 2–7. Global Clock Network Sources (Part 2 of 2)

Source		GCLK0	GCLK1	GCLK2	GCLK3	GCLK4	GCLK5	GCLK6	GCLK7
Dual-Purpose Clock Pins	DPCLK0 *(3)*	—	—	—	✓	—	—	—	—
	DPCLK1 *(3)*	—	—	✓	—	—	—	—	—
	DPCLK2	✓	—	—	—	—	—	—	—
	DPCLK3	—	—	—	—	✓	—	—	—
	DPCLK4	—	—	—	—	—	—	✓	—
	DPCLK5 *(3)*	—	—	—	—	—	—	—	✓
	DPCLK6	—	—	—	—	—	✓	—	—
	DPCLK7	—	✓	—	—	—	—	—	—

Notes to Table 2–7:

(1) EP1C3 devices only have one PLL (PLL 1).

(2) EP1C3 devices in the 100-pin TQFP package do not have dedicated clock pins `CLK1` and `CLK3`.

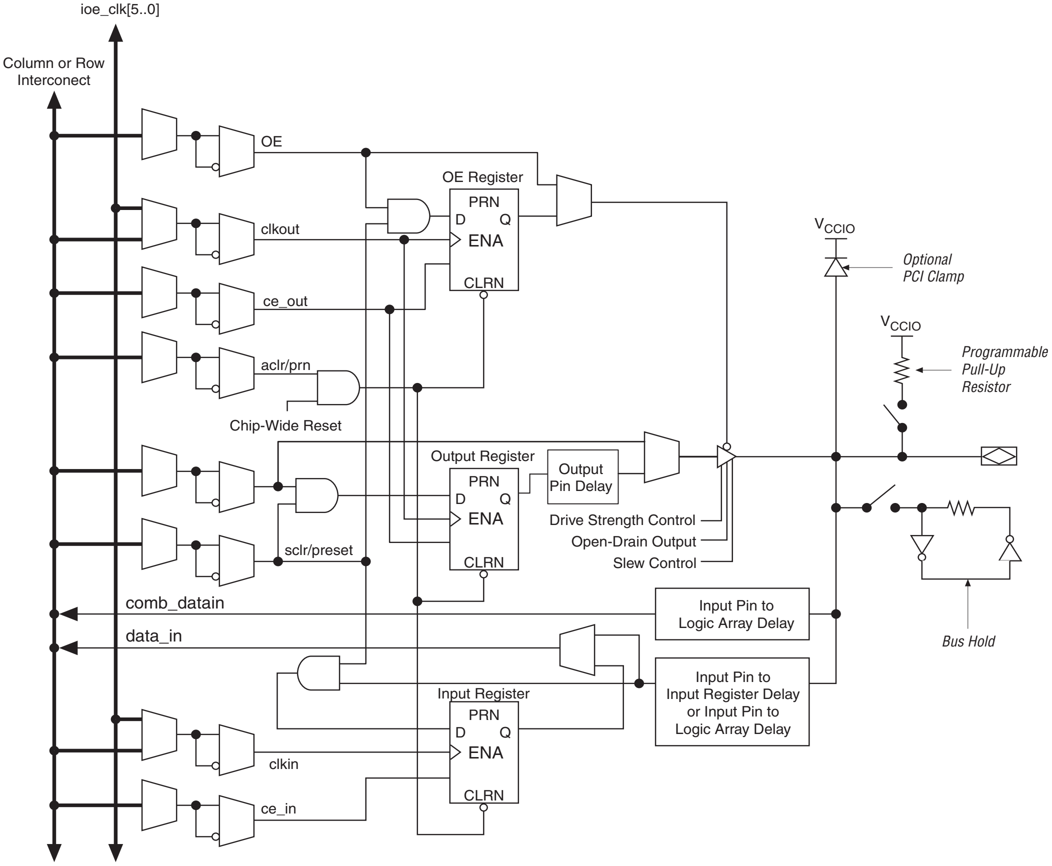
(3) EP1C3 devices in the 100-pin TQFP package do not have the `DPCLK0`, `DPCLK1`, or `DPCLK5` pins.

Clock Multiplication and Division

Cyclone PLLs provide clock synthesis for PLL output ports using $m/(n \times$ post scale counter) scaling factors. The input clock is divided by a pre-scale divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter to divide down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least-common multiple in the VCO's range).

Each PLL has one pre-scale divider, n, that can range in value from 1 to 32. Each PLL also has one multiply divider, m, that can range in value from 2 to 32. Global clock outputs have two post scale G dividers for global clock outputs, and external clock outputs have an E divider for external clock output, both ranging from 1 to 32. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Figure 2–32. Cyclone IOE in Bidirectional I/O Configuration



The Cyclone device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays

Table 2–10. DQ Pin Groups (Part 2 of 2)

Device	Package	Number of × 8 DQ Pin Groups	Total DQ Pin Count
EP1C6	144-pin TQFP	4	32
	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
EP1C12	240-pin PQFP	4	32
	256-pin FineLine BGA	4	32
	324-pin FineLine BGA	8	64
EP1C20	324-pin FineLine BGA	8	64
	400-pin FineLine BGA	8	64

Note to Table 2–10:

(1) EP1C3 devices in the 100-pin TQFP package do not have any DQ pin groups in I/O bank 1.

A programmable delay chain on each DQS pin allows for either a 90° phase shift (for DDR SDRAM), or a 72° phase shift (for FCRAM) which automatically center-aligns input DQS synchronization signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal clocks DQ signals on internal LE registers.

These DQS delay elements combine with the PLL's clocking and phase shift ability to provide a complete hardware solution for interfacing to high-speed memory.

The clock phase shift allows the PLL to clock the DQ output enable and output paths. The designer should use the following guidelines to meet 133 MHz performance for DDR SDRAM and FCRAM interfaces:

- The DQS signal must be in the middle of the DQ group it clocks
- Resynchronize the incoming data to the logic array clock using successive LE registers or FIFO buffers
- LE registers must be placed in the LAB adjacent to the DQ I/O pin column it is fed by

Figure 2–34 illustrates DDR SDRAM and FCRAM interfacing from the I/O through the dedicated circuitry to the logic array.

4. DC and Switching Characteristics

C51004-1.7

Operating Conditions

Cyclone® devices are offered in both commercial, industrial, and extended temperature grades. However, industrial-grade and extended-temperature-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Cyclone devices.

Table 4–1. Cyclone Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_{CCA}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	BGA packages under bias	—	135	°C

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(5)*	–0.5	4.1	V

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA	—	0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.1	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1	—	V
		I_{OH} = –1 mA	2.0	—	V
		I_{OH} = –2 to –16 mA *(11)*	1.7	—	V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	—	0.2	V
		I_{OH} = 1 mA	—	0.4	V
		I_{OH} = 2 to 16 mA *(11)*	—	0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage	—	1.65	1.95	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(12)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(11)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(11)*	—	0.45	V

Table 4–16. Cyclone Device Capacitance *Note (14)*

Symbol	Parameter	Typical	Unit
C_{IO}	Input capacitance for user I/O pin	4.0	pF
C_{LVDS}	Input capacitance for dual-purpose LVDS/user I/O pin	4.7	pF
C_{VREF}	Input capacitance for dual-purpose V_{REF}/user I/O pin.	12.0	pF
C_{DPCLK}	Input capacitance for dual-purpose `DPCLK`/user I/O pin.	4.4	pF
C_{CLK}	Input capacitance for CLK pin.	4.7	pF

Notes to Tables 4–1 through 4–16:

(1) Refer to the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.

(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(7) V_I = ground, no load, no toggling inputs.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(9) R_{CONF} is the measured value of internal pull-up resistance when the I/O pin is tied directly to GND. R_{CONF} value will be lower if an external source drives the pin higher than V_{CCIO}.

(10) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

(11) Drive strength is programmable according to values in *Cyclone Architecture* chapter in the *Cyclone Device Handbook*.

(12) Overdrive is possible when a 1.5 V or 1.8 V and a 2.5 V or 3.3 V input signal feeds an input pin. Turn on “Allow voltage overdrive” for LVTTL/LVCMOS input pins in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combination. However, higher leakage current is expected.

(13) The Cyclone LVDS interface requires a resistor network outside of the transmitter channels.

(14) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

Typically, the user-mode current during device operation is lower than the power-up current in Table 4–17. Altera recommends using the Cyclone Power Calculator, available on the Altera web site, to estimate the user-mode I_{CCINT} consumption and then select power supplies or regulators based on the higher value.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–18 shows the status of the Cyclone device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–18. Cyclone Device Timing Model Status

Device	Preliminary	Final
EP1C3	—	✓
EP1C4	—	✓
EP1C6	—	✓
EP1C12	—	✓
EP1C20	—	✓

Table 4–22. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	IOE input and output register setup time before clock
t_{H}	IOE input and output register hold time after clock
t_{CO}	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–23. M4K Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width

Table 4–29. Cyclone Global Clock External I/O Timing Parameters Notes (1), (2) (Part 2 of 2)

Symbol	Parameter	Conditions
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 4–29:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for IOE pins using a 3.3-V LVTTL, 24-mA setting. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–30 through 4–31 show the external timing parameters on column and row pins for EP1C3 devices.

Table 4–30. EP1C3 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.085	—	3.547	—	4.009	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	4.073	2.000	4.682	2.000	5.295	ns
$t_{INSUPLL}$	1.795	—	2.063	—	2.332	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	2.306	0.500	2.651	0.500	2.998	ns

Table 4–31. EP1C3 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.157	—	3.630	—	4.103	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.984	2.000	4.580	2.000	5.180	ns
$t_{INSUPLL}$	1.867	—	2.146	—	2.426	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	2.217	0.500	2.549	0.500	2.883	ns

Table 4–39. EP1C20 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.417	—	2.779	—	3.140	—	ns
t_{INH}	0.000	—	0.000	—	0.000	—	ns
t_{OUTCO}	2.000	3.724	2.000	4.282	2.000	4.843	ns
t_{XZ}	—	3.645	—	4.191	—	4.740	ns
t_{ZX}	—	3.645	—	4.191	—	4.740	ns
$t_{INSUPLL}$	1.417	—	1.629	—	1.840	—	ns
t_{INHPLL}	0.000	—	0.000	—	0.000	—	ns
$t_{OUTCOPLL}$	0.500	1.667	0.500	1.917	0.500	2.169	ns
t_{XZPLL}	—	1.588	—	1.826	—	2.066	ns
t_{ZXPLL}	—	1.588	—	1.826	—	2.066	ns

External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–40 through 4–45 show the adder delays associated with column and row I/O pins for all packages. If an I/O standard is selected other than LVTTL 4 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters shown in Tables 4–25 through 4–28.

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS	—	0	—	0	—	0	ps
3.3-V LVTTL	—	0	—	0	—	0	ps
2.5-V LVTTL	—	27	—	31	—	35	ps
1.8-V LVTTL	—	182	—	209	—	236	ps
1.5-V LVTTL	—	278	—	319	—	361	ps
SSTL-3 class I	—	–250	—	–288	—	–325	ps
SSTL-3 class II	—	–250	—	–288	—	–325	ps
SSTL-2 class I	—	–278	—	–320	—	–362	ps

Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.5-V LVTTL	2 mA	—	6,789	—	7,807	—	8,825	ps
	4 mA	—	5,109	—	5,875	—	6,641	ps
	8 mA	—	4,793	—	5,511	—	6,230	ps
SSTL-3 class I		—	1,390	—	1,598	—	1,807	ps
SSTL-3 class II		—	989	—	1,137	—	1,285	ps
SSTL-2 class I		—	1,965	—	2,259	—	2,554	ps
SSTL-2 class II		—	1,692	—	1,945	—	2,199	ps
LVDS		—	802	—	922	—	1,042	ps

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 1 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA	—	1,800	—	2,070	—	2,340	ps
	4 mA	—	1,311	—	1,507	—	1,704	ps
	8 mA	—	945	—	1,086	—	1,228	ps
	12 mA	—	807	—	928	—	1,049	ps
3.3-V LVTTL	4 mA	—	1,831	—	2,105	—	2,380	ps
	8 mA	—	1,484	—	1,705	—	1,928	ps
	12 mA	—	973	—	1,118	—	1,264	ps
	16 mA	—	1,012	—	1,163	—	1,315	ps
	24 mA	—	838	—	963	—	1,089	ps
2.5-V LVTTL	2 mA	—	2,747	—	3,158	—	3,570	ps
	8 mA	—	1,757	—	2,019	—	2,283	ps
	12 mA	—	1,763	—	2,026	—	2,291	ps
	16 mA	—	1,623	—	1,865	—	2,109	ps
1.8-V LVTTL	2 mA	—	5,506	—	6,331	—	7,157	ps
	8 mA	—	4,220	—	4,852	—	5,485	ps
	12 mA	—	4,008	—	4,608	—	5,209	ps
1.5-V LVTTL	2 mA	—	6,789	—	7,807	—	8,825	ps
	4 mA	—	5,109	—	5,875	—	6,641	ps
	8 mA	—	4,793	—	5,511	—	6,230	ps
3.3-V PCI		—	923	—	1,061	—	1,199	ps

February 2005 v1.1	Updated Figure 5-1.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—