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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 598 |
| Number of Logic Elements/Cells | 5980 |
| Total RAM Bits | 92160 |
| Number of I/O | 185 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1c6q240c7n |

| Table 1–1. Cyclone Device Features  (Part 2 of 2) | | | | | |
|---|---|---|---|---|---|
| Feature | EP1C3 | EP1C4 | EP1C6 | EP1C12 | EP1C20 |
| Total RAM bits | 59,904 | 78,336 | 92,160 | 239,616 | 294,912 |
| PLLs | 1 | 2 | 2 | 2 | 2 |
| Maximum user I/O pins (1) | 104 | 301 | 185 | 249 | 301 |

Note to Table 1–1:
(1)    This parameter includes global clock pins.

Cyclone devices are available in quad flat pack (QFP) and space-saving FineLine® BGA packages (see Tables 1–2 through 1–3).

| Table 1–2. Cyclone Package Options and I/O Pin Counts | | | | | | |
|---|---|---|---|---|---|---|
| Device | 100-Pin TQFP (1) | 144-Pin TQFP (1), (2) | 240-Pin PQFP (1) | 256-Pin FineLine BGA | 324-Pin FineLine BGA | 400-Pin FineLine BGA |
| EP1C3 | 65 | 104 | — | — | — | — |
| EP1C4 | — | — | — | — | 249 | 301 |
| EP1C6 | — | 98 | 185 | 185 | — | — |
| EP1C12 | — | — | 173 | 185 | 249 | — |
| EP1C20 | — | — | — | — | 233 | 301 |

Notes to Table 1–2:
(1)    TQFP: thin quad flat pack.
        PQFP: plastic quad flat pack.
(2)    Cyclone devices support vertical migration within the same package (i.e., designers can migrate between the EP1C3 device in the 144-pin TQFP package and the EP1C6 device in the same package).

Vertical migration means you can migrate a design from one device to another that has the same dedicated pins, JTAG pins, and power pins, and are subsets or supersets for a given package across device densities. The largest density in any package has the  highest number of power pins; you must use the layout for the largest planned density in a package to provide the necessary power pins for migration.

For I/O pin migration across densities, cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list. If one device has power or ground pins, but these same pins are user I/O on a different device that is in the migration path,the Quartus II software ensures the pins are not used as user I/O in the Quartus II software. Ensure that these pins are connected

*Figure 2–1. Cyclone EP1C12 Device Block Diagram*
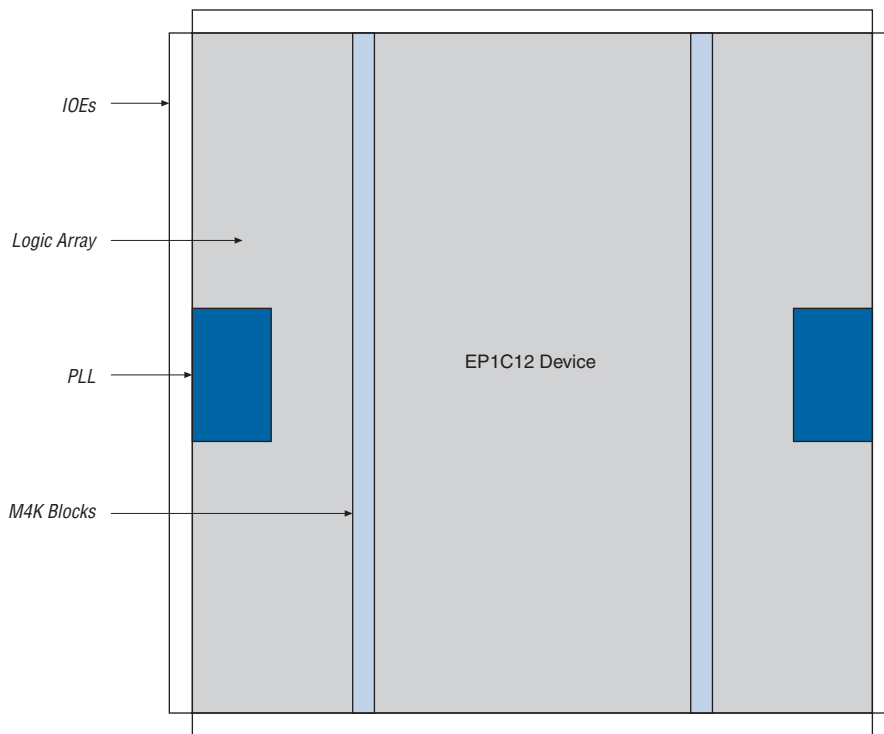


The number of M4K RAM blocks, PLLs, rows, and columns vary per device. Table 2–1 lists the resources available in each Cyclone device.

| Table 2–1. Cyclone Device Resources | | | | | |
|---|---|---|---|---|---|
| **Device** | **M4K RAM** | | **PLLs** | **LAB Columns** | **LAB Rows** |
| | **Columns** | **Blocks** | | | |
| EP1C3 | 1 | 13 | 1 | 24 | 13 |
| EP1C4 | 1 | 17 | 2 | 26 | 17 |
| EP1C6 | 1 | 20 | 2 | 32 | 20 |
| EP1C12 | 2 | 52 | 2 | 48 | 26 |
| EP1C20 | 2 | 64 | 2 | 64 | 32 |

*Figure 2–10. LUT Chain and Register Chain Interconnects*
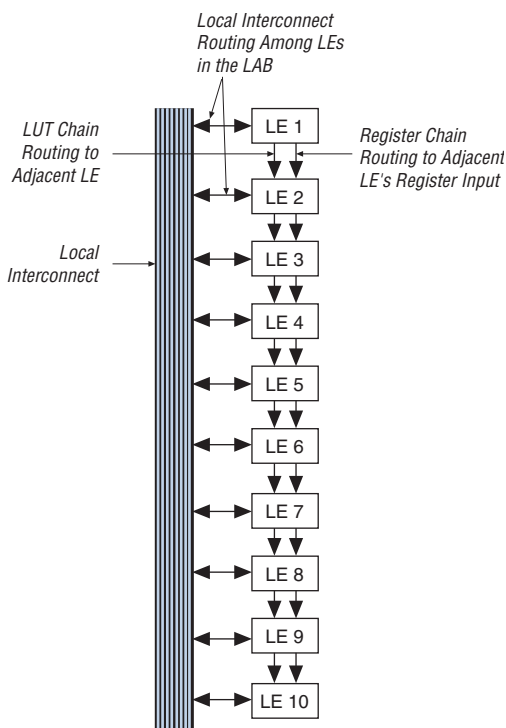


The C4 interconnects span four LABs or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–11 shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including PLLs, M4K memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

*Figure 2–19. Input/Output Clock Mode in Simple Dual-Port Mode*     *Notes (1), (2)*
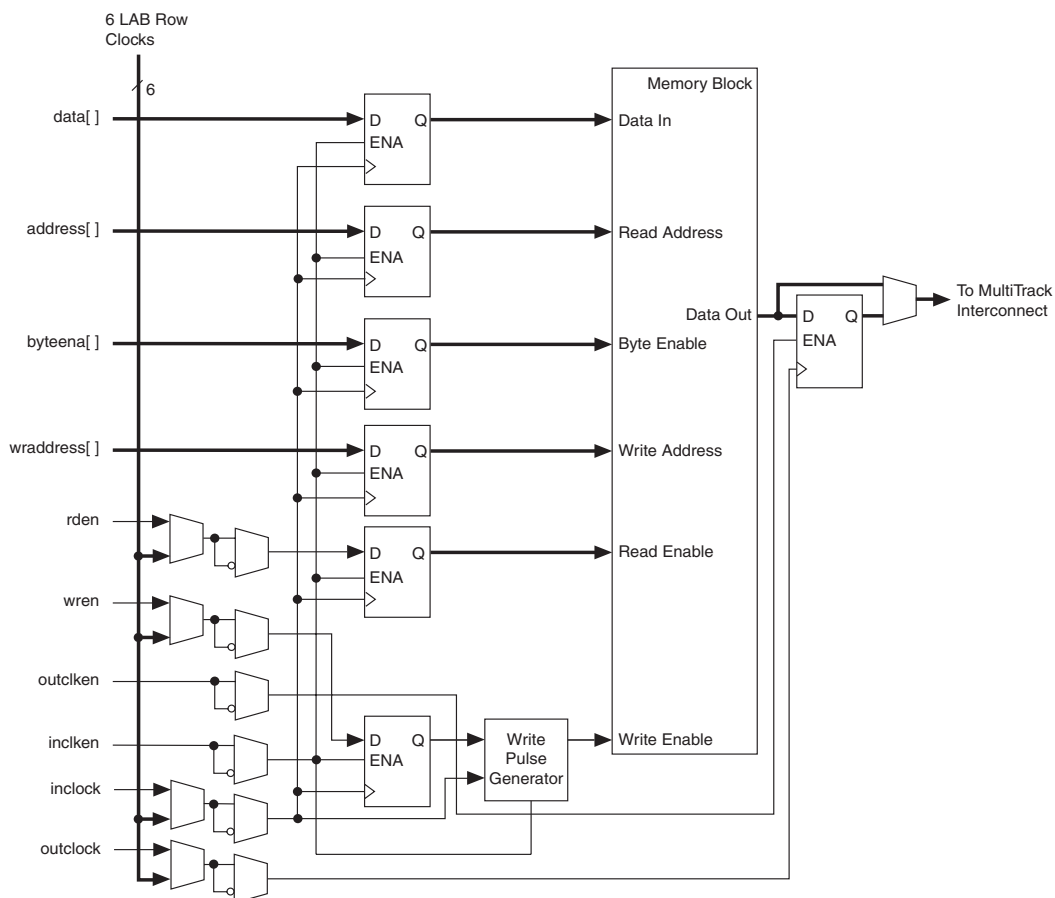


***Notes to Figure 2–19:***
(1)    All registers shown except the rden register have asynchronous clear ports.
(2)    Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

## Single-Port Mode

The M4K memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–21. A single M4K memory block can support up to two single-port mode RAM blocks if each RAM block is less than or equal to 2K bits in size.

*Figure 2–21. Single-Port Mode    Note (1)*
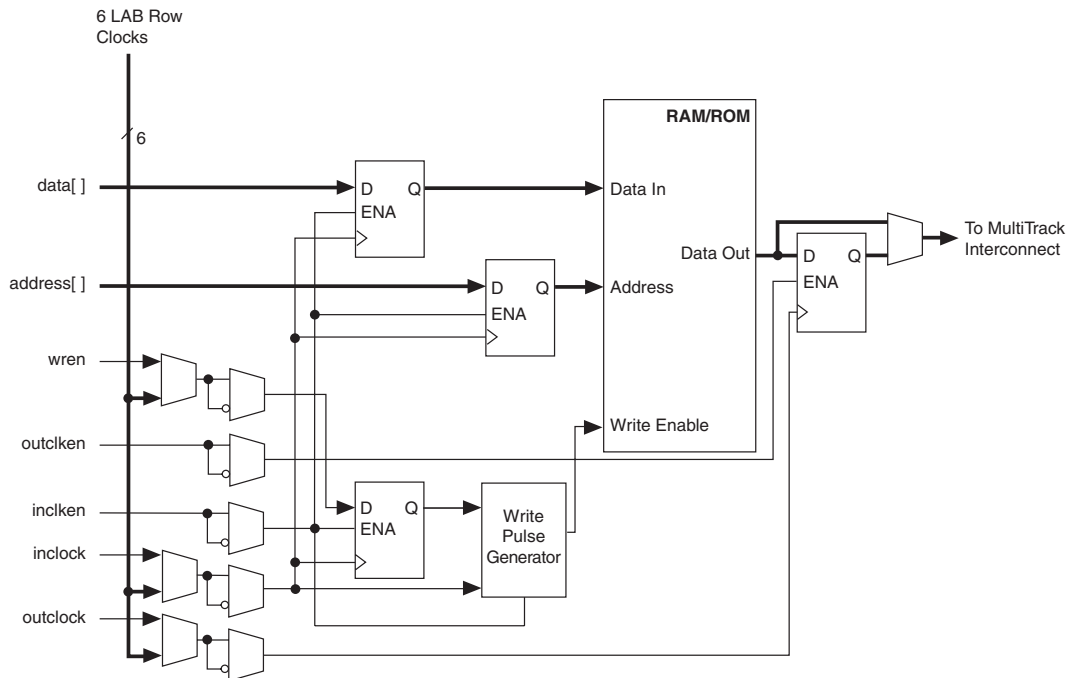


*Note to Figure 2–21:*
(1)   Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

# Global Clock Network and Phase-Locked Loops

Cyclone devices provide a global clock network and up to two PLLs for a complete clock management solution.

## Global Clock Network

There are four dedicated clock pins (CLK[3..0], two pins on the left side and two pins on the right side) that drive the global clock network, as shown in Figure 2–22. PLL outputs, logic array, and dual-purpose clock (DPCLK[7..0]) pins can also drive the global clock network.

does not have dedicated clock output pins. The EP1C6 device in the 144-pin TQFP package only supports dedicated clock outputs from PLL 1.

## Clock Feedback

Cyclone PLLs have three modes for multiplication and/or phase shifting:

■ Zero delay buffer mode—The external clock output pin is phase-aligned with the clock input pin for zero delay.

■ Normal mode—If the design uses an internal PLL clock output, the normal mode compensates for the internal clock delay from the input clock pin to the IOE registers. The external clock output pin is phase shifted with respect to the clock input pin if connected in this mode. You defines which internal clock output from the PLL should be phase-aligned to compensate for internal clock delay.

■ No compensation mode—In this mode, the PLL will not compensate for any clock networks.

## Phase Shifting

Cyclone PLLs have an advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 125 to 250 ps. The finest resolution equals one eighth of the VCO period. The VCO period is a function of the frequency input and the multiplication and division factors. Each clock output counter can choose a different phase of the VCO period from up to eight taps. You can use this clock output counter along with an initial setting on the post-scale counter to achieve a phase-shift range for the entire period of the output clock. The phase tap feedback to the m counter can shift all outputs to a single phase. The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entered.

## Lock Detect Signal

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. Therefore, you may need to gate the lock signal for use as a system-control signal. For correct operation of the lock circuit below –20 C, $f_{IN/N} > 200$ MHz.

## Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (g0, g1, e). The duty cycle setting is achieved by a low- and high-time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

## Control Signals

There are three control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

The `pllenable` signal enables and disables PLLs. When the `pllenable` signal is low, the clock output ports are driven by ground and all the PLLs go out of lock. When the `pllenable` signal goes high again, the PLLs relock and resynchronize to the input clocks. An input pin or LE output can drive the `pllenable` signal.

The `areset` signals are reset/resynchronization inputs for each PLL. Cyclone devices can drive these input signals from input pins or from LEs. When `areset` is driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use their own control signal or gated locked status signals to trigger the `pfdena` signal.

For more information about Cyclone PLLs, refer to *Using PLLs in Cyclone Devices* chapter in the *Cyclone Device Handbook*.

*Figure 2–27. Cyclone IOE Structure*
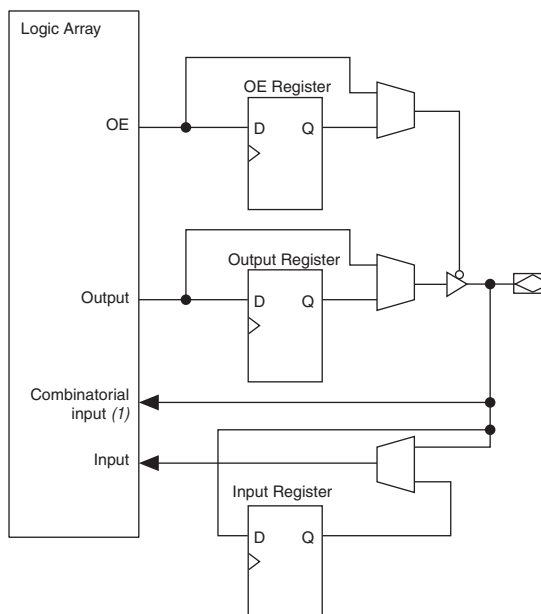


Note to *Figure 2–27*:
(1)    There are two paths available for combinatorial inputs to the logic array. Each path contains a unique programmable delay chain.

The IOEs are located in I/O blocks around the periphery of the Cyclone device. There are up to three IOEs per row I/O block and up to three IOEs per column I/O block (column I/O blocks span two columns). The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–28 shows how a row I/O block connects to the logic array. Figure 2–29 shows how a column I/O block connects to the logic array.

*Figure 2–29. Column I/O Block Connection to the Interconnect*
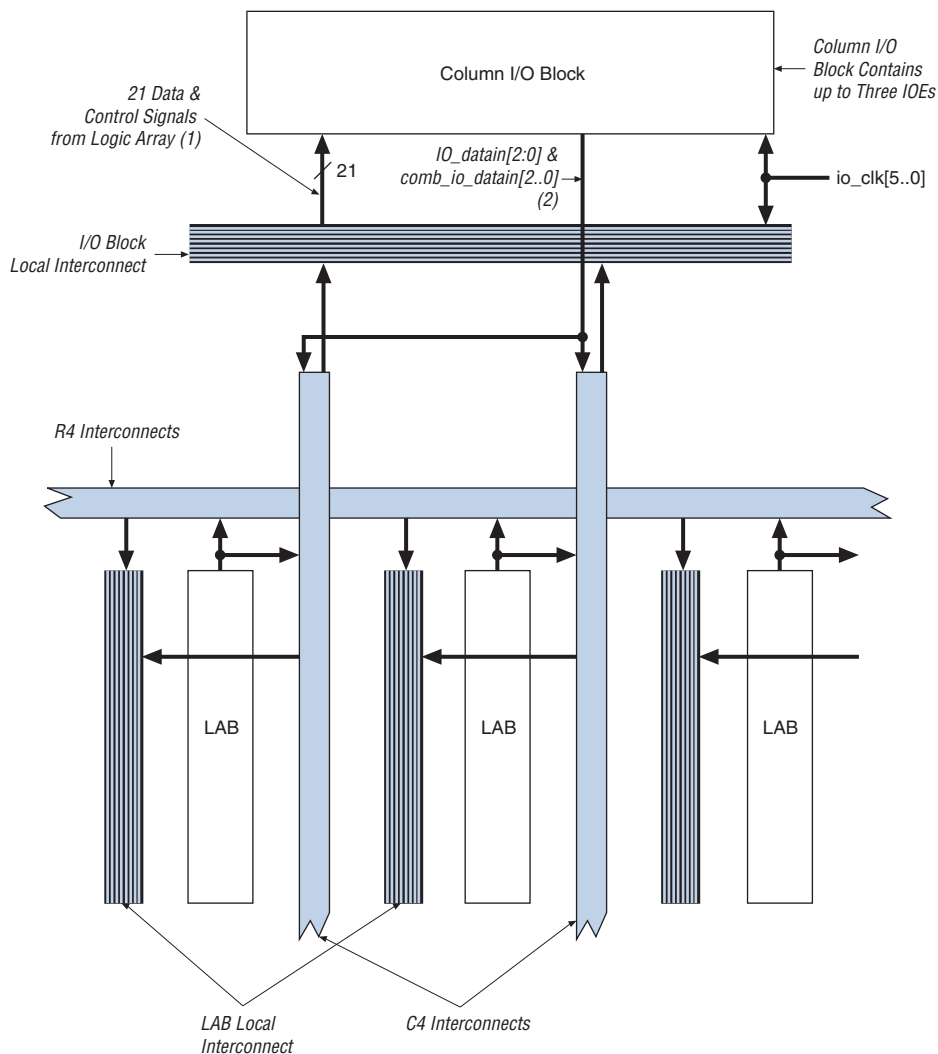


*Notes to Figure 2–29:*
(1)  The 21 data and control signals consist of three data out lines, `io_dataout[2..0]`, three output enables, `io_coe[2..0]`, three input clock enables, `io_cce_in[2..0]`, three output clock enables, `io_cce_out[2..0]`, three clocks, `io_cclk[2..0]`, three asynchronous clear signals, `io_caclr[2..0]`, and three synchronous clear signals, `io_csclr[2..0]`.
(2)  Each of the three IOEs in the column I/O block can have one `io_datain` input (combinatorial or registered) and one `comb_io_datain` (combinatorial) input.

The Cyclone $V_{CCINT}$ pins must always be connected to a 1.5-V power supply. If the $V_{CCINT}$ level is 1.5 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The $V_{CCIO}$ pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when $V_{CCIO}$ pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When $V_{CCIO}$ pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V or 5.0-V systems. Table 2–14 summarizes Cyclone MultiVolt I/O support.

| *Table 2–14. Cyclone MultiVolt I/O Support* *Note (1)* | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **$V_{CCIO}$ (V)** | **Input Signal** | | | | | **Output Signal** | | | | |
| | **1.5 V** | **1.8 V** | **2.5 V** | **3.3 V** | **5.0 V** | **1.5 V** | **1.8 V** | **2.5 V** | **3.3 V** | **5.0 V** |
| 1.5 | ✓ | ✓ | ✓ *(2)* | ✓ *(2)* | — | ✓ | — | — | — | — |
| 1.8 | ✓ | ✓ | ✓ *(2)* | ✓ *(2)* | — | ✓ *(3)* | ✓ | — | — | — |
| 2.5 | — | — | ✓ | ✓ | — | ✓ *(5)* | ✓ *(5)* | ✓ | — | — |
| 3.3 | — | — | ✓ *(4)* | ✓ | ✓ *(6)* | ✓ *(7)* | ✓ *(7)* | ✓ *(7)* | ✓ | ✓ *(8)* |

*Notes to Table 2–14:*
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$.
(2) When $V_{CCIO}$ = 1.5-V or 1.8-V and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected. Turn on **Allow voltage overdrive for LVTTL / LVCMOS input pins** in the Assignments > Device > Device and Pin Options > Pin Placement tab when a device has this I/O combinations.
(3) When $V_{CCIO}$ = 1.8-V, a Cyclone device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When $V_{CCIO}$ = 3.3-V and a 2.5-V input signal feeds an input pin, the $V_{CCIO}$ supply current will be slightly larger than expected.
(5) When $V_{CCIO}$ = 2.5-V, a Cyclone device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(6) Cyclone devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.
(7) When $V_{CCIO}$ = 3.3-V, a Cyclone device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
(8) When $V_{CCIO}$ = 3.3-V, a Cyclone device can drive a device with 5.0-V LVTTL inputs but not 5.0-V LVCMOS inputs.

# Power Sequencing and Hot Socketing

Because Cyclone devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the $V_{CCIO}$ and $V_{CCINT}$ power supplies may be powered in any order.

Signals can be driven into Cyclone devices before and during power up without damaging the device. In addition, Cyclone devices do not drive out during power up. Once operating conditions are reached and the device is configured, Cyclone devices operate as specified by the user.

*Table 3–1. Cyclone JTAG Instructions (Part 2 of 2)*

| JTAG Instruction | Instruction Code | Description |
|---|---|---|
| USERCODE | 00 0000 0111 | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | 00 0000 0110 | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| HIGHZ *(1)* | 00 0000 1011 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |
| CLAMP *(1)* | 00 0000 1010 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | — | Used when configuring a Cyclone device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor. |
| PULSE_NCONFIG | 00 0000 0001 | Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected. |
| CONFIG_IO | 00 0000 1101 | Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction will hold nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured. |
| SignalTap II instructions | — | Monitors internal device operation with the SignalTap II embedded logic analyzer. |

*Note to Table 3–1:*

(1)   Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

In the Quartus II software, there is an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. Choose Assignments > Device > Device and Pin Options > General. Turn on **Auto Usercode**.

Multiple Cyclone devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 3–5. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Active serial | Low-cost serial configuration device |
| Passive serial (PS) | Enhanced or EPC2 configuration device, MasterBlaster or ByteBlasterMV download cable, or serial data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file |

## Referenced Documents

This chapter references the following document:

■ *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
■ *Jam Programming & Test Language Specification*

## Document Revision History

Table 3–6 shows the revision history for this chapter.

*Table 3–6. Document Revision History*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| May 2008 v1.4 | Minor textual and style changes. Added "Referenced Documents" section. | — |
| January 2007 v1.3 | ● Added document revision history.<br>● Updated handpara note below Table 3–4. | — |
| August 2005 V1.2 | Minor updates. | — |
| February 2005 V1.1 | Updated JTAG chain limits. Added information concerning test vectors. | — |
| May 2003 v1.0 | Added document to Cyclone Device Handbook. | — |

**Table 4–2. Cyclone Device Recommended Operating Conditions  (Part 2 of 2)**

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | 85 | $^\circ$ C |
| | | For industrial use | –40 | 100 | $^\circ$ C |
| | | For extended-temperature use | –40 | 125 | $^\circ$ C |

**Table 4–3. Cyclone Device DC Operating Conditions**     *Note (6)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I = V_{CCIOmax}$ to 0 V *(8)* | –10 | — | 10 | μA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O = V_{CCIOmax}$ to 0 V *(8)* | –10 | — | 10 | μA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All M4K blocks in power-down mode) *(7)* | EP1C3 | — | 4 | — | mA |
| | | EP1C4 | — | 6 | — | mA |
| | | EP1C6 | — | 6 | — | mA |
| | | EP1C12 | — | 8 | — | mA |
| | | EP1C20 | — | 12 | — | mA |
| $R_{CONF}$ *(9)* | Value of I/O pin pull-up resistor before and during configuration | $V_I = 0$ V; $V_{CCI0} = 3.3$ V | 15 | 25 | 50 | kΩ |
| | | $V_I = 0$ V; $V_{CCI0} = 2.5$ V | 20 | 45 | 70 | kΩ |
| | | $V_I = 0$ V; $V_{CCI0} = 1.8$ V | 30 | 65 | 100 | kΩ |
| | | $V_I = 0$ V; $V_{CCI0} = 1.5$ V | 50 | 100 | 150 | kΩ |
| | Recommended value of I/O pin external pull-down resistor before and during configuration | — | — | 1 | 2 | kΩ |

**Table 4–4. LVTTL Specifications**

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | — | 1.7 | 4.1 | V |
| $V_{IL}$ | Low-level input voltage | — | –0.5 | 0.7 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -4$ to $-24$ mA *(11)* | 2.4 | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 4$ to 24 mA *(11)* | — | 0.45 | V |

### Table 4–10. 3.3-V PCI Specifications  (Part 2 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OUT} = -500\ \mu A$ | $0.9 \times V_{CCIO}$ | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT} = 1{,}500\ \mu A$ | — | — | $0.1 \times V_{CCIO}$ | V |

### Table 4–11. SSTL-2 Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | — | $V_{REF} - 0.04$ | $V_{REF}$ | $V_{REF} + 0.04$ | V |
| $V_{REF}$ | Reference voltage | — | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | — | $V_{REF} + 0.18$ | — | 3.0 | V |
| $V_{IL}$ | Low-level input voltage | — | −0.3 | — | $V_{REF} - 0.18$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -8.1$ mA *(11)* | $V_{TT} + 0.57$ | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 8.1$ mA *(11)* | — | — | $V_{TT} - 0.57$ | V |

### Table 4–12. SSTL-2 Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 2.3 | 2.5 | 2.7 | V |
| $V_{TT}$ | Termination voltage | — | $V_{REF} - 0.04$ | $V_{REF}$ | $V_{REF} + 0.04$ | V |
| $V_{REF}$ | Reference voltage | — | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | — | $V_{REF} + 0.18$ | — | $V_{CCIO} + 0.3$ | V |
| $V_{IL}$ | Low-level input voltage | — | −0.3 | — | $V_{REF} - 0.18$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -16.4$ mA *(11)* | $V_{TT} + 0.76$ | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 16.4$ mA *(11)* | — | — | $V_{TT} - 0.76$ | V |

### Table 4–13. SSTL-3 Class I Specifications  (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | — | $V_{REF} - 0.05$ | $V_{REF}$ | $V_{REF} + 0.05$ | V |

**Table 4–29. Cyclone Global Clock External I/O Timing Parameters** *Notes (1), (2)* **(Part 2 of 2)**

| Symbol | Parameter | Conditions |
|---|---|---|
| t<sub>OUTCOPLL</sub> | Clock-to-output delay output or bidirectional pin using IOE output register with global clock enhanced PLL with default phase setting | C<sub>LOAD</sub> = 10 pF |

*Notes to Table 4–29:*
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for IOE pins using a 3.3-V LVTTL, 24-mA setting. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–30 through 4–31 show the external timing parameters on column and row pins for EP1C3 devices.

**Table 4–30. EP1C3 Column Pin Global Clock External I/O Timing Parameters**

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.085 | — | 3.547 | — | 4.009 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 4.073 | 2.000 | 4.682 | 2.000 | 5.295 | ns |
| $t_{INSUPLL}$ | 1.795 | — | 2.063 | — | 2.332 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.306 | 0.500 | 2.651 | 0.500 | 2.998 | ns |

**Table 4–31. EP1C3 Row Pin Global Clock External I/O Timing Parameters**

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.157 | — | 3.630 | — | 4.103 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.984 | 2.000 | 4.580 | 2.000 | 5.180 | ns |
| $t_{INSUPLL}$ | 1.867 | — | 2.146 | — | 2.426 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.217 | 0.500 | 2.549 | 0.500 | 2.883 | ns |

Tables 4–32 through 4–33 show the external timing parameters on column and row pins for EP1C4 devices.

*Table 4–32. EP1C4 Column Pin Global Clock External I/O Timing Parameters* Note (1)

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.471 | — | 2.841 | — | 3.210 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.937 | 2.000 | 4.526 | 2.000 | 5.119 | ns |
| $t_{INSUPLL}$ | 1.471 | — | 1.690 | — | 1.910 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.080 | 0.500 | 2.392 | 0.500 | 2.705 | ns |

*Table 4–33. EP1C4 Row Pin Global Clock External I/O Timing Parameters* Note (1)

| Symbol | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.600 | — | 2.990 | — | 3.379 | — | ns |
| $t_{INH}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCO}$ | 2.000 | 3.991 | 2.000 | 4.388 | 2.000 | 5.189 | ns |
| $t_{INSUPLL}$ | 1.300 | — | 1.494 | — | 1.689 | — | ns |
| $t_{INHPLL}$ | 0.000 | — | 0.000 | — | 0.000 | — | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.234 | 0.500 | 2.569 | 0.500 | 2.905 | ns |

*Note to Tables 4–32 and 4–33:*
(1)    Contact Altera Applications for EP1C4 device timing parameters.

**Table 4–47. Cyclone IOE Programmable Delays on Row Pins**

| Parameter | Setting | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Decrease input delay to internal cells | Off | — | 154 | — | 177 | — | 200 | ps |
| | Small | — | 2,212 | — | 2,543 | — | 2,875 | ps |
| | Medium | — | 2,639 | — | 3,034 | — | 3,430 | ps |
| | Large | — | 3,057 | — | 3,515 | — | 3,974 | ps |
| | On | — | 154 | — | 177 | — | 200 | ps |
| Decrease input delay to input register | Off | — | 0 | — | 0 | — | 0 | ps |
| | On | — | 3,057 | — | 3,515 | — | 3,974 | ps |
| Increase delay to output pin | Off | — | 0 | — | 0 | — | 0 | ps |
| | On | — | 556 | — | 639 | — | 722 | ps |

*Note to Table 4–47:*
(1)   EPC1C3 devices do not support the PCI I/O standard.

## Maximum Input and Output Clock Rates

Tables 4–48 and 4–49 show the maximum input clock rate for column and row pins in Cyclone devices.

**Table 4–48. Cyclone Maximum Input Clock Rate for Column Pins**

| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 464 | 428 | 387 | MHz |
| 2.5 V | 392 | 302 | 207 | MHz |
| 1.8 V | 387 | 311 | 252 | MHz |
| 1.5 V | 387 | 320 | 243 | MHz |
| LVCMOS | 405 | 374 | 333 | MHz |
| SSTL-3 class I | 405 | 356 | 293 | MHz |
| SSTL-3 class II | 414 | 365 | 302 | MHz |
| SSTL-2 class I | 464 | 428 | 396 | MHz |
| SSTL-2 class II | 473 | 432 | 396 | MHz |
| LVDS | 567 | 549 | 531 | MHz |

### Table 4–49. Cyclone Maximum Input Clock Rate for Row Pins

| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 464 | 428 | 387 | MHz |
| 2.5 V | 392 | 302 | 207 | MHz |
| 1.8 V | 387 | 311 | 252 | MHz |
| 1.5 V | 387 | 320 | 243 | MHz |
| LVCMOS | 405 | 374 | 333 | MHz |
| SSTL-3 class I | 405 | 356 | 293 | MHz |
| SSTL-3 class II | 414 | 365 | 302 | MHz |
| SSTL-2 class I | 464 | 428 | 396 | MHz |
| SSTL-2 class II | 473 | 432 | 396 | MHz |
| 3.3-V PCI *(1)* | 464 | 428 | 387 | MHz |
| LVDS | 567 | 549 | 531 | MHz |

*Note to Tables 4–48 through 4–49:*
(1)    EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

Tables 4–50 and 4–51 show the maximum output clock rate for column and row pins in Cyclone devices.

### Table 4–50. Cyclone Maximum Output Clock Rate for Column Pins

| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 304 | 304 | 304 | MHz |
| 2.5 V | 220 | 220 | 220 | MHz |
| 1.8 V | 213 | 213 | 213 | MHz |
| 1.5 V | 166 | 166 | 166 | MHz |
| LVCMOS | 304 | 304 | 304 | MHz |
| SSTL-3 class I | 100 | 100 | 100 | MHz |
| SSTL-3 class II | 100 | 100 | 100 | MHz |
| SSTL-2 class I | 134 | 134 | 134 | MHz |
| SSTL-2 class II | 134 | 134 | 134 | MHz |
| LVDS | 320 | 320 | 275 | MHz |

*Note to Table 4–50:*
(1)    EP1C3 devices do not support the PCI I/O standard.

| Table 4–52. Cyclone PLL Specifications  (Part 2 of 2) | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $f_{OUT}$ (to global clock) | PLL output frequency (-6 speed grade) | 15.625 | 405 | MHz |
|  | PLL output frequency (-7 speed grade) | 15.625 | 320 | MHz |
|  | PLL output frequency (-8 speed grade) | 15.625 | 275 | MHz |
| $t_{OUT}$ DUTY | Duty cycle for external clock output (when set to 50%) | 45.00 | 55 | % |
| $t_{JITTER}$ *(1)* | Period jitter for external clock output | — | ±300 *(2)* | ps |
| $t_{LOCK}$ *(3)* | Time required to lock from end of device configuration | 10.00 | 100 | μs |
| $f_{VCO}$ | PLL internal VCO operating range | 500.00 | 1,000 | MHz |
| - | Minimum areset time | 10 | — | ns |
| N, G0, G1, E | Counter values | 1 | 32 | integer |

*Notes to Table 4–52:*
(1)  The $t_{JITTER}$ specification for the `PLL[2..1]_OUT` pins are dependent on the I/O pins in its $V_{CCIO}$ bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength or slow slew rate.
(2)  $f_{OUT} \geq 100$ MHz. When the PLL external clock output frequency ($f_{OUT}$) is smaller than 100 MHz, the jitter specification is 60 mUI.
(3)  $f_{IN/N}$ must be greater than 200 MHz to ensure correct lock detect circuit operation below –20 C. Otherwise, the PLL operates with the specified parameters under the specified conditions.