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#### Applications of [Embedded - Microcontroller,](#)

#### Details

Product Status	Active
Module/Board Type	MPU Core
Core Processor	ARM® Cortex®-A5
Co-Processor	-
Speed	500MHz
Flash Size	64Mb Flash, 1Kb EEPROM
RAM Size	1Gb (128M x 8)
Connector Type	Edge Connector
Size / Dimension	1.18" x 1.57" (30mm x 40mm)
Operating Temperature	-40°C ~ 85°C (TA)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27-som1">https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27-som1</a>

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## 4.2 Pin List

The pin list of the SAMA5D27 SOM1 is provided in the following tables.

**Table 4-1. System-On-Module Pin Description: PIOA**

Pin Number	PIO	Power Rail	Other Features	Type
80	PA00	VDDSDHC	SDMMC0_CK/QSPI0_SLK/D0	I/O
76	PA01	VDDSDHC	SDMMC0_CMD/QSPI0_CS/D1	I/O
83	PA02	VDDSDHC	SDMMC0_DAT0/QSPI0_IO0/D2	I/O
81	PA03	VDDSDHC	SDMMC0_DAT1/QSPI0_IO1/D3	I/O
84	PA04	VDDSDHC	SDMMC0_DAT2/QSPI0_IO2/D4	I/O
85	PA05	VDDSDHC	SDMMC0_DAT3/QSPI0_IO3/D5	I/O
86	PA06	VDDSDHC	SDMMC0_DAT4/TIOA5/ FLEXCOM2_IO0/D6	I/O
79	PA07	VDDSDHC	SDMMC0_DAT5/TIOB5/ FLEXCOM2_IO1/D7	I/O
78	PA08	VDDSDHC	SDMMC0_DAT6/TCLK5/ FLEXCOM2_IO2/NWE/NANDWE	I/O
77	PA09	VDDSDHC	SDMMC0_DAT7/TIOA4/ FLEXCOM2_IO3/NCS3	I/O
82	PA10	VDDSDHC	SDMMC0_RSTN/TIOB4/ FLEXCOM2_IO4/A21/NANDALE	I/O
87	PA11	VDDIN_3V3	SDMMC0_VDDSEL/TCLK4/A22/ NANDCLE	I/O
92	PA12	VDDIN_3V3	SDMMC0_WP/IRQ/NRD/NANDOE	I/O
91	PA13	VDDIN_3V3	SDMMC0_CD/FLEXCOM3_IO1/D8	I/O
111	PA14	VDDIN_3V3	SPI0_SPCK/TK1/QSPI0_SCK/ I2SMCK1/FLEXCOM3_IO2/D9	I/O
109	PA15	VDDIN_3V3	SPI0_MOSI/TF1/QSPI0_CS/I2SCK1/ FLEXCOM3_IO0/D10	I/O
112	PA16	VDDIN_3V3	SPI0_MISO/TD1/QSPI0_IO0/ I2SWS1/FLEXCOM3_IO3/D11	I/O
108	PA17	VDDIN_3V3	SPI0_NPCS0/RD1/QSPI0_IO1/ I2SDI1/FLEXCOM3_IO4/D12	I/O
105	PA18	VDDIN_3V3	SPI0_NPCS1/RK1/QSPI0_IO2/ I2SDO1/SDMMC1_DAT0/D13	I/O
101	PA19	VDDIN_3V3	SPI0_NPCS2/RF1/QSPI0_IO3/ TIOA0/SDMMC1_DAT1/D14	I/O

Pin Number	PIO	Power Rail	Other Features	Type
135	PB10	VDDIN_3V3	TIOB3/PWMEXTRG1/QSPI1_IO3	I/O
148	PB11	VDDIN_3V3	LCDDAT0/URXD3/PDMDAT0	I/O
151	PB12	VDDIN_3V3	LCDDAT1/UTXD3/PDMCLK0	I/O
155	PB13	VDDIN_3V3	LCDDAT2/PCK1	I/O
150	PB14	VDDIN_3V3	LCDDAT3/TK1/I2SMCK1	I/O
162	PB15	VDDIN_3V3	LCDDAT4/TF1/I2SCK1	I/O
154	PB16	VDDIN_3V3	LCDDAT5/TD1/I2SWS1	I/O
157	PB17	VDDIN_3V3	LCDDAT6/RD1/I2SDI1	I/O
152	PB18	VDDIN_3V3	LCDDAT7/RK1/I2SDO1	I/O
158	PB19	VDDIN_3V3	LCDDAT8/RF1/TIOA3	I/O
156	PB20	VDDIN_3V3	LCDDAT9/TK0/TIOB3/PCK1	I/O
164	PB21	VDDIN_3V3	LCDDAT10/TF0/TCLK3/ FLEXCOM3_IO2	I/O
161	PB22	VDDIN_3V3	LCDDAT11/TD0/TIOA2/ FLEXCOM3_IO1	I/O
160	PB23	VDDIN_3V3	LCDDAT12/RD0/TIOB2/ FLEXCOM3_IO0	I/O
168	PB24	VDDIN_3V3	LCDDAT13/RK0/TCLK2/ FLEXCOM3_IO3	I/O
159	PB25	VDDIN_3V3	LCDDAT14/RF0/FLEXCOM3_IO4	I/O
169	PB26	VDDIN_3V3	LCDDAT15/URXD0	I/O
163	PB27	VDDIN_3V3	LCDDAT16/UTXD0	I/O
167	PB28	VDDIN_3V3	LCDDAT17/FLEXCOM0_IO0/TIOA5	I/O
144	PB29	VDDIN_3V3	LCDDAT18/FLEXCOM0_IO1/TIOB5	I/O
165	PB30	VDDIN_3V3	LCDDAT19/FLEXCOM0_IO2/TCLK5	I/O
143	PB31	VDDIN_3V3	LCDDAT20/FLEXCOM0_IO3	I/O

**Table 4-3. System On Module Pin Table : PIOC**

Pin Number	PIO	Power Rail	Other Features	Type
145	PC00	VDDIN_3V3	LCDDAT21/FLEXCOM0_IO4	I/O
141	PC01	VDDIN_3V3	LCDDAT22/CANTX0/SPI1_SPCK/ I2SCK0	I/O
146	PC02	VDDIN_3V3	LCDDAT23/CANRX0/SPI1_MOSI/ I2SMCK0	I/O

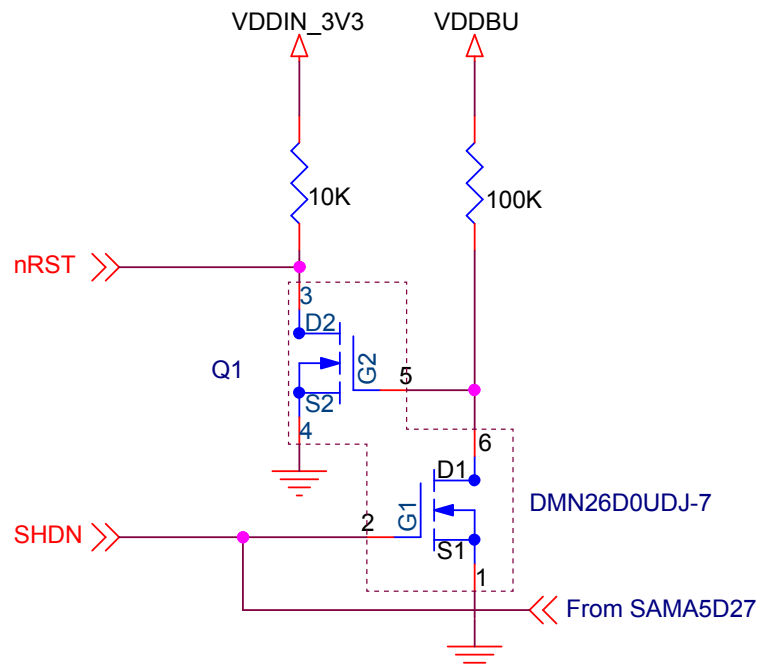
Pin Number	PIO	Power Rail	Other Features	Type
142	PC03	VDDIN_3V3	LCDPWM/TIOA1/SPI1_MISO/ I2SWS0	I/O
136	PC04	VDDIN_3V3	LCDDISP/TIOB1/SPI1_NPCS0/ I2SDI0	I/O
137	PC05	VDDIN_3V3	LCDVSYNC/TCLK1/SPI1_NPCS1/ I2SDO0	I/O
140	PC06	VDDIN_3V3	LCDHSYNC/TWD1/SPI1_NPCS2	I/O
139	PC07	VDDIN_3V3	LCDPCK/TWCK1/SPI1_NPCS3/ URXD1	I/O
138	PC08	VDDIN_3V3	LCDDEN/FIQ/PCK0/UTXD1	I/O
2	PC09	VDDISC	FIQ/ISI_D0/TIOA4	I/O
9	PC10	VDDISC	ISI_D1/TIOB4/CANTX0	I/O
175	PC11	VDDISC	ISI_D2/TCLK4/CANRX0/A0/NBS0	I/O
3	PC12	VDDISC	ISI_D3/URXD3/TK0/A1	I/O
4	PC13	VDDISC	ISI_D4/UTXD3/TF0/A2	I/O
8	PC14	VDDISC	ISI_D5/TD0/A3	I/O
12	PC15	VDDISC	ISI_D6/RD0/A4	I/O
174	PC16	VDDISC	ISI_D7/RK0/A5	I/O
5	PC17	VDDISC	ISI_D8/RF0/A6	I/O
172	PC18	VDDISC	ISI_D9/FLEXCOM3_IO2/A7	I/O
6	PC19	VDDISC	ISI_D10/FLEXCOM3_IO1/A8	I/O
14	PC20	VDDISC	ISI_D11/FLEXCOM3_IO0/A9	I/O
7	PC21	VDDISC	ISI_PCK/FLEXCOM3_IO3/A10	I/O
11	PC22	VDDISC	ISI_VSYNC/FLEXCOM3_IO4/A11	I/O
170	PC23	VDDISC	ISI_HSYNC/A12	I/O
13	PC24	VDDISC	ISI_MCK/A13	I/O
173	PC25	VDDISC	ISI_FIELD/A14	I/O
115	PC26	VDDIN_3V3	CANTX1/A15	I/O
114	PC27	VDDIN_3V3	PCK1/CANRX1/A16	I/O
117	PC28	VDDIN_3V3	FLEXCOM4_IO0/PCK2/A17	I/O
118	PC29	VDDIN_3V3	FLEXCOM4_IO1/A18	I/O
120	PC30	VDDIN_3V3	FLEXCOM4_IO2/A19	I/O
116	PC31	VDDIN_3V3	FLEXCOM4_IO3/URXD3/A20	I/O

Pin Number	PIO	Power Rail	Designation	Type
74	DATA	VDDHSIC	USB High-Speed Inter-Chip Data	–
73	STROBE	VDDHSIC	USB High-Speed Inter-Chip Strobe	–
60	NRST	VDDIN_3V3	Microprocessor reset	Input / Active Low
33	PIOBU1	VDDDBU	Tamper or Wakeup input	Input
44	PIOBU2	VDDDBU	Tamper or Wakeup input	Input
48	PIOBU3	VDDDBU	Tamper or Wakeup input	Input
47	PIOBU4	VDDDBU	Tamper or Wakeup input	Input
46	PIOBU5	VDDDBU	Tamper or Wakeup input	Input
59	PIOBU6	VDDDBU	Tamper or Wakeup input	Input
45	PIOBU7	VDDDBU	Tamper or Wakeup input	Input
32	RXD	VDDDBU	Low Power Asynchronous Receiver	Input
35	SHDN	VDDDBU	Shutdown Control	Output
49	WKUP	VDDDBU	Wakeup	Input
36	ETH_LED0	VDDIN_3V3	Status LED control for Ethernet ports	Output
37	ETH_RXM	± 2.5V	Physical receive or transmit signal (– differential)	I/O
38	ETH_RXP	± 2.5V	Physical receive or transmit signal (+ differential)	I/O
40	ETH_TXM	± 2.5V	Physical receive or transmit signal (– differential)	I/O
41	ETH_TXP	± 2.5V	Physical receive or transmit signal (+ differential)	I/O

**Table 4-6. System-On-Module Pin Description: Power**

Pin Number	PIO	Description	Comments
16,17	VDDIN_3V3	Main 3.3V Supply inputs. Used for Peripheral I/O lines and MIC2800-G1JJYML supplies.	–
55	VDDDBU	Input supply for Slow Clock Oscillator, internal 32 kHz RC Oscillator and a part of the System Controller	–
65	VDDSDHC	SDMMC I/O lines supply input	–
15	VDDISC	Image Sensor I/O lines supply input	For decoupling guidelines, refer to the section "Design Guidelines".

Figure 5-5. Internal System Control Schematic



## 5.4 Ethernet PHY

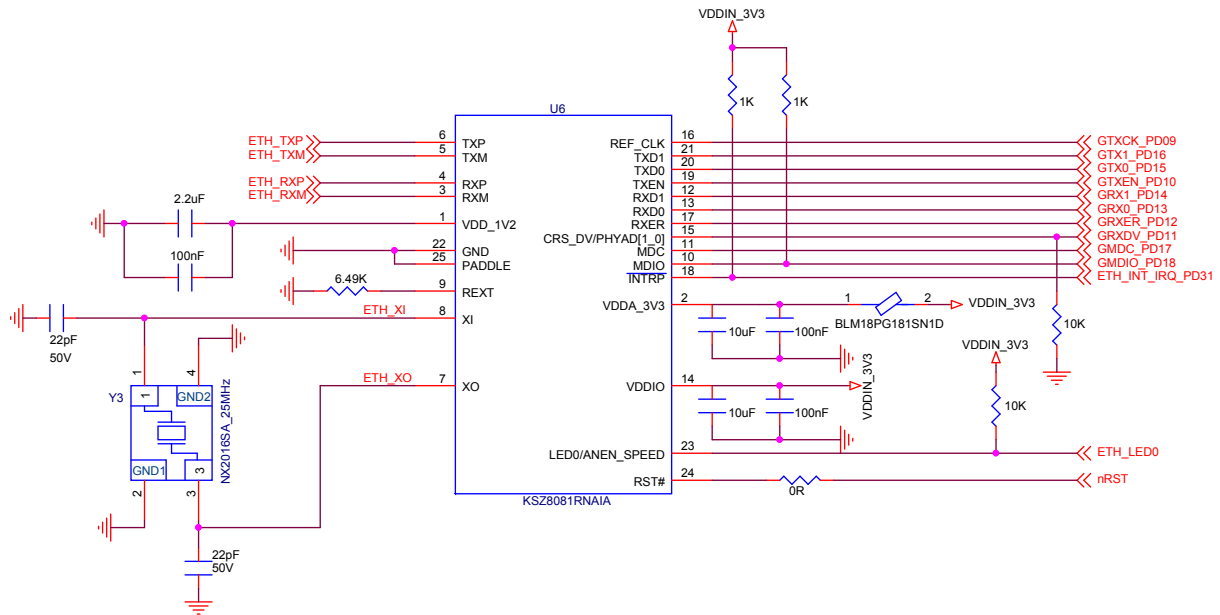
The Microchip SAMA5D27 SOM1 embeds a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors.

The KSZ8081RNAIA is available in 24-pin, lead-free QFN packages. For more information, refer to the [product web page](#).



**Figure 5-6. Ethernet PHY Schematic**



**Table 5-2. KSZ8081RNAIA External Crystal**

Item	Designation	Type	Manufacturer	Manufacturer Specification Number
Y3	25MHz Crystal	NX2016SA	NDK	EXS00A-CS10694

## 5.5 QSPI Memory

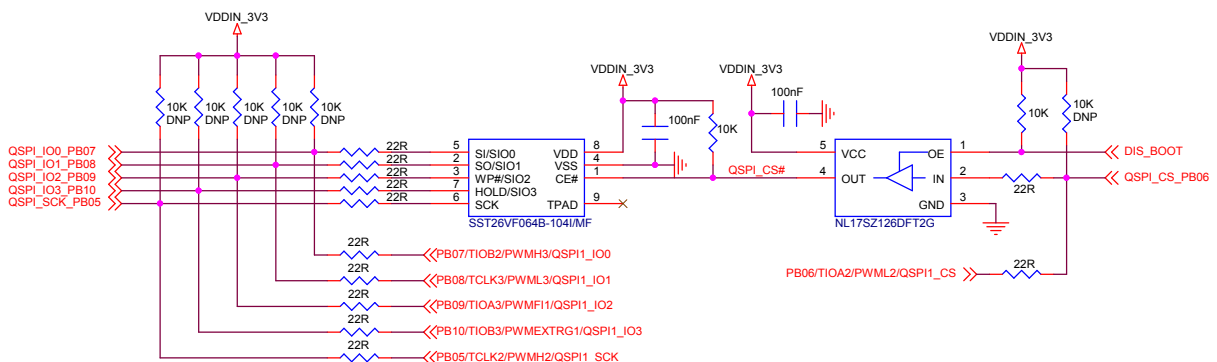
The SAMA5D27 SOM1 embeds the SST26VF064BT-104I/MF, a 64Mb Serial Quad I/O Flash memory.

The SST26VF064BT-104I/MF SQI features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

The SST26VF064BT-104I/MF is available in 8-lead WDFN package with 6mm × 5mm dimensions.

For more information, refer to the [product web page](#).

**Figure 5-7. QSPI Memory Schematic**





**Tip:** In case of non-use at application level of the QSPI embedded in SAMA5D27 SOM1, it is possible to reassign the signals dedicated to QSPI memory to another PIO function as defined in the table below. To do so, the DIS\_BOOT pin (SAMA5D27 SOM1 pad 126) must be forced to ground.

**Table 5-3. Other GPIO Possibilities for QSPI Interface in Case of Non-use**

Pin Number	Power Rail	Primary		PIO Peripheral				Reset State
		Signal	Dir	Func	Signal	Dir	IOset	
134	VDDIN_3V3	PB05	I/O	A	TCLK2	I	1	PIO, I, PU, ST
				C	PWMH2	O	1	
				D	QSPI1_SCK	O	2	
127	VDDIN_3V3	PB06	I/O	A	TIOA2	I/O	1	PIO, I, PU, ST
				C	PWML2	O	1	
				D	QSPI1_CS	O	2	
133	VDDIN_3V3	PB07	I/O	A	TIOB2	I/O	1	PIO, I, PU, ST
				C	PWMH3	O	1	
				D	QSPI1_IO0	I/O	2	
128	VDDIN_3V3	PB08	I/O	A	TCLK3	I	1	PIO, I, PU, ST
				C	PWML3	O	1	
				D	QSPI1_IO1	I/O	2	
132	VDDIN_3V3	PB09	I/O	A	TIOA3	I/O	1	PIO, I, PU, ST
				C	PWMF11	I	1	
				D	QSPI1_IO2	I/O	2	
135	VDDIN_3V3	PB10	I/O	A	TIOB3	I/O	1	PIO, I, PU, ST
				C	PWMEXTRG1	I	1	
				D	QSPI1_IO3	I/O	2	



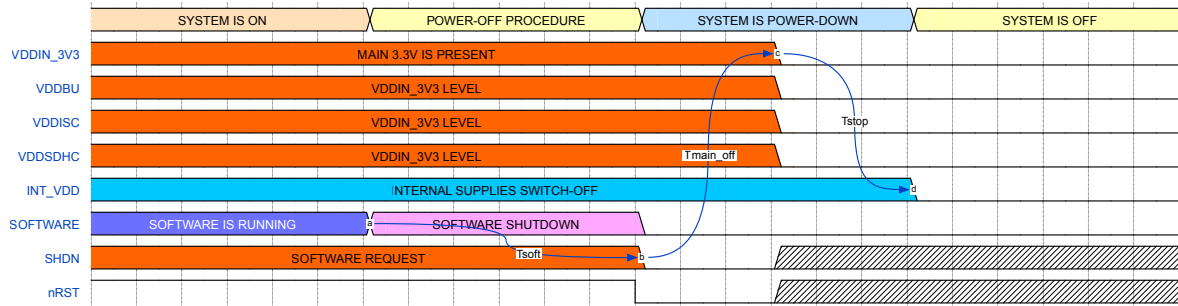
**Tip:** The QSPI interface can be shared with another external device. To do so, the QSPI\_CS# node must stay at "High" level. That means that the DIS\_BOOT pin (SAMA5D27 SOM1 pad 126) must be forced to ground.

## 5.6 EEPROM Memory

The SAMA5D27 SOM1 embeds the 24AA02E48T-I/OT, a 1Kb Serial EEPROM with pre-programmed EUI-48 MAC address.

The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. The second block is reserved for MAC Address storage.

**Figure 6-3. Power-Off Sequence Timing Diagram**



**Table 6-1. Timing Values**

Symbol	Description	Min.	Typ.	Max.	Unit
$t_{main}^{(1)}$	Main 3.3V Startup Time	–	–	1	ms
$t_{start}$	Internal Delay before starting System Core Supplies	1	–	3	ms
$t_{por}$	Power-On Reset Delay	–	10	11	ms
$t_{soft}$	Software Shutdown Time	Depending on system off time			ms
$t_{main\_off}$	Main 3.3V Power-off Time	–	–	1	ms
$t_{stop}$	Internal Delay before switching off System Core Supplies	1	–	3	ms

**Note:**

1. The three supplies VDDIN\_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than 800µs. VDDBU must be applied at the same time as VDDIN\_3V3 or just before. It is forbidden to apply VDDBU after VDDIN\_3V3.

## 6.2 Power Supply Configuration #2

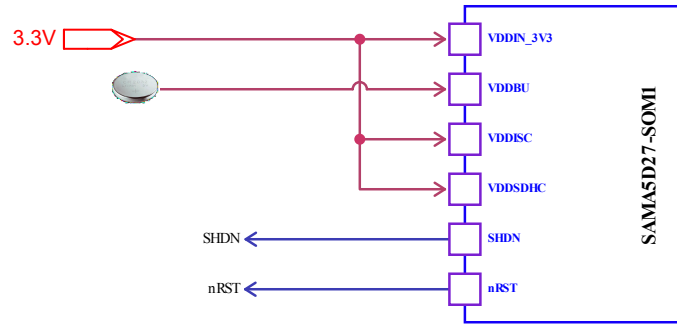
The SAMA5D27 SOM1 is supplied by different power supplies.

- Backup domain is connected to a coin-cell.
- The rest of the power inputs are connected to the main 3.3V supply.

In this configuration, the following PIOs have VDDBU Power Rail as reference. All other PIO have VDDIN\_3V3 Power Rail as reference.

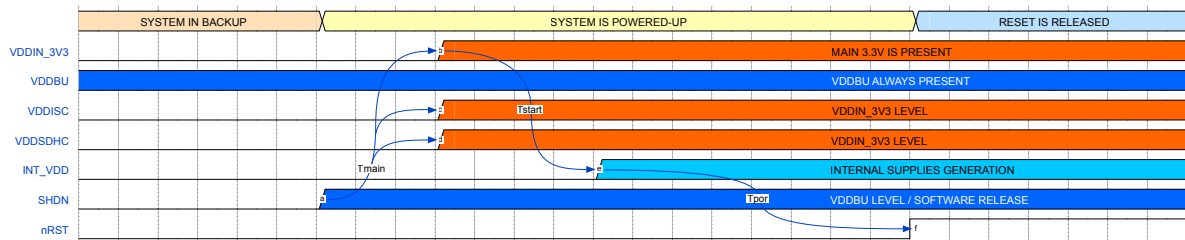
- COMPP and COMPN
- PIOBU1 to PIOBU7
- RXD, SHDN and WKUP

**Figure 6-4. Power Configuration #2**

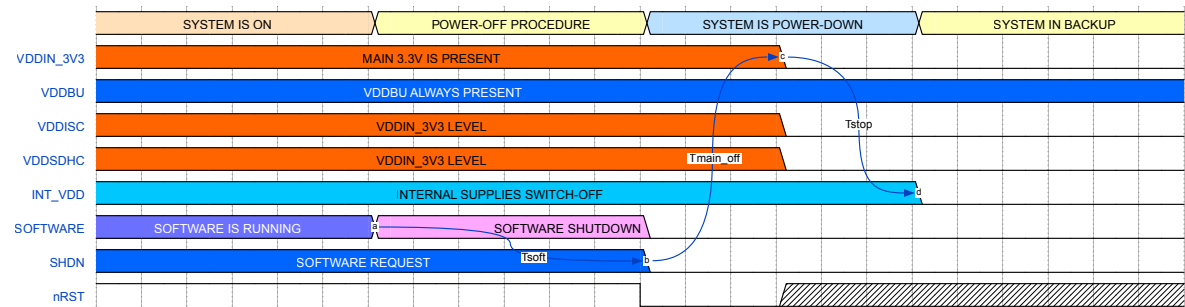


In this configuration, the two following timing sequences are applied.

**Figure 6-5. Power-On Sequence Timing Diagram**



**Figure 6-6. Power-Off Sequence Timing Diagram**



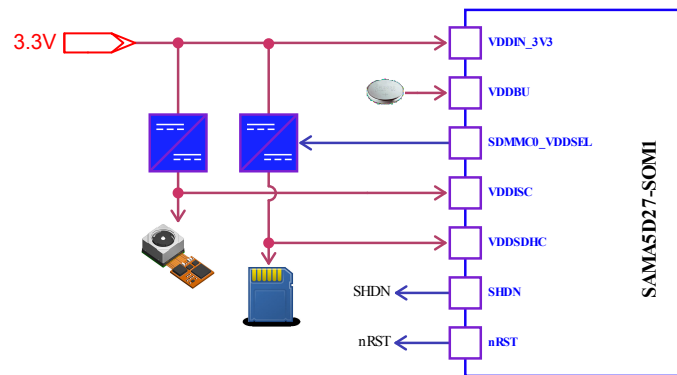
**Table 6-2. Timing Values**

Symbol	Description	Min.	Typ.	Max.	Unit
$t_{main}^{(1)}$	Main 3.3V Startup Time	–	–	1	ms
$t_{start}$	Internal Delay before starting System Core Supplies	1	–	3	ms
$t_{por}$	Power-On Reset Delay	–	10	11	ms
$t_{soft}$	Software Shutdown Time	Depending on system off time			ms
$t_{main\ off}$	Main 3.3V Power-off Time	–	–	1	ms
$t_{stop}$	Internal Delay before switching-off System Core Supplies	1	–	3	ms

**Note:**

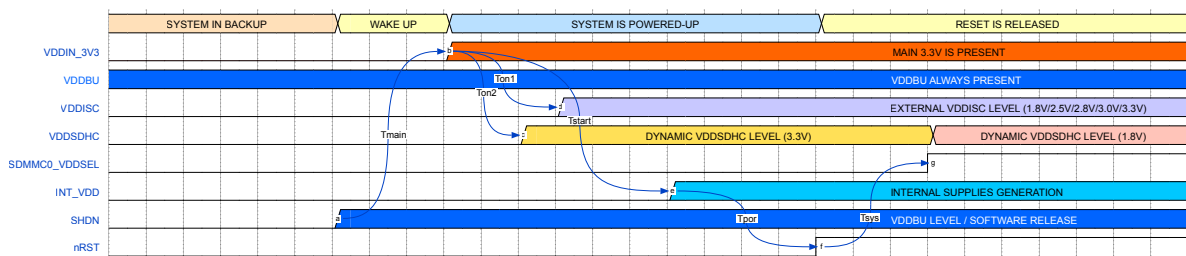
- VDDBU Power Rail as reference
  - COMPP and COMPN
  - PIOBU1 to PIOBU7
  - RXD, SHDN and WKUP
- VDDISC Power Rail as reference
  - PC09 to PC25
- VDDSDHC Power Rail as reference
  - PA00 to PA10
- All other PIOs have VDDIN\_3V3 Power Rail as reference.

**Figure 6-10. Power Configuration #4**

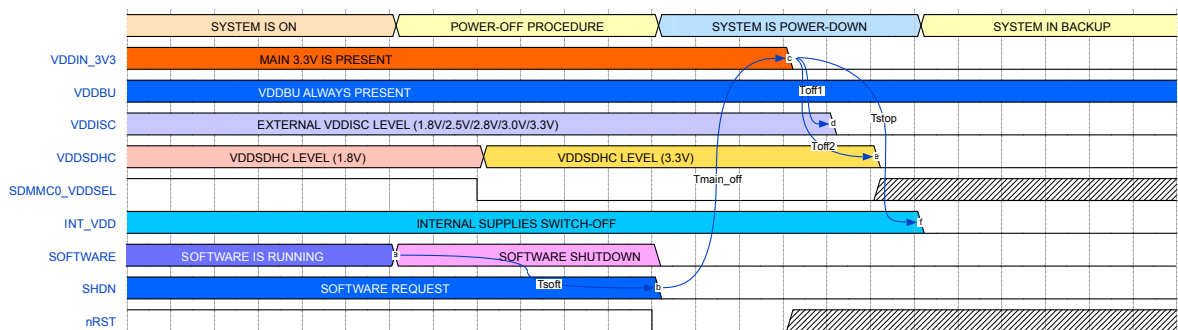


In this configuration mode, the two following timing sequences are applied.

**Figure 6-11. Power-On Sequence Timing Diagram**



**Figure 6-12. Power-Off Sequence Timing Diagram**



## 8. Debug Considerations

The SAMA5D27 SOM1 JTAG access is disabled during the execution of the ROM code sequence. It is re-enabled when jumping into SRAM when a valid code has been found on an external NVM, at the same time the ROM memory and fuses are hidden. If no valid boot is found on an external NVM, the ROM code

- enables the USB connection and one UART serial port
- starts the standard SAM-BA monitor
- locks access to the ROM memory
- re-enables the JTAG connection

The SAMA5D27 SOM1 has multiple debug and JTAG settings. For more information, refer to the SAMA5D2 datasheet, document no. DS60001476, "SECUMOD JTAG Protection Control Register", "Customer Fuse Matrix" and "Special Function Bits".

The JTAG I/O set can be configured. For correct operations, the I/O set to be used is JTAG\_IOSET\_3, i.e., the field JTAG\_IO\_SET in the Boot Configuration Word must be written with value '2'.<sup>(1)</sup>

**Note:** Due to IO conflict on line PA22, JTAG\_IOSET\_4 must not be implemented when SDMMC1 is used as an NVM boot media. See the SAMA5D2 datasheet, document no. DS60001476, "Boot Configuration Word".

Pad	Parameters	Conditions	Min.	Typ.	Max.
VDDSDHC	DC Supply	SDHC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA
VDDISC	DC Supply	ISC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA

## 9.3 DC Electrical Characteristics

### 9.3.1 Standard Interfaces

The following characteristics are applicable to the operating temperature range  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise specified.

**Table 9-3. DC Electrical Characteristics for GPIO Inputs**

Pad	Parameters	Conditions	Min.	Typ.	Max.
$V_{IL}$	Low-level Input Voltage	All GPIO @ 3.3V	-0.3V	–	0.4V
$V_{IH}$	High-level Input Voltage	All GPIO @ 3.3V	2.3V	–	3.6V
$V_{OL}$	Low-level Output Voltage	$I_O$ Max.	–	–	0.41V
$V_{OH}$	High-level Output Voltage	$I_O$ Max.	2.9V	–	--
$I_{IL}$	Low-level Input Current	All GPIO @ 3.3V	-1 $\mu$ A	–	1 $\mu$ A
$I_{IH}$	High-level Input Current	All GPIO @ 3.3V	-1 $\mu$ A	–	1 $\mu$ A
$I_{OL}$	Low-level Output Current	All GPIO @ 3.3V / Low	-2mA	–	--
		All GPIO @ 3.3V / High	-32mA	–	--
$I_{OH}$	High-level Output Current	All GPIO @ 3.3V / Low	–	–	2mA
		All GPIO @ 3.3V / High	–	–	32mA
$R_{PULLUP}$	Pull-up Resistors	All GPIO @ 3.3V and PDxx in AD mode.	280k $\Omega$	380k $\Omega$	480k $\Omega$
		All IOs in GPIO mode @3.3V.	40k $\Omega$	66k $\Omega$	130k $\Omega$
$R_{PULLDOWN}$	Pull-down Resistors	All GPIO @ 3.3V and PDxx in AD mode	280 k $\Omega$	380k $\Omega$	480k $\Omega$
		All IOs in GPIO mode @3.3V.	40k $\Omega$	77k $\Omega$	160k $\Omega$

**Note:** This table applies to all the following pads: PA0–PA31, PB0–PB31, PC0–PC31, PD0–PD8, PD19–PD30.

## 9.3.2 Other PIOs

The following characteristics are applicable to the operating temperature range  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise specified.

**Table 9-4. Table 7. DC Electrical Characteristics for System Inputs**

Pad	Parameters	Conditions	Min.	Typ.	Max.
$V_{IL}$	Low-level Input Voltage	DIS_BOOT	–	–	1.0V
$V_{IH}$	High-level Input Voltage	DIS_BOOT	2.3V	–	–

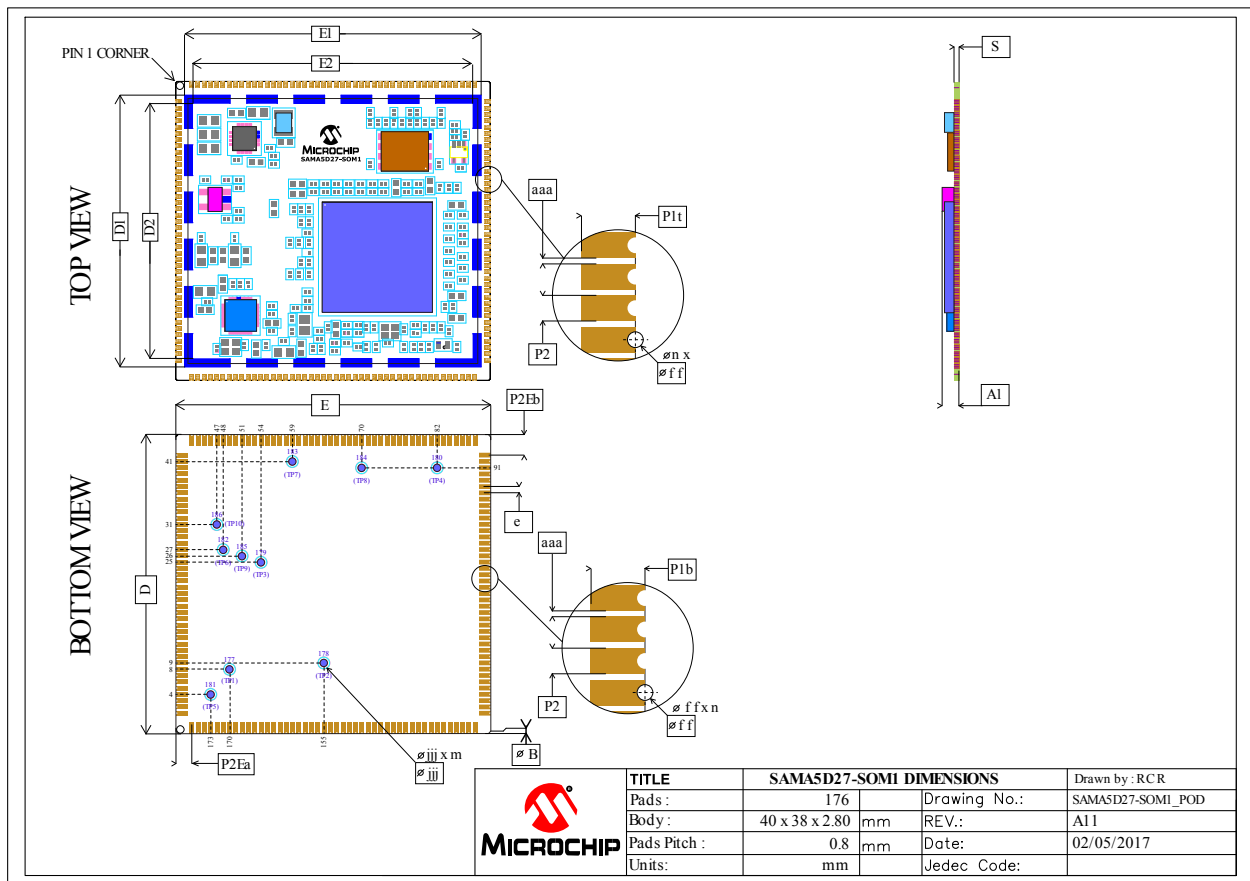


## 10. Mechanical Characteristics

### 10.1 Module Dimensions

The SAMA5D27 SOM1 has dimensions of 40mm x 38mm with the specific following mechanical characteristics.

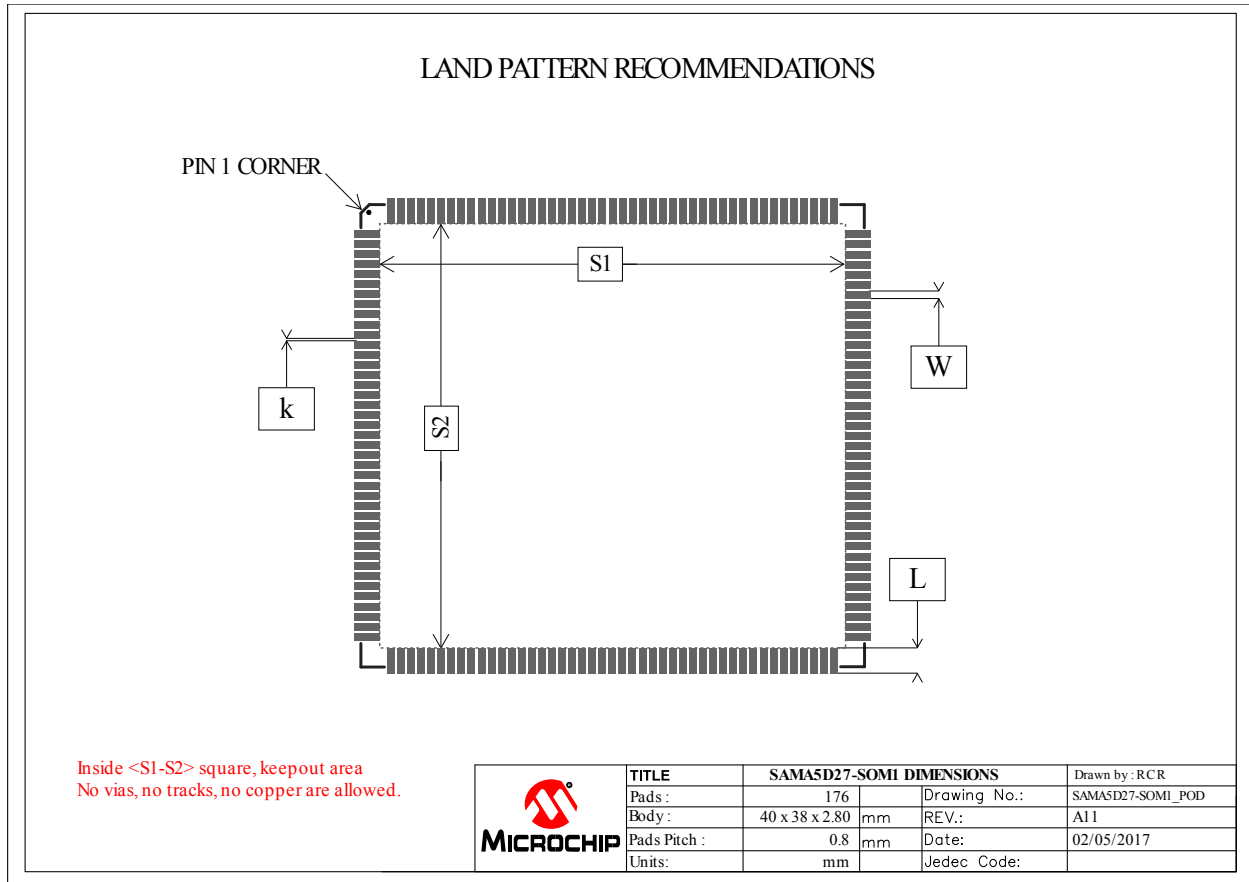
**Figure 10-1. System-On-Module Dimensions**



**Table 10-1. System-On-Module Dimensions**

	Symbol	Common Dimensions			Comments	
		Min.	Typ.	Max.		
Body Size	X	E	--	40.000	40.100	--
	Y	D	--	38.000	38.100	--
Pad Pitch	e	--	0.800	--	--	
PCB Thickness	S	1.150	1.200	1.250	--	
Total Thickness	A1	--	2.750	2.800	--	
PCB Angle Hole Diameter <sup>(1)</sup>	B	--	0.200	--	--	
Pad Length <sup>(1)</sup>	Bottom Side	P1b	--	1.500	--	

**Figure 10-2. System-On-Module Land Pattern**



**Table 10-2. System-On-Module Land Pattern Dimensions**

	Symbol	Common Dimensions			Comments
		Min.	Typ.	Max.	
Land Pattern Pad Width	W	–	0.600	–	Solder Mask Defined 0.550
Land Pattern Pad Length	L	–	2.000	–	–
Land Pattern Pad X Space	S1	–	37.000	–	–
Land Pattern Pad Y Space	S2	–	35.000	–	–
Land Pattern Pad Space	k	–	0.200	–	–

### 13. Revision History

Table 13-1. SAMA5D27 SOM1 Datasheet, Rev. DS60001521A, Oct-2017

Changes
First issue.

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