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Understanding Embedded - Microprocessors

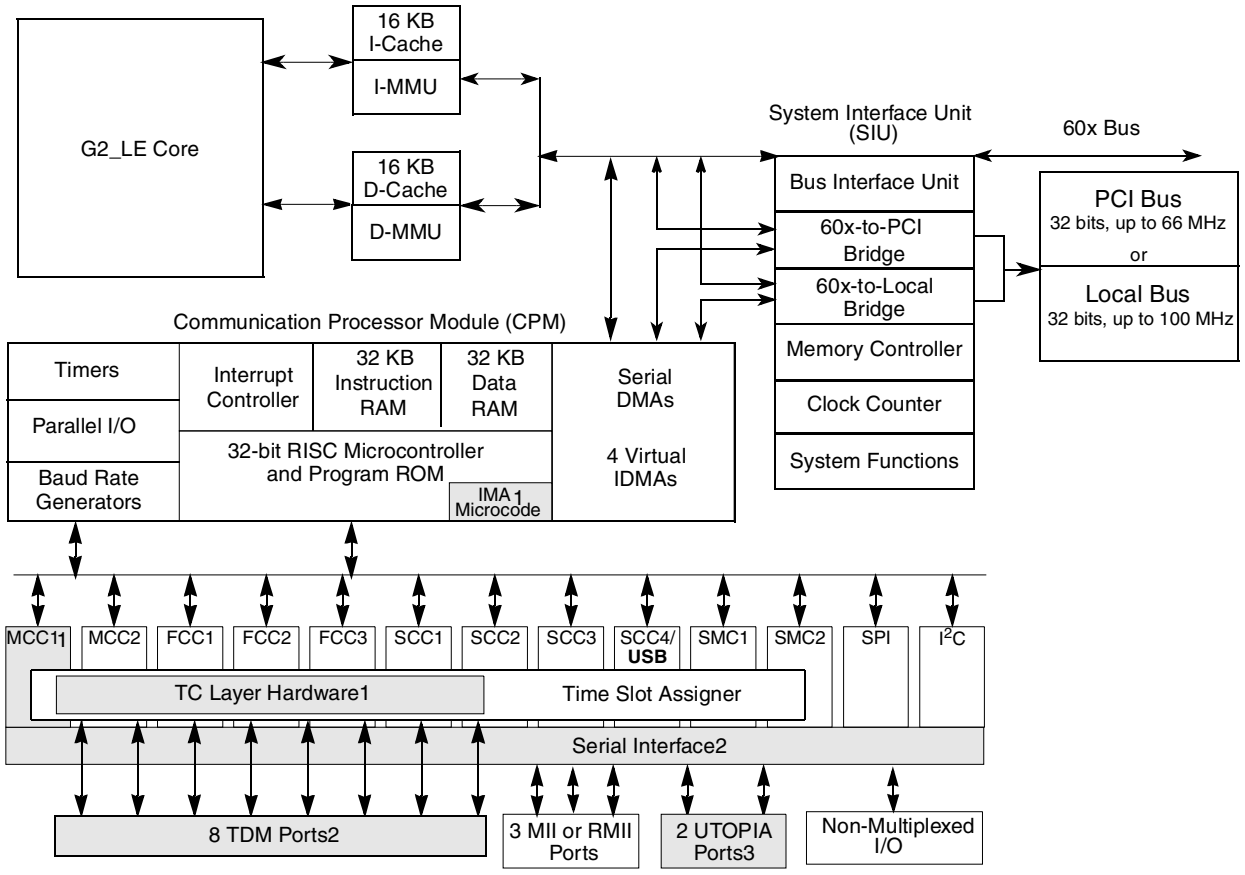
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	450MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8270cvvupea

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.



Notes:
[1] MPC8280 only (**not on MPC8270,** the VR package, nor the ZQ package)
[2] MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).
[3] MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270,** MPC8270VR, nor MPC8270ZQ)

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)

  - Common on-chip processor (COP) test interface
  - High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
  - Supports bus snooping
  - Support for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
  - PCI host bridge or peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI

Table 5. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 6.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/EXT_DBG3/IRQ5/CINT DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5/CINT CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/PCI_RSTINT_OUT/APE PORESET HRESET SRESET RSTCONF	V_{OL}	—	0.4	V

5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

Table 7. Estimated Power Dissipation for Various Configurations[1]

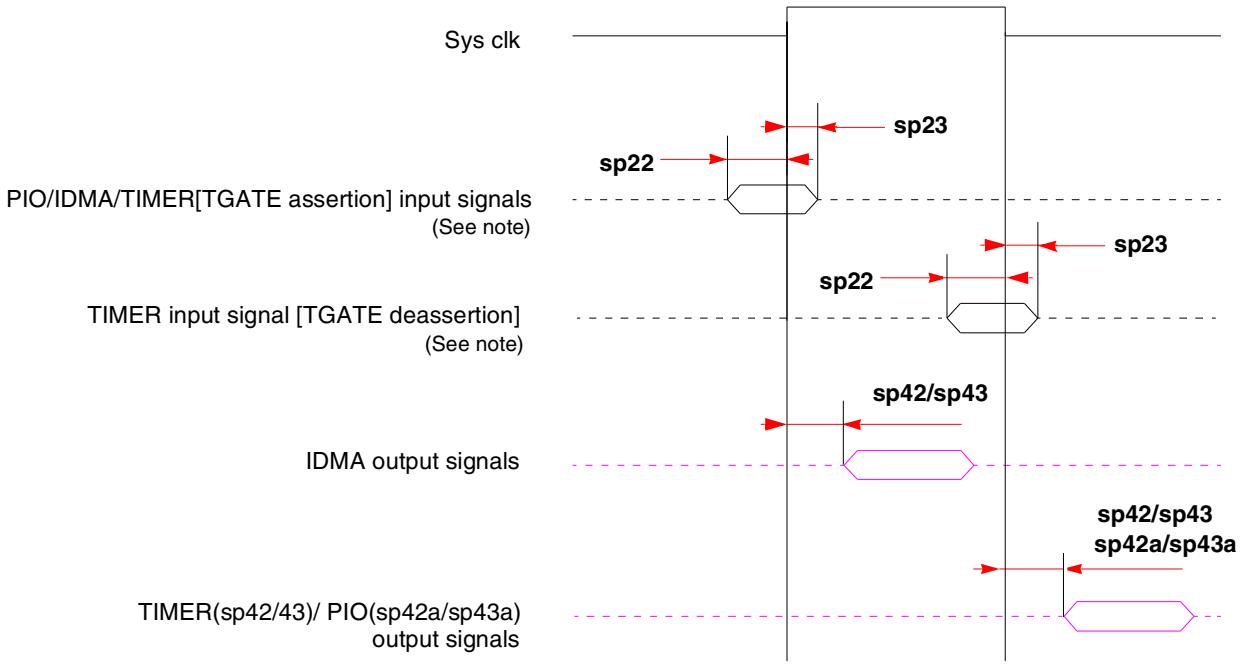
Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	P_{INT}(W)[2,3]	
					Vddl 1.5 Volts	
					Nominal	Maximum
66.67	2.5	166	3.5	233	0.95	1.0
66.67	2.5	166	4	266	1.0	1.05
66.67	3	200	4	266	1.05	1.1
66.67	3.5	233	4.5	300	1.05	1.15
83.33	3	250	4	333	1.25	1.35
83.33	3	250	4.5	375	1.3	1.4
83.33	3.5	292	5	417	1.45	1.55
100	3	300	4	400	1.5	1.6
100	3	300	4.5	450	1.55	1.65

1 Test temperature = 105° C

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

3 Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.45 W (nominal), 0.5 W (maximum)
83.3 MHz = 0.5W (nominal), 0.6 W (maximum)
100 MHz = 0.6 W (nominal), 0.7 W (maximum)

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/file time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

This figure shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

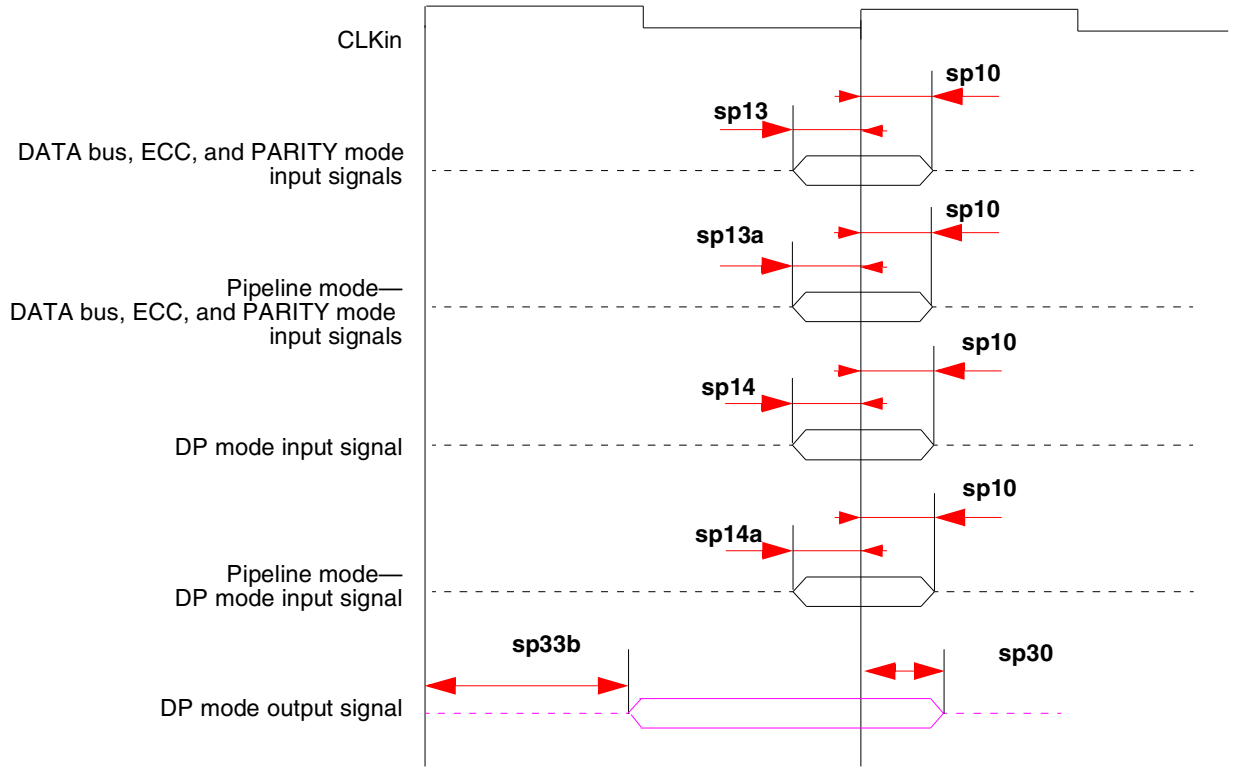


Figure 10. Parity Mode Diagram

This figure shows signal behavior in MEMC mode.

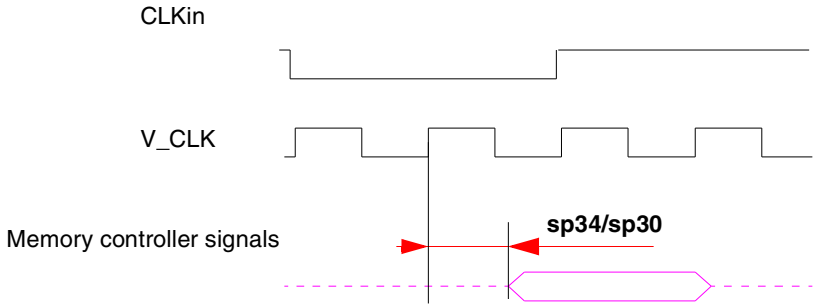


Figure 11. MEMC Mode Diagram

NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 15.

Table 15. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

This table is a representation of the information in Table 15.

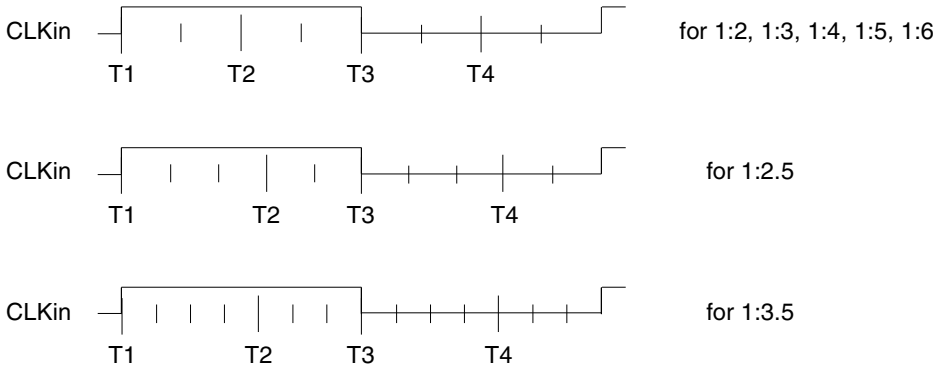


Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

6.3 JTAG Timings

This table lists the JTAG timings.

Table 16. JTAG Timings[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	 ns ns	 4, 7 4, 7

Table 17. SoC Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK[1]			
1	—	—	Local bus	—	Table 18
0	0	0	PCI host	50–66	Table 19
0	0	1		25–50	Table 20
0	1	0	PCI agent	50–66	Table 21
0	1	1		25–50	Table 22

[1] Determines PCI clock frequency range. See Section 7.2, "PCI Host Mode," and Section 7.3, "PCI Agent Mode."

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

7.1 Local Bus Mode

This table lists clock configurations for the SoC in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

Table 18. Clock Configurations for Local Bus Mode[1]

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
Default Modes (MODCK_H= 0000)								
0000_000	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0000_001	33.3	133.3	3	100.0	400.0	5	166.7	666.7
0000_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0000_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0000_100	60.0	167.0	2	120.0	334.0	2.5	150.0	417.5
0000_101	50.0	167.0	2	100.0	334.0	3	150.0	501.0
0000_110	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0000_111	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
Full Configuration Modes								
0001_000	50.0	167.0	2	100.0	334.0	4	200.0	668.0

Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0110_011	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7
0111_000	Reserved										
0111_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0111_010	50.0	66.7	3	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0111_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0111_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
1000_000	Reserved										
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7
1000_010	66.7	88.9	3	200.0	266.6	3.5	233.3	311.1	4	50.0	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200.0	266.6	3.5	200.0	266.6	4	50.0	66.7
1001_011	57.1	76.2	3.5	200.0	266.6	4	228.6	304.7	4	50.0	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0
1000_010	66.7	133.3	3	200.0	400.0	3.5	233.3	466.7	8	25.0	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	114.3	3.5	200.0	400.0	3.5	200.0	400.0	8	25.0	50.0
1001_011	57.1	114.3	3.5	200.0	400.0	4	228.6	457.1	8	25.0	50.0
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	42.9	85.7	3.5	150.0	300.0	5	214.3	428.6	6	25.0	50.0
1001_110	42.9	85.7	3.5	150.0	300.0	5.5	235.7	471.4	6	25.0	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As Table 17 shows, PCI_MODCK determines the PCI clock frequency range. See Table 20 for higher configurations.

3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

4 60x and local bus frequency. Identical to CLKIN.

5 CPM multiplication factor = CPM clock/bus clock

6 CPU multiplication factor = Core PLL multiplication factor

7.3 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI agent mode the following:

Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0	266.6	4.5	225.0	300.0	4	50.0	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7

This figure shows the pinout of the ZU and VV packages as viewed from the top surface.

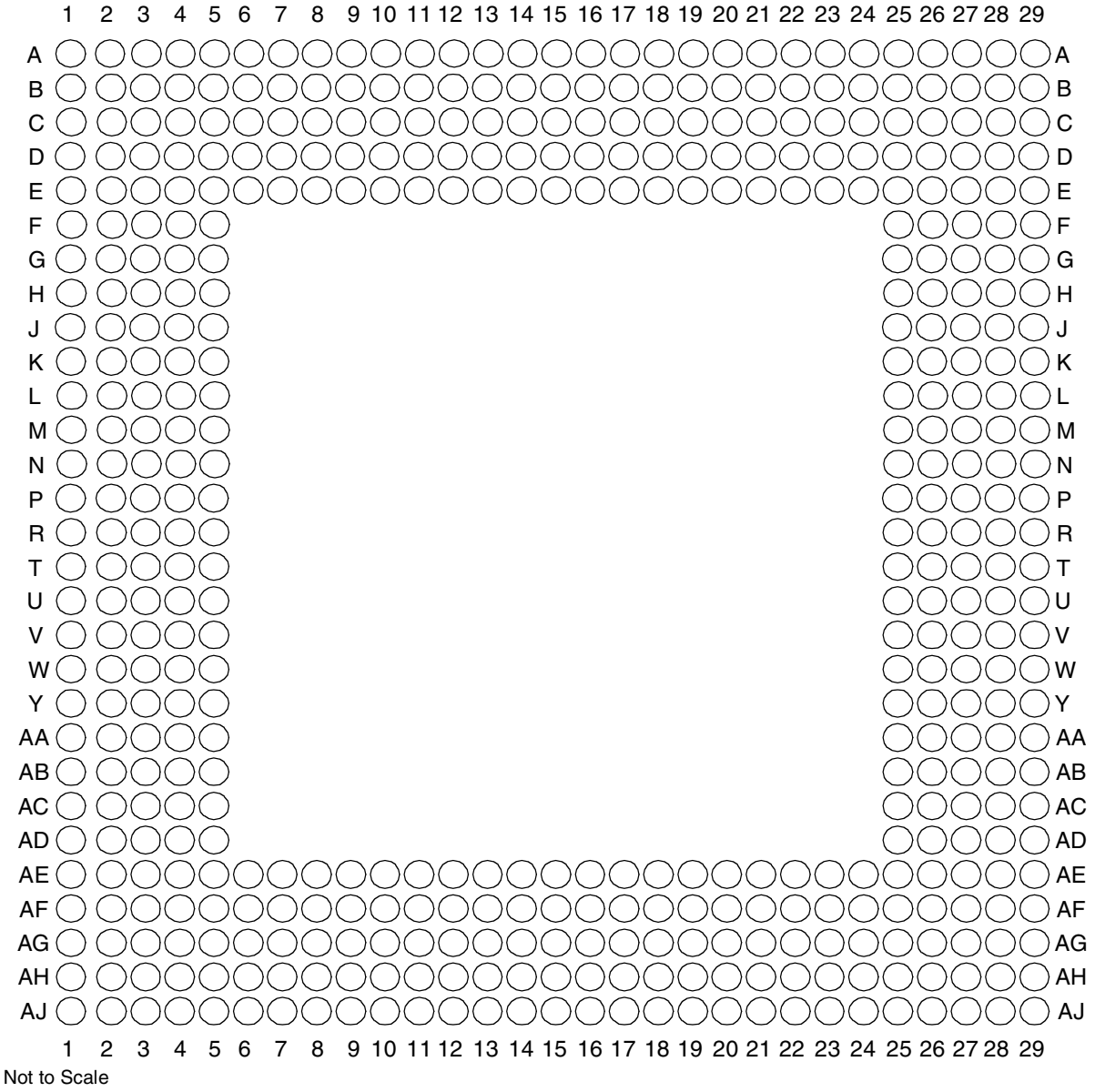


Figure 13. Pinout of the 480 TBGA Package (View from Top)

This table lists the pins of the MPC8280 and MPC8270, and Table 24 defines conventions and acronyms used in this table.

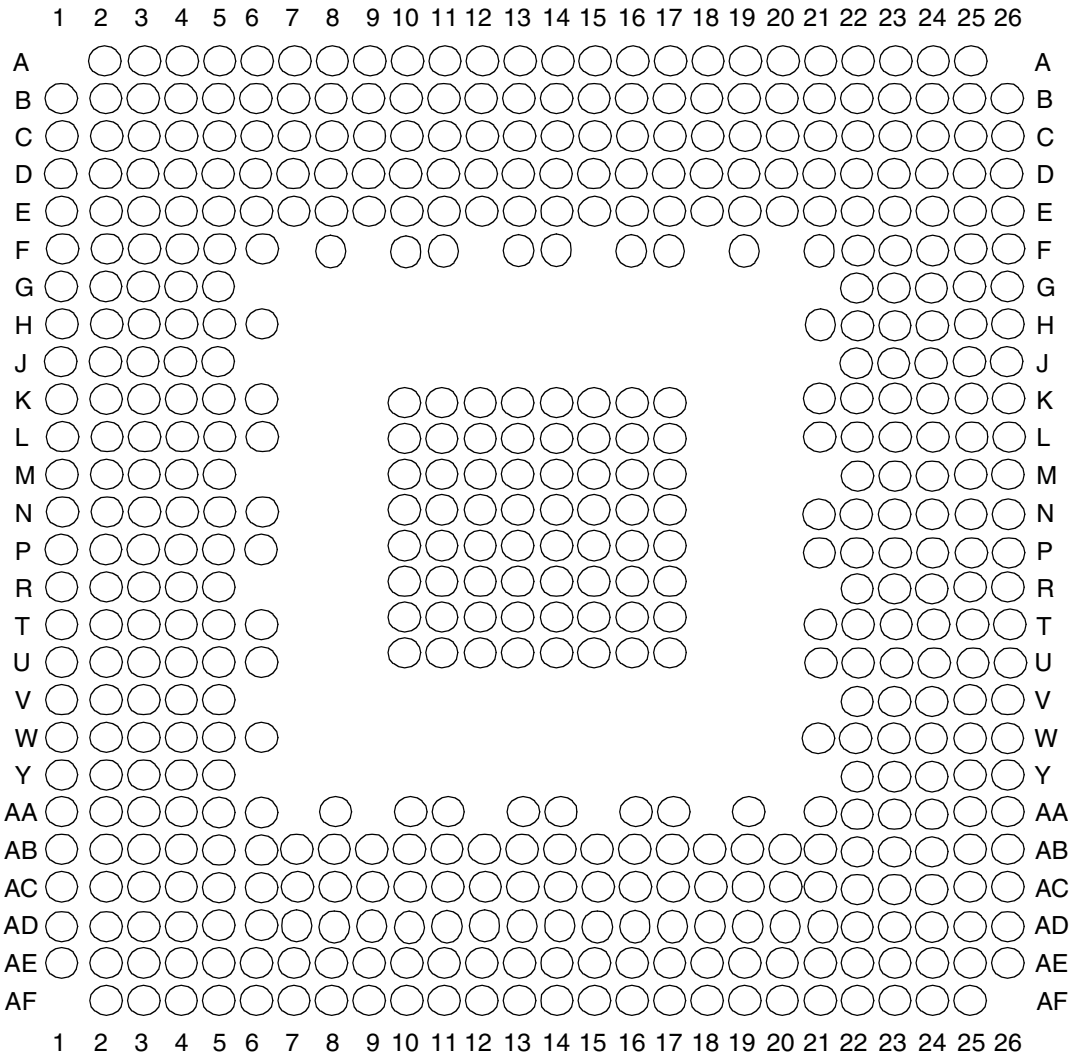
Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{BR}$		W5
$\overline{BG}$		F4

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
D51		C12
D52		B10
D53		A7
D54		C6
D55		D5
D56		B18
D57		B16
D58		E14
D59		D12
D60		C10
D61		E8
D62		D6
D63		C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$		B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$		A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$		E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$		D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$		C21
$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$		B21
$\overline{\text{IRQ6}}$/DP6/CSE0		A21
$\overline{\text{IRQ7}}$/DP7/CSE1		E20
$\overline{\text{PSDVAL}}$		V3
$\overline{\text{TA}}$		C22
$\overline{\text{TEA}}$		V5
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		U3
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$		Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		U4
$\overline{\text{CPU\_DBG}}$		R2
$\overline{\text{CPU\_BR}}$		Y3
$\overline{\text{CS0}}$		F25
$\overline{\text{CS1}}$		C29

This figure shows the pinout of the VR and ZQ packages as viewed from the top surface.



Not to Scale

Figure 14. Pinout of the 516 PBGA Package (View from Top)

This table shows the pinout list of the MPC8275 and MPC8270. Table 24 defines conventions and acronyms used in Table 25.

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
$\overline{\text{BR}}$		C16
$\overline{\text{BG}}$		D2
$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$		C1
$\overline{\text{TS}}$		D1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
TT1		B3
TT2		F8
TT3		A3
TT4		C3
$\overline{\text{TBST}}$		F5
TSIZ0		E3
TSIZ1		E2
TSIZ2		E1
TSIZ3		E4
$\overline{\text{AACK}}$		D3
$\overline{\text{ARTRY}}$		C2
$\overline{\text{DBG}}$		A14
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$		C15
D0		W4
D1		Y1
D2		V1
D3		P4
D4		N3
D5		K5
D6		J4
D7		G1
D8		AB1
D9		U4
D10		U2
D11		N6
D12		N1
D13		L1
D14		J5
D15		G3
D16		AA2
D17		W1
D18		T3
D19		T1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D20		M2
D21		K2
D22		J1
D23		G4
D24		U5
D25		T5
D26		P5
D27		P3
D28		M3
D29		K3
D30		H2
D31		G5
D32		AA1
D33		V2
D34		U1
D35		P2
D36		M4
D37		K4
D38		H3
D39		F2
D40		Y2
D41		U3
D42		T2
D43		N2
D44		M5
D45		K1
D46		H4
D47		F1
D48		W2
D49		T4
D50		R3
D51		N4
D52		M1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D53		J2
D54		H5
D55		F3
D56		V3
D57		R5
D58		R2
D59		N5
D60		L2
D61		J3
D62		H1
D63		F4
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$		AB3
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$		W5
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$		AC2
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$		AA3
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$		AD1
$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$		AC1
$\overline{\text{IRQ6}}$/DP6/CSE0		AB2
$\overline{\text{IRQ7}}$/DP7/CSE1		Y3
$\overline{\text{PSDVAL}}$		D15
$\overline{\text{TA}}$		Y4
$\overline{\text{TEA}}$		D16
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		E15
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		D14
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		E14
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$		A17
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		B14
$\overline{\text{CPU\_DBG}}$		F13
$\overline{\text{CPU\_BR}}$		B17
$\overline{\text{CS0}}$		AC6
$\overline{\text{CS1}}$		AD6
$\overline{\text{CS2}}$		AE6
$\overline{\text{CS3}}$		AB7

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.0	2/2004	• Removal of “Advance Information” and “Preliminary.” The MPC8280 is fully qualified. • Table 2: New • Figure 1: Modification to note 2 • Section 1.1: Core frequency range is 166–450 MHz • Addition of ZQ (516 PBGA with Lead spheres) package references • Table 4: VDD and VCCSYN modified to 1.45–1.60 V • Note following Table 4: Modified • Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5) • Table 5: Changed I_{OL} for 60x signals to 6.0 mA • Table 5: Moved QREQ to V_{OL}: I_{OL}= 3.2 mA • Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for V_{OL} (I_{OL} = 6.0mA) • Table 10: Addition of Ψ_{JT} and note 4 • Sections 4.1–4.5: New • Table 12: Modified power values (+ 150mW to each) • Table 14: Addition of note 2. Changed PCI impedance to 27 Ω. • Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41 • Table 20: Changes to sp16a, sp18a, sp20 and sp21 • Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle • Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz • Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2. • Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables. • Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6) • Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted. • Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted. • Table 23: Addition of note 5 to ‘No connect’ (AA1, AG4) • Addition of “Note: Temperature Reflow for the VR Package" on page 76 • Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25) • Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins: PA6—FCC2_UT_RXADDR3 PA7—FCC2_UT_TXADDR3 PA8—FCC2_UT_TXADDR4 PB14—RXD3 PC19—SPICLK PC22—FCC1_UT_TXPRTY PC28—FCC2_UT_RXADDR4 • Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1): PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28] • Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted. • Table 25: Addition of note 5 to ‘No connect’ (E17, C23)

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
0.3	6/2003	• Removal of notes stating “no local bus” on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support. • References to “G2 core” changed to “G2_LE core.” See the *G2 Core Reference Manual* (G2CORERM/D). • Addition of VCCSYN to “Note” below Table 4, and to note 3 of Table 5 • Figure 2: New • Table 5: Addition of note 1 • Table 10: Addition of θ_{JB} and θ_{JC}. Modifications to ZU package values. • Table 12: Addition of various configurations, Modification of values. Addition of note 3. • Table 9: Addition of 66 MHZ and 100 MHz values. Addition of sp42a/sp43a. • Table 20: Addition of 66 MHZ and 100 MHz values • Table 12: sp30 values. sp33b @100 MHz value. Removal of previous note 2. Modification of current note 2. • Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes • Section 6.2: Addition of note on PCI timing • Table 18, Table 32, Table 33, Table 36, Table 37: Addition of note 1 concerning minimum operating frequencies • Addition of statement before clock tables about selection of clock configuration and input frequency • Table 23 and Table 25: Addition of note 1 to CPM pins
0.2	11/2002	Table 25, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 63)
0.1	—	Initial public release