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Understanding Embedded - Microprocessors

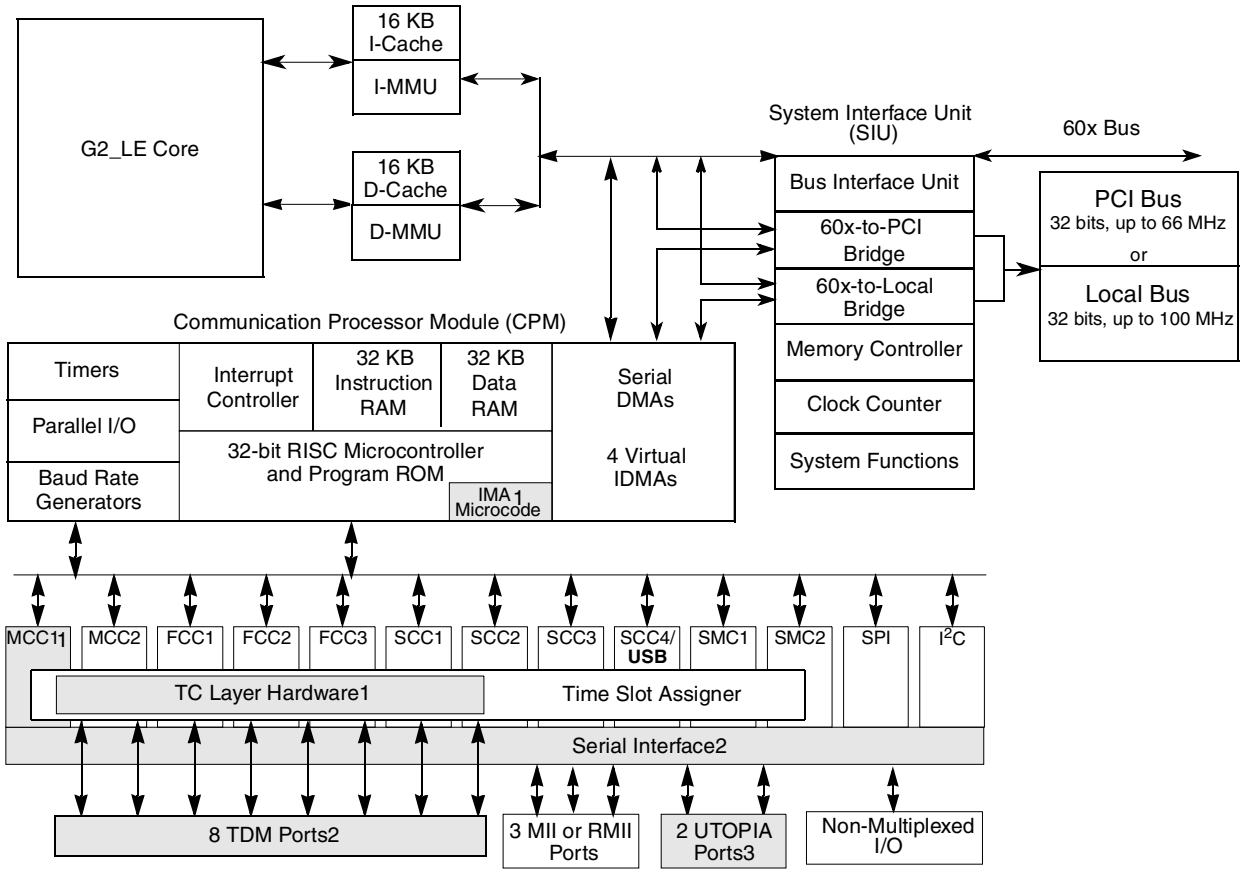
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8270czuqlda

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.



Notes:
[1] MPC8280 only (**not on MPC8270,** the VR package, nor the ZQ package)
[2] MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).
[3] MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270,** MPC8270VR, nor MPC8270ZQ)

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)

Table 5. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE[0–7]/PSDDQM[0–7]/PBS[0–7] PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3] LSDA10/LGPL0/PCI_MODCKH0 LSDWE/LGPL1/PCI_MODCKH1 LOE/LSDRAS/LGPL2/PCI_MODCKH2 LSDCAS/LGPL3/PCI_MODCKH3 LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK LWR MODCK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2]	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR L_A15/FRAME/SMI L_A16/TRDY L_A17/IRDY/CKSTP_OUT L_A18/STOP L_A19/DEVSEL L_A20/IDSEL L_A21/PERR L_A22/SERR L_A23/REQ0 L_A24/REQ1/HSEJSW L_A25/GNT0 L_A26/GNT1/HSLED L_A27/GNT2/HSENUM L_A28/RST/CORE_SRESET L_A29/INTAL_A30/REQ2 L_A31 LCL_D[0-31)]/AD[0-31] LCL_DP[03]/C/BE[0-3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO QREQ				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, either pull unused pins to GND or VDDH or configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

Table 7. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	P_{INT}(W)[2,3]	
					Vddl 1.5 Volts	
					Nominal	Maximum
66.67	2.5	166	3.5	233	0.95	1.0
66.67	2.5	166	4	266	1.0	1.05
66.67	3	200	4	266	1.05	1.1
66.67	3.5	233	4.5	300	1.05	1.15
83.33	3	250	4	333	1.25	1.35
83.33	3	250	4.5	375	1.3	1.4
83.33	3.5	292	5	417	1.45	1.55
100	3	300	4	400	1.5	1.6
100	3	300	4.5	450	1.55	1.65

1 Test temperature = 105° C

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

3 Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.45 W (nominal), 0.5 W (maximum)
83.3 MHz = 0.5W (nominal), 0.6 W (maximum)
100 MHz = 0.6 W (nominal), 0.7 W (maximum)

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 10. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	2	2	2
sp20	sp21	TDM inputs/SI	5	5	5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	0.5	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

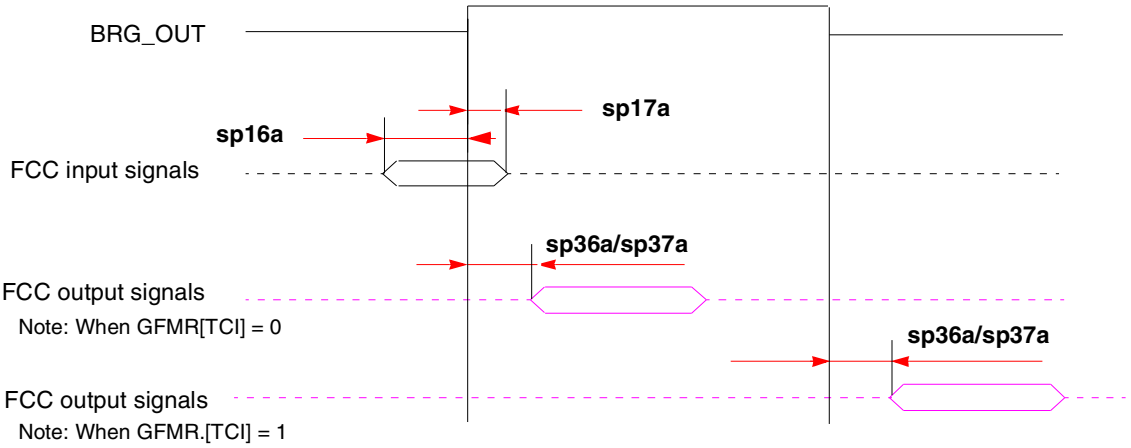
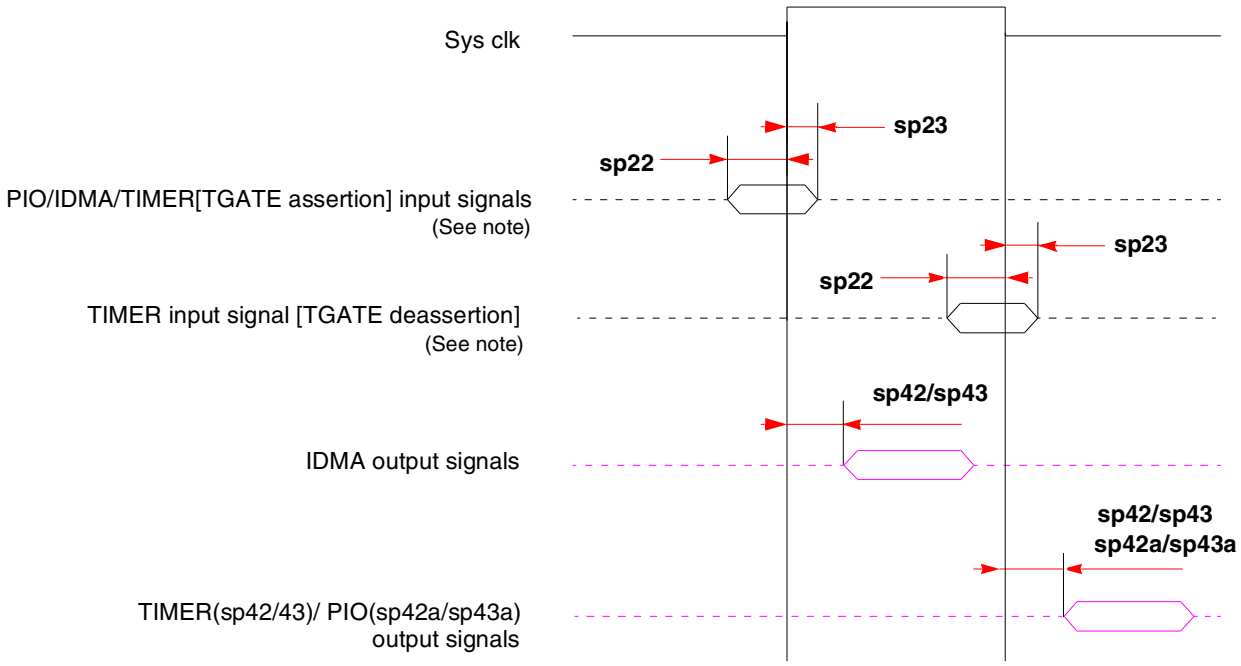


Figure 3. FCC Internal Clock Diagram

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/file time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	25.0	50.0	5	125.0	250.0	3.5	218.8	437.5	2	62.5	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev 0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
$\overline{\text{TBST}}$		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
$\overline{\text{AACK}}$		F3
$\overline{\text{ARTRY}}$		E1
$\overline{\text{DBG}}$		V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4
D16		D19
D17		D17

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
D51		C12
D52		B10
D53		A7
D54		C6
D55		D5
D56		B18
D57		B16
D58		E14
D59		D12
D60		C10
D61		E8
D62		D6
D63		C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$		B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$		A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$		E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$		D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$		C21
$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$		B21
$\overline{\text{IRQ6}}$/DP6/CSE0		A21
$\overline{\text{IRQ7}}$/DP7/CSE1		E20
$\overline{\text{PSDVAL}}$		V3
$\overline{\text{TA}}$		C22
$\overline{\text{TEA}}$		V5
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		U3
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$		Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		U4
$\overline{\text{CPU\_DBG}}$		R2
$\overline{\text{CPU\_BR}}$		Y3
$\overline{\text{CS0}}$		F25
$\overline{\text{CS1}}$		C29

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
CS2		E27
CS3		E28
CS4		F26
CS5		F27
CS6		F28
CS7		G25
CS8		D29
CS9		E29
CS10/BCTL1		F29
CS11/AP0		G28
BADDR27		T5
BADDR28		U1
ALE		T2
BCTL0		A27
PWE0/PSDDQM0/PBS0		C25
PWE1/PSDDQM1/PBS1		E24
PWE2/PSDDQM2/PBS2		D24
PWE3/PSDDQM3/PBS3		C24
PWE4/PSDDQM4/PBS4		B26
PWE5/PSDDQM5/PBS5		A26
PWE6/PSDDQM6/PBS6		B25
PWE7/PSDDQM7/PBS7		A25
PSDA10/PGPL0		E23
PSDWE/PGPL1		B24
POE/PSDRAS/PGPL2		A24
PSDCAS/PGPL3		B23
PGTA/PUPMWAIT/PGPL4/PPBS		A23
PSDAMUX/PGPL5		D22
LWE0/LSDDQM0/LBS0/PCI_CFG0		H28
LWE1/LSDDQM1/LBS1/PCI_CFG1		H27
LWE2/LSDDQM2/LBS2/PCI_CFG2		H26
LWE3/LSDDQM3/LBS3/PCI_CFG3		G29
LSDA10/LGPL0/PCI_MODCKH0		D27

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCCI_RMII_RXD0	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	AE16[2]
PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT8_TXD7/FCC1_UT16_TXD15	AJ16[2]
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	AG15[2]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	AJ13[2]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	AE13[2]
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12[2]
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11[2]
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	AH9[2]
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	AJ8[2]
PA26/FCC1_RMII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	AH7[2]
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	AF7[2]
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	$\overline{\text{FCC1\_UTM\_RXENB}}$/ $\overline{\text{FCC1\_UTS\_RXENB}}$	AD5[2]
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	AF1[2]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	AD3[2]
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UTM\_TXENB}}$/ $\overline{\text{FCC1\_UTS\_TXENB}}$	AB5[2]
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	FCC2_UT8_RXD0	AD28[2]
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD26[2]
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AD25[2]
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26[2]
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3/L1RSYNCD1	AH27[2]
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2/L1TSYNCD1/ L1GNTD1	AG24[2]

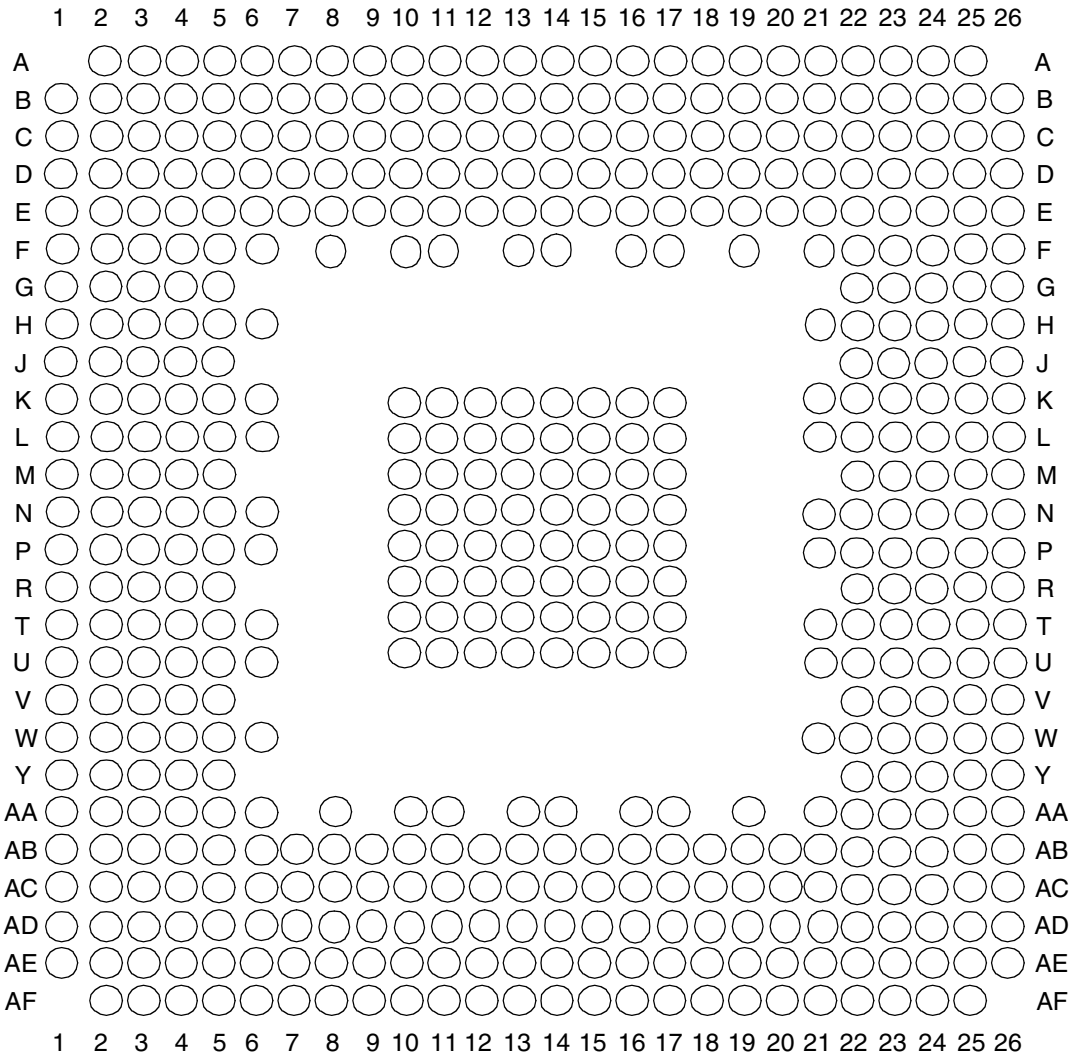
Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/TXD2	L1CLKOB1/L1RSYNCC1	AG22[2]
PB13/FCC3_MII_COL/L1TXD1A2	$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1	AH21[2]
PB14/FCC3_MII_RMII_TX_EN//RXD3	L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19[2]
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18[2]
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV	L1RQA1	AJ17[2]
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14[2]
PB19FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13[2]
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12[2]
PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11[2]
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16[2]
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15[2]
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9[2]
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7[2]
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6[2]
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1		AE3[2]
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2[2]
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5[2]
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4[2]

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	AF9[2]
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	AE8[2]
PC26/CLK6/TOUT3/TMCLK		AJ6[2]
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		AG2[2]
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2/ FCC2_RXADDR4		AF3[2]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		AF2[2]
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	AE1[2]
PC31/CLK1/BRGO1		AD1[2]
PD4/BRGO8/FCC3_RTS/SMRXD2	L1TSYNCD1/L1GNTD1	AC28[2]
PD5/DONE1	FCC1_UT16_TXD3	AD27[2]
PD6/DACK1	FCC1_UT16_TXD4	AF29[2]
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AF28[2]
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AG25[2]
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	AH26[2]
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AJ27[2]
PD11/L1RQB2	FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1	AJ23[2]
PD12	SI1_L1ST2/L1RXDB1	AG23[2]
PD13	SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	AE20[2]
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	AJ20[2]
PD16/SPIMISO	FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1	AG18[2]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	AG17[2]
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	AF16[2]
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	AH15[2]

This figure shows the pinout of the VR and ZQ packages as viewed from the top surface.



Not to Scale

Figure 14. Pinout of the 516 PBGA Package (View from Top)

This table shows the pinout list of the MPC8275 and MPC8270. Table 24 defines conventions and acronyms used in Table 25.

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
$\overline{\text{BR}}$		C16
$\overline{\text{BG}}$		D2
$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$		C1
$\overline{\text{TS}}$		D1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
CS4		AF7
CS5		AC7
CS6		AD7
CS7		AF8
CS8		AE8
CS9		AD8
CS10/BCTL1		AC8
CS11/AP0		AB8
BADDR27		C13
BADDR28		A12
ALE		D13
BCTL0		AF4
PWE0/PSDDQM0/PBS0		AA5
PWE1/PSDDQM1/PBS1		AE4
PWE2/PSDDQM2/PBS2		AD4
PWE3/PSDDQM3/PBS3		AF3
PWE4/PSDDQM4/PBS4		AB4
PWE5/PSDDQM5/PBS5		AE3
PWE6/PSDDQM6/PBS6		AF2
PWE7/PSDDQM7/PBS7		AD3
PSDA10/PGPL0		AE2
PSDWE/PGPL1		AD2
POE/PSDRAS/PGPL2		AE1
PSDCAS/PGPL3		AC3
PGTA/PUPMWAIT/PGPL4/PPBS		W6
PSDAMUX/PGPL5		AA4
LWE0/LSDDQM0/LBS0/PCI_CFG0		AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1		AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2		AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3		AF9
LSDA10/LGPL0/PCI_MODCKH0		AB6
LSDWE/LGPL1/PCI_MODCKH1		AF5
LOE/LSDRAS/LGPL2/PCI_MODCKH2		AE5

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PORESET[2]		B25
HRESET		D24
SRESET		E23
QREQ		D18
RSTCONF		E24
MODCK1/AP1/TC0/BNKSEL0		B16
MODCK2/AP2/TC1/BNKSEL1		F16
MODCK3/AP3/TC2/BNKSEL2		A15
CLKIN1		G22
PA0/RESTART1/DREQ3	FCC2_UTM_TXADDR2	AC20[2]
PA1/REJECT1/DONE3	FCC2_UTM_TXADDR1	AC21[2]
PA2/CLK20/DACK3	FCC2_UTM_TXADDR0	AF25[2]
PA3/CLK19/DACK4/L1RXD1A2	FCC2_UTM_RXADDR0	AE24[2]
PA4/REJECT2/DONE4	FCC2_UTM_RXADDR1	AA21[2]
PA5/RESTART2/DREQ4	FCC2_UTM_RXADDR2	AD25[2]
PA6	FCC2_UT_RXADDR3	AC24[2]
PA7/SMSYN2	FCC2_UT_TXADDR3	AA22[2]
PA8/SMRXD2	FCC2_UT_TXADDR4	AA23[2]
PA9/SMTXD2		Y26[2]
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	W22[2]
PA11/MSNUM4	FCC1_UT8_RXD1/FCC1_UT16_RXD9	W23[2]
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	V26[2]
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	V25[2]
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	T22[2]
PA15/FCC1_MII_HDLC_RXD2	/FCC1_UT8_RXD5/ FCC1_UT16_RXD13	T25[2]
PA16/FCC1_MII_HDLC_RXD1/ FCC1_RMII_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	R24[2]
PA17/FCC_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCCI_RMII_RXD0	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	P22[2]
PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT8_TXD7/FCC1_UT16_TXD15	N26[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23[2]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26[2]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23[2]
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23[2]
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26[2]
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25[2]
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26[2]
PA26/FCC1_MII_RMII_RX_ER/	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25[2]
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	C25[2]
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	$\overline{\text{FCC1\_UTM\_RXENB}}$/ $\overline{\text{FCC1\_UTS\_RXENB}}$	C22[2]
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21[2]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20[2]
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UTM\_TXENB}}$/ $\overline{\text{FCC1\_UTS\_TXENB}}$	A19[2]
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	FCC2_UT8_RXD0	AD21[2]
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD22[2]
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22[2]
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26[2]
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23[2]
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26[2]
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25[2]
PB12/FCC3_MII_CRS/TXD2		W26[2]
PB13/FCC3_MII_COL/L1TXD1A2		W25[2]
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24[2]

3 Must be pulled down or left floating.
4 If PCI is not desired, must be pulled up or left floating.
5 Sphere is not connected to die.
6 GNDSYN (B18): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8275/MPC8270. New designs must connect B18 to GND and follow the suggestions in Section 4.6, "Layout Practices." Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.
7 XFC (A18) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8275/MPC8270 because there is no need for external capacitor to operate the PLL. New designs should connect A18 (XFC) pin to GND. Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to the current capacitor.

9 Package Description

This figure shows the side profile of the TBGA package to indicate the direction of the top surface view.

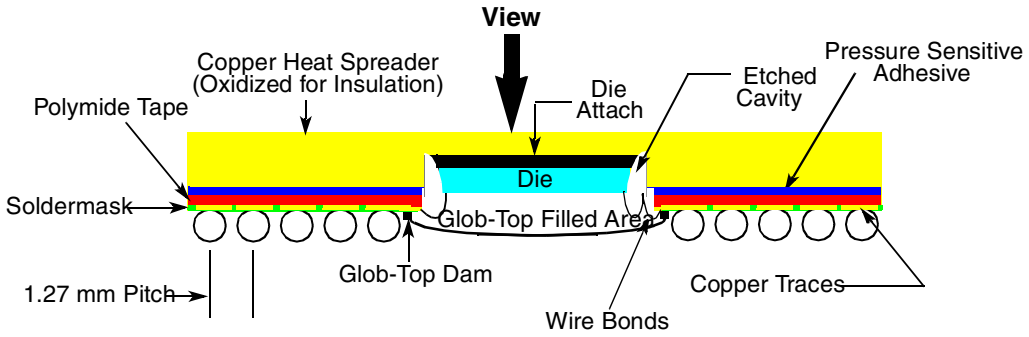


Figure 15. Side View of the TBGA Package

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

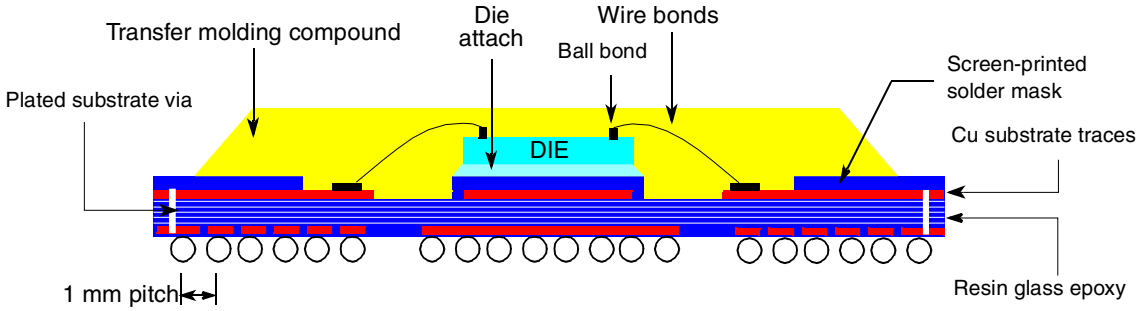


Figure 16. Side View of the PBGA Package Remove

9.1 Package Parameters

This table provides package parameters.

NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

Table 26. Package Parameters

Package	SoCs	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8280 MPC8270	37.5 × 37.5	TBGA	480	1.27	1.55
VV	MPC8280 MPC8270	37.5 × 37.5	TBGA	480	1.27	1.55
VR	MPC8275VR MPC8270VR	27 × 27	PBGA	516	1	2.25
ZQ	MPC8275ZQ MPC8270ZQ	27 × 27	PBGA	516	1	2.25

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.0	2/2004	• Removal of “Advance Information” and “Preliminary.” The MPC8280 is fully qualified. • Table 2: New • Figure 1: Modification to note 2 • Section 1.1: Core frequency range is 166–450 MHz • Addition of ZQ (516 PBGA with Lead spheres) package references • Table 4: VDD and VCCSYN modified to 1.45–1.60 V • Note following Table 4: Modified • Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5) • Table 5: Changed I_{OL} for 60x signals to 6.0 mA • Table 5: Moved QREQ to V_{OL}: I_{OL}= 3.2 mA • Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for V_{OL} (I_{OL} = 6.0mA) • Table 10: Addition of Ψ_{JT} and note 4 • Sections 4.1–4.5: New • Table 12: Modified power values (+ 150mW to each) • Table 14: Addition of note 2. Changed PCI impedance to 27 Ω. • Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41 • Table 20: Changes to sp16a, sp18a, sp20 and sp21 • Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle • Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz • Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2. • Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables. • Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6) • Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted. • Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted. • Table 23: Addition of note 5 to ‘No connect’ (AA1, AG4) • Addition of “Note: Temperature Reflow for the VR Package" on page 76 • Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25) • Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins: PA6—FCC2_UT_RXADDR3 PA7—FCC2_UT_TXADDR3 PA8—FCC2_UT_TXADDR4 PB14—RXD3 PC19—SPICLK PC22—FCC1_UT_TXPRTY PC28—FCC2_UT_RXADDR4 • Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1): PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28] • Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted. • Table 25: Addition of note 5 to ‘No connect’ (E17, C23)