Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8270vrmiba

1 Overview

This table shows the functionality supported by each SoC in the MPC8280 family.

Table 1. MPC8280 PowerQUICC II Family Functionality

Functionality	SoCs			
	MPC8270		MPC8275	MPC8280
Package[1]	480 TBGA	516 PBGA	516 PBGA	480 TBGA
Serial communications controllers (SCCs)	4	4	4	4
QUICC multi-channel controller (QMC)	—	—	—	—
Fast communication controllers (FCCs)	3	3	3	3
I-Cache (Kbyte)	16	16	16	16
D-Cache (Kbyte)	16	16	16	16
Ethernet (10/100)	3	3	3	3
UTOPIA II Ports	0	0	2	2
Multi-channel controllers (MCCs)	1	1	1	2
PCI bridge	Yes	Yes	Yes	Yes
Transmission convergence (TC) layer	—	—	—	Yes
Inverse multiplexing for ATM (IMA)	—	—	—	Yes
Universal serial bus (USB) 2.0 full/low rate	1	1	1	1
Security engine (SEC)	—	—	—	—

[1] See Table 2.

Devices in the MPC8280 family are available in four packages—the standard ZU and VV packages and the alternate VR or ZQ packages—as shown in Table 2. Note that throughout this document, references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Freescale sales office. For package ordering information, see Section 10, “Ordering Information.”

Table 2. HiP7 PowerQUICC II Device Packages

Code (Package)	ZU (480 TBGA—Leaded)	VV (480 TBGA—Lead Free)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8280	MPC8280	MPC8275VR	MPC8275ZQ
	MPC8270	MPC8270	MPC8270VR	MPC8270ZQ

  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One I^2C controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
  - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

2 Operating Conditions

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	–0.3 – 2.25	V
PLL supply voltage[2]	VCCSYN	–0.3 – 2.25	V
I/O supply voltage[3]	VDDH	–0.3 – 4.0	V
Input voltage[4]	VIN	GND(–0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(–55) – (+150)	°C

[1] Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

Table 5. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE[0–7]/PSDDQM[0–7]/PBS[0–7] PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3] LSDA10/LGPL0/PCI_MODCKH0 LSDWE/LGPL1/PCI_MODCKH1 LOE/LSDRAS/LGPL2/PCI_MODCKH2 LSDCAS/LGPL3/PCI_MODCKH3 LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK LWR MODCK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2]	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR L_A15/FRAME/SMI L_A16/TRDY L_A17/IRDY/CKSTP_OUT L_A18/STOP L_A19/DEVSEL L_A20/IDSEL L_A21/PERR L_A22/SERR L_A23/REQ0 L_A24/REQ1/HSEJSW L_A25/GNT0 L_A26/GNT1/HSLED L_A27/GNT2/HSENUM L_A28/RST/CORE_SRESET L_A29/INTAL_A30/REQ2 L_A31 LCL_D[0-31)]/AD[0-31] LCL_DP[03]/C/BE[0-3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO QREQ				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, either pull unused pins to GND or VDDH or configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

4 V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.
5 MPC8280, MPC8275VR, MPC8275ZQ only.

4 Thermal Characteristics

This table describes thermal characteristics for both the packages. See Table 2 for information on a given SoC's package. Discussions of each characteristic are provided in Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance," and Section 4.5, "Experimental Determination." For the these discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

Table 6. Thermal Characteristics

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA	516 PBGA		
Junction to ambient—single-layer board[1]	$R_{\theta JA}$	16	27	°C/W	Natural convection
		11	21		1 m/s
Junction to ambient—four-layer board	$R_{\theta JA}$	12	19	°C/W	Natural convection
		9	16		1 m/s
Junction to board[2]	$R_{\theta JB}$	6	11	°C/W	—
Junction to case[3]	$R_{\theta JC}$	2	8	°C/W	—
Junction-to-package top[4]	Ψ_{JT}	2	2	°C/W	—

1 Assumes no thermal vias
2 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)
$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

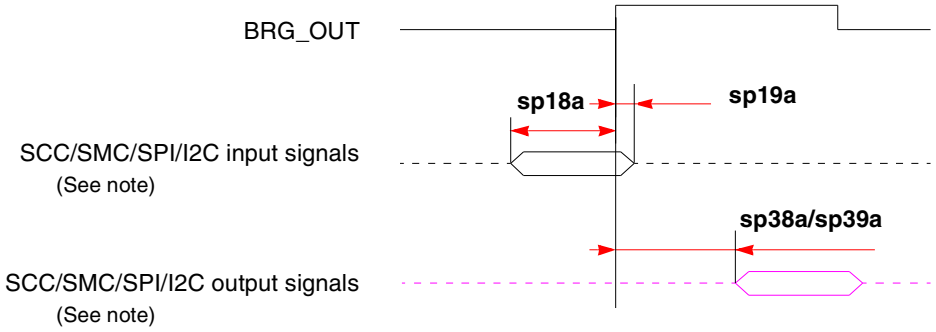
$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

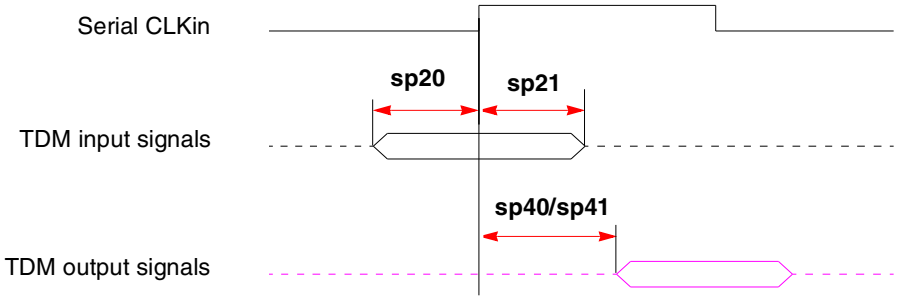
This figure shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

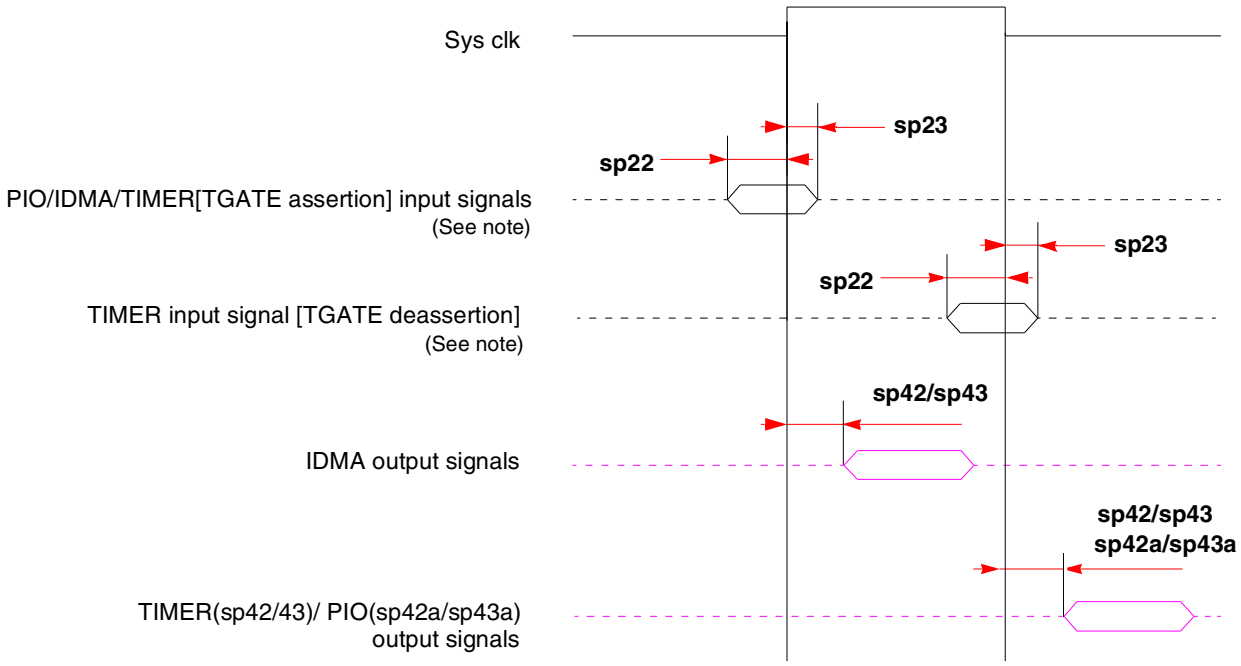
This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/file time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing.

This table lists SIU input characteristics.

Table 13. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11	sp10	$\overline{\text{AACK}}$/$\overline{\text{TA}}$/$\overline{\text{TS}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{ARTRY}}$/ $\overline{\text{TEA}}$	6	5	3.5	0.5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	7	5	3.5	0.5	0.5	0.5
sp13a	sp10	Pipeline mode—Data bus (with or without ECC/PARITY)	5	4	2.5	0.5	0.5	0.5
sp14	sp10	DP pins	7	5	3.5	0.5	0.5	0.5
sp14a	sp10	Pipeline mode—DP pins	—	4	2.5	—	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	0.5	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 14. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31	sp30	$\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$	7	6	5.5	1	1	1
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	1	1	1
sp33a	sp30	Data bus[2]	6.5	6.5	5.5	0.7	0.7	0.7
sp33b	sp30	DP	6	5.5	5.5	1	1	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	1	1	1
sp35a	sp30	AP	7	7	7	1	1	1

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2 To achieve 1 ns of hold time at 66, 83, or 100 MHz, a minimum loading of 20 pF is required.

Table 16. JTAG Timings[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Input hold times Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	 ns ns	 4, 7 4, 7
Output valid times Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 — —	 10 10	 ns ns	 5, 7 5, 7
Output hold times Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 1 1	 — —	 ns ns	 5, 7 5, 7
JTAG external clock to output high impedance Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 1 1	 10 10	 ns ns	 5, 6 5, 6

1 All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to t_{TCLK}.

5 Non-JTAG signal output timing with respect to t_{TCLK}.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

7 Clock Configuration Modes

This SoC includes the following clocking modes:

- Local
- PCI host
- PCI agent

The clocking mode is set according to the following input pins as shown in the following table:

- PCI_MODE
- PCI_CFG[0]
- PCI_MODCK

Table 17. SoC Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK[1]			
1	—	—	Local bus	—	Table 18
0	0	0	PCI host	50–66	Table 19
0	0	1		25–50	Table 20
0	1	0	PCI agent	50–66	Table 21
0	1	1		25–50	Table 22

[1] Determines PCI clock frequency range. See Section 7.2, "PCI Host Mode," and Section 7.3, "PCI Agent Mode."

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

7.1 Local Bus Mode

This table lists clock configurations for the SoC in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

Table 18. Clock Configurations for Local Bus Mode[1]

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
Default Modes (MODCK_H= 0000)								
0000_000	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0000_001	33.3	133.3	3	100.0	400.0	5	166.7	666.7
0000_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0000_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0000_100	60.0	167.0	2	120.0	334.0	2.5	150.0	417.5
0000_101	50.0	167.0	2	100.0	334.0	3	150.0	501.0
0000_110	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0000_111	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
Full Configuration Modes								
0001_000	50.0	167.0	2	100.0	334.0	4	200.0	668.0

Table 18. Clock Configurations for Local Bus Mode[1] (continued)

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
0001_001	50.0	167.0	2	100.0	334.0	5	250.0	835.0
0001_010	50.0	145.8	2	100.0	291.7	6	300.0	875.0
0001_011	Reserved							
0001_100	Reserved							
0001_101	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0001_110	33.3	133.3	3	100.0	400.0	5	166.7	666.7
1000_111	33.3	133.3	3	100.0	400.0	5.5	183.3	733.3
0001_111	33.3	133.3	3	100.0	400.0	6	200.0	800.0
0010_000	Reserved							
0010_001	Reserved							
0010_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0010_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0010_100	25.0	100.0	4	100.0	400.0	6	150.0	600.0
0010_101	25.0	100.0	4	100.0	400.0	7	175.0	700.0
0010_110	25.0	100.0	4	100.0	400.0	8	200.0	800.0
0010_111	Reserved							
0011_000	30.0	80.0	5	150.0	400.0	5	150.0	400.0
0011_001	25.0	80.0	5	125.0	400.0	6	150.0	480.0
0011_010	25.0	80.0	5	125.0	400.0	7	175.0	560.0
0011_011	25.0	80.0	5	125.0	400.0	8	200.0	640.0
0011_100	Reserved							
0011_101	Reserved							
0011_110	25.0	66.7	6	150.0	400.0	6	150.0	400.0
0011_111	25.0	66.7	6	150.0	400.0	7	175.0	466.7
0100_000	25.0	66.7	6	150.0	400.0	8	200.0	533.3
0101_101	75.0	167.0	2	150.0	334.0	2	166.7	334.0
0101_110	60.0	167.0	2	120.0	334.0	2.5	166.7	417.5
0101_111	50.0	167.0	2	100.0	334.0	3	200.0	501.0

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As Table 17 shows, PCI_MODCK determines the PCI clock frequency range. See Table 20 for higher configurations.

3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

4 60x and local bus frequency. Identical to CLKIN.

5 CPM multiplication factor = CPM clock/bus clock

6 CPU multiplication factor = Core PLL multiplication factor

7.3 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI agent mode the following:

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0100_100	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
0101_000	30.0	50.0	5	150.0	250.0	2.5	150.0	250.0	2.5	60.0	100.0
0101_001	25.0	50.0	5	125.0	250.0	3	150.0	300.0	2.5	50.0	100.0
0101_010	25.0	50.0	5	125.0	250.0	3.5	175.0	350.0	2.5	50.0	100.0
0101_011	25.0	50.0	5	125.0	250.0	4	200.0	400.0	2.5	50.0	100.0
0101_100	25.0	50.0	5	125.0	250.0	4.5	225.0	450.0	2.5	50.0	100.0
0101_101	25.0	50.0	5	125.0	250.0	5	250.0	500.0	2.5	50.0	100.0
0101_110	25.0	50.0	5	125.0	250.0	5.5	275.0	550.0	2.5	50.0	100.0

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0110_000	Reserved										
0110_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
0110_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0110_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
0110_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
0111_000	25.0	50.0	6	150.0	300.0	2	150.0	300.0	2	75.0	150.0
0111_001	25.0	50.0	6	150.0	300.0	2.5	187.5	375.0	2	75.0	150.0
0111_010	25.0	50.0	6	150.0	300.0	3	225.0	450.0	2	75.0	150.0
0111_011	25.0	50.0	6	150.0	300.0	3.5	262.5	525.0	2	75.0	150.0
1000_000	Reserved										
1000_001	25.0	50.0	6	150.0	300.0	2.5	150.0	300.0	2.5	60.0	120.0
1000_010	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
1000_011	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1000_100	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1000_101	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LCL_D9/AD9		L26
LCL_D10/AD10		L25
LCL_D11/AD11		M29
LCL_D12/AD12		M28
LCL_D13/AD13		M27
LCL_D14/AD14		M26
LCL_D15/AD15		N29
LCL_D16/AD16		T25
LCL_D17/AD17		U27
LCL_D18/AD18		U26
LCL_D19/AD19		U25
LCL_D20/AD20		V29
LCL_D21/AD21		V28
LCL_D22/AD22		V27
LCL_D23/AD23		V26
LCL_D24/AD24		W27
LCL_D25/AD25		W26
LCL_D26/AD26		W25
LCL_D27/AD27		Y29
LCL_D28/AD28		Y28
LCL_D29/AD29		Y25
LCL_D30/AD30		AA29
LCL_D31/AD31		AA28
LCL_DP0/C0/$\overline{\text{BE0}}$		L28
LCL_DP1/C1/$\overline{\text{BE1}}$		N28
LCL_DP2/C2/$\overline{\text{BE2}}$		T28
LCL_DP3/C3/$\overline{\text{BE3}}$		W28
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$		T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$		D1
$\overline{\text{TRST}}$[1]		AH3
TCK		AG5
TMS		AJ3
TDI		AE6

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
Core power		U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground		AA5, AB1[6], AB2[7], AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 Should be tied to VDDH via a 2K Ω external pull-up resistor.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

3 Must be pulled down or left floating.

4 If PCI is not desired, must be pulled up or left floating.

5 Sphere is not connected to die.

6 GNDSYN (AB1): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the SoC. New designs must connect AB1 to GND and follow the suggestions in Section 4.6, "Layout Practices." Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.

7 XFC (AB2) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8280 because there is no need for external capacitor to operate the PLL. New designs should connect AB2 (XFC) pin to GND. Old designs in which the SoC is used as a drop-in replacement can leave the pin connected to the current capacitor.

This table describes symbols used in Table 23.

Table 24. Symbol Legend

Symbol	Meaning
$\overline{\text{OVERBAR}}$	Signals with overbars, such as $\overline{\text{TA}}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.
RMII	Indicates that a signal is part of the reduced media independent interface.

8.2 VR and ZQ Packages—MPC8275 and MPC8270

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8280 and the MPC8270, see Section 8.1, "ZU and VV Packages—MPC8280 and MPC8270.

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23[2]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26[2]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23[2]
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23[2]
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26[2]
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25[2]
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26[2]
PA26/FCC1_MII_RMII_RX_ER/	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25[2]
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	C25[2]
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	$\overline{\text{FCC1\_UTM\_RXENB}}$/ $\overline{\text{FCC1\_UTS\_RXENB}}$	C22[2]
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21[2]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20[2]
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UTM\_TXENB}}$/ $\overline{\text{FCC1\_UTS\_TXENB}}$	A19[2]
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	FCC2_UT8_RXD0	AD21[2]
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD22[2]
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22[2]
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26[2]
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23[2]
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26[2]
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25[2]
PB12/FCC3_MII_CRS/TXD2		W26[2]
PB13/FCC3_MII_COL/L1TXD1A2		W25[2]
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25[2]
PC6/FCC1_CD	FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25[2]
PC7/FCC1_CTS	FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24[2]
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USB_RN	FCC1_UT16_TXD0	Y24[2]
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	U22[2]
PC10/CD3/RENA3	FCC1_UT16_TXD2/FCC2_UT8_RXD3	V23[2]
PC11/CTS3/CLSN3/L1TXD3A2	FCC2_UT8_RXD2	U23[2]
PC12/CD2/RENA2	FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26[2]
PC13/CTS2/CLSN2	FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26[2]
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26[2]
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24[2]
PC16/CLK16/TIN4		M26[2]
PC17/CLK15/TIN3/BRGO8		L26[2]
PC18/CLK14/TGATE2		M24[2]
PC19/CLK13/BRGO7/SPICLK		L22[2]
PC20/CLK12/TGATE1/USB_OE		K25[2]
PC21/CLK11/BRGO6		J25[2]
PC22/CLK10/DONE1	FCC1_UT_TXPRTY	G26[2]
PC23/CLK9/BRGO5/DACK1		F26[2]
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	G24[2]
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25[2]
PC26/CLK6/TOUT3/TMCLK		G23[2]
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		B23[2]
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	FCC2_UT_RXADDR4	E22[2]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21[2]
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	D21[2]

9.1 Package Parameters

This table provides package parameters.

NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

Table 26. Package Parameters

Package	SoCs	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8280 MPC8270	37.5 × 37.5	TBGA	480	1.27	1.55
VV	MPC8280 MPC8270	37.5 × 37.5	TBGA	480	1.27	1.55
VR	MPC8275VR MPC8270VR	27 × 27	PBGA	516	1	2.25
ZQ	MPC8275ZQ MPC8270ZQ	27 × 27	PBGA	516	1	2.25