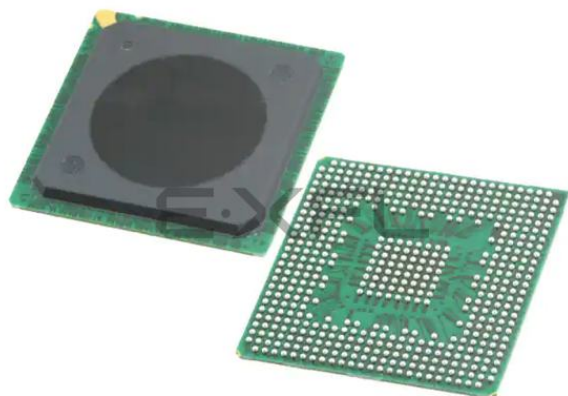




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8275cvmiba

- Common on-chip processor (COP) test interface
- High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
- Supports bus snooping
- Support for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
 - G2_LE core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
 - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
 - Programmable host bridge and agent
 - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- PCI bridge
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
 - PCI host bridge or peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI

Operating Conditions

- ² **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.
- ³ **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.
- ⁴ **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

This table lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions¹

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.45 – 1.60	V
PLL supply voltage	VCCSYN	1.45 – 1.60	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T _j	105 ²	°C
Ambient temperature	T _A	0–70 ²	°C

¹ **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

² Note that for extended temperature parts the range is (–40)T_A – 105T_j.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

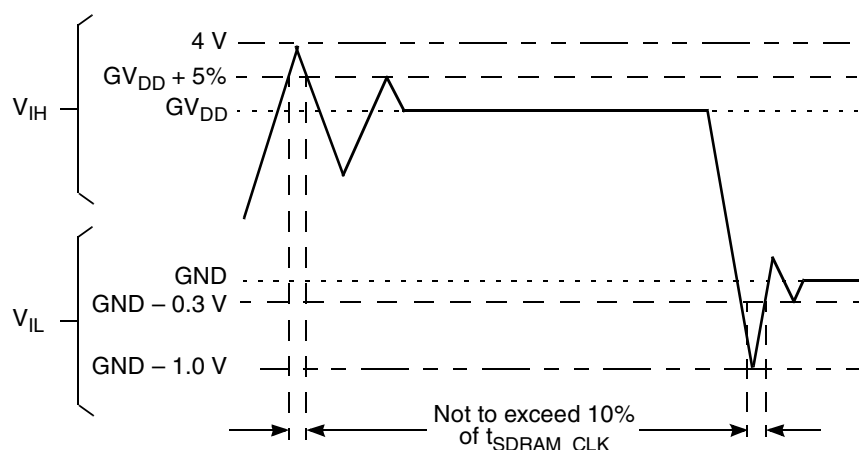


Figure 2. Overshoot/Undershoot Voltage

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Table 8. Output Buffer Impedances¹

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27 ²
Local bus	45
Memory controller	45 or 27 ²
Parallel I/O	45
PCI	27

¹ These are typical values at 65° C. Impedance may vary by $\pm 25\%$ with process and temperature.

² On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45 Ω .
On all other revisions, impedance value is selected through the SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

This table lists CPM output characteristics.

Table 9. AC Characteristics for CPM Outputs¹

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	0.5	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 10. AC Characteristics for CPM Inputs¹

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	2	2	2
sp20	sp21	TDM inputs/SI	5	5	5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	0.5	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

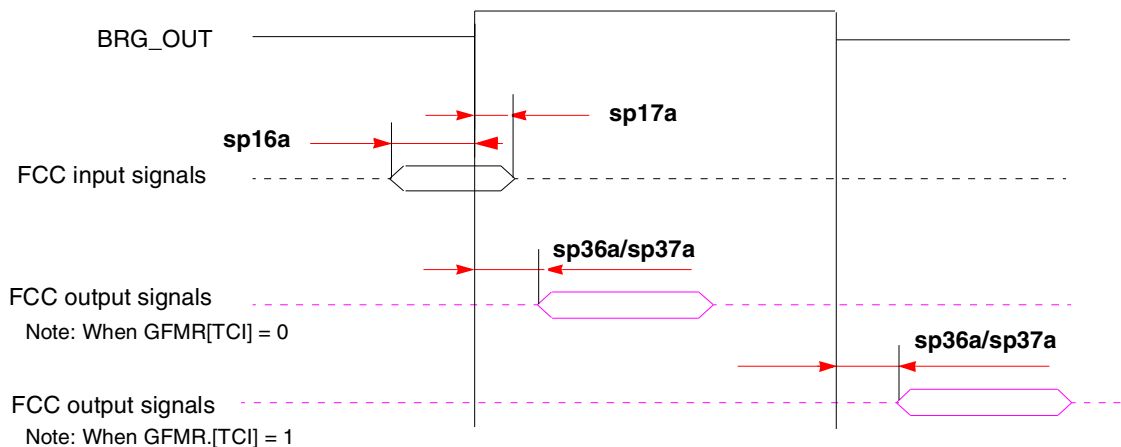


Figure 3. FCC Internal Clock Diagram

This figure shows the FCC external clock.

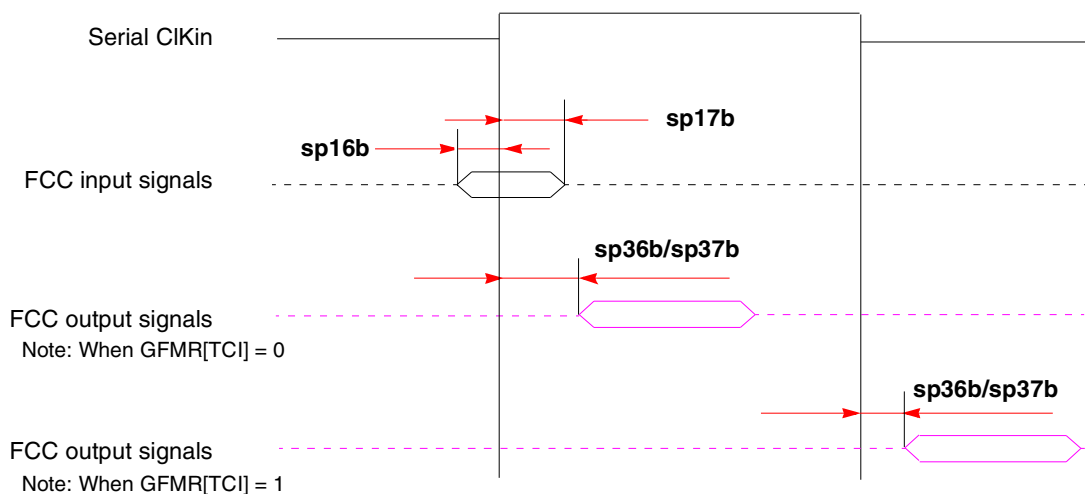
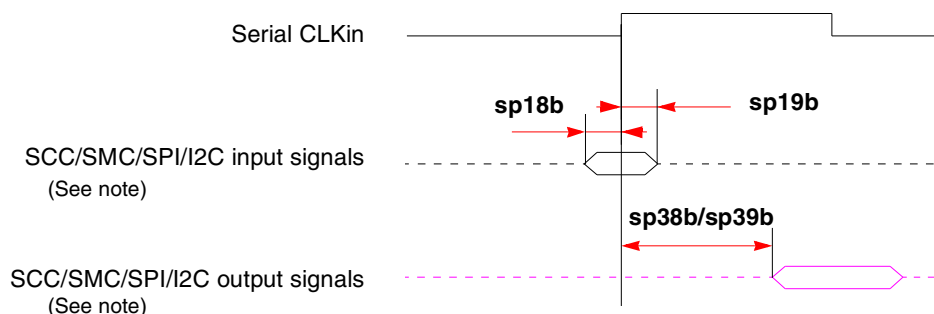


Figure 4. FCC External Clock Diagram

This figure shows the SCC/SMC/SPI/I²C external clock.

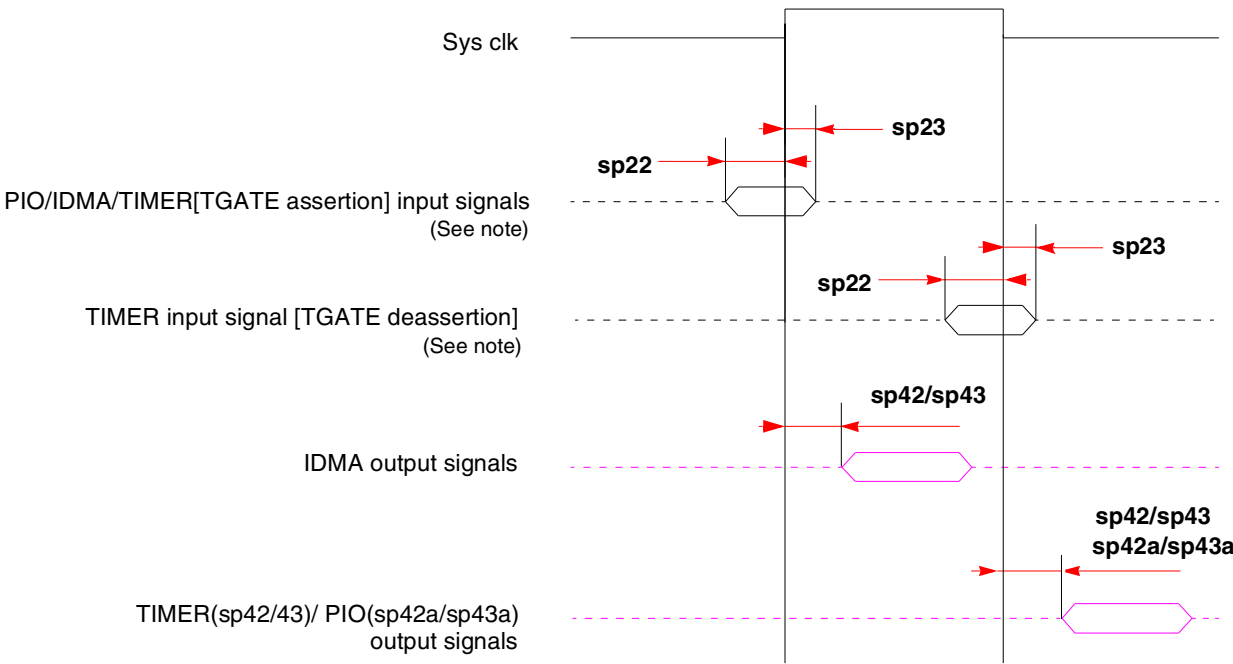


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed ± 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/fall time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See [Section 7, “Clock Configuration Modes,”](#) and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

This figure shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

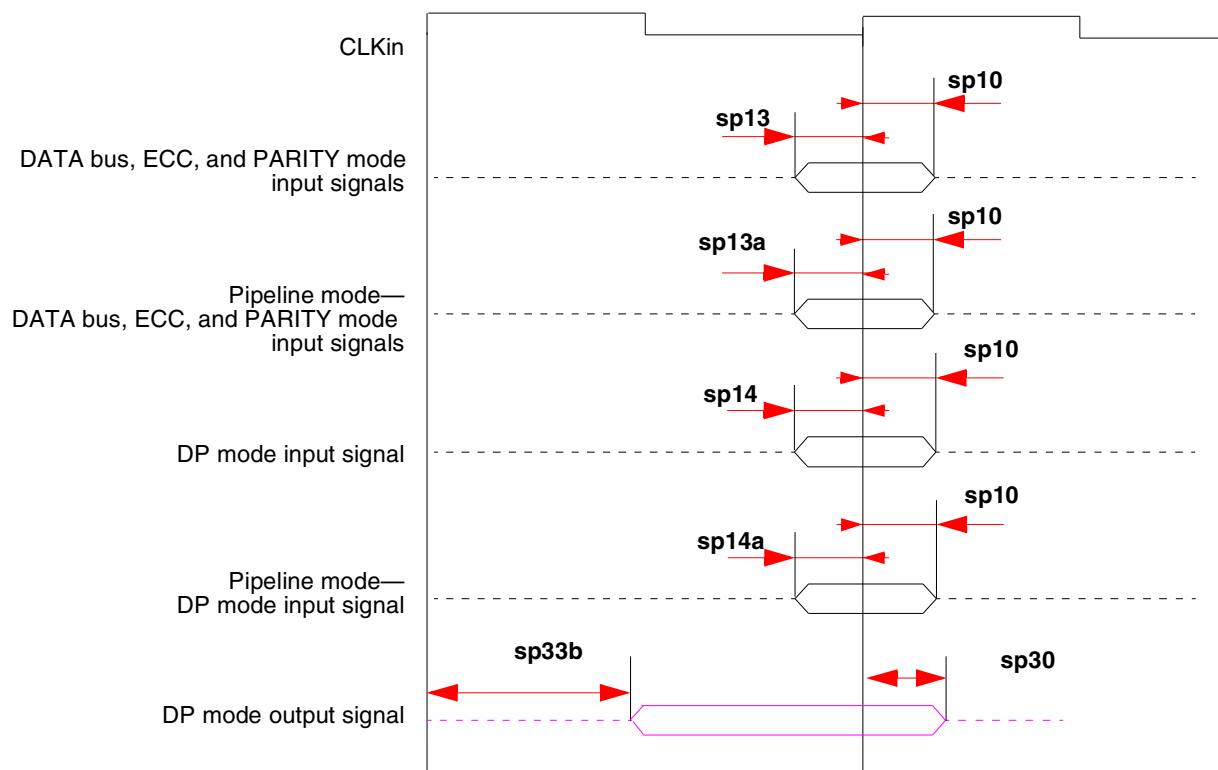


Figure 10. Parity Mode Diagram

This figure shows signal behavior in MEMC mode.

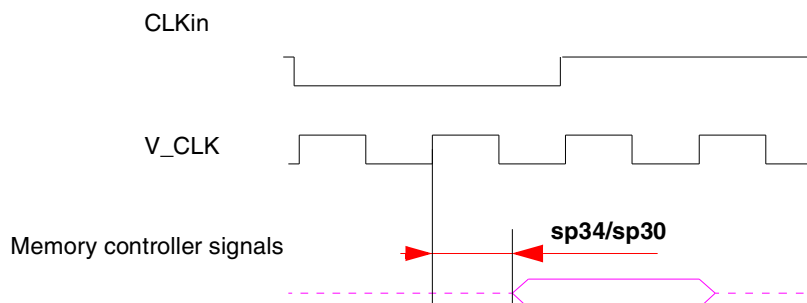


Figure 11. MEMC Mode Diagram

NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in [Table 15](#).

Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)^{1,2} (continued)

Mode ³	Bus Clock ⁴ (MHz)		CPM Multiplication Factor ⁵	CPM Clock (MHz)		CPU Multiplication Factor ⁶	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7
1011_100	80.0	106.7	2.5	200.0	266.6	4	320.0	426.6	4	50.0	66.7
1011_101	80.0	106.7	2.5	200.0	266.6	4.5	360.0	480.0	4	50.0	66.7
1101_000	100.0	133.3	2.5	250.0	333.3	3	300.0	400.0	5	50.0	66.7
1101_001	100.0	133.3	2.5	250.0	333.3	3.5	350.0	466.6	5	50.0	66.7
1101_010	100.0	133.3	2.5	250.0	333.3	4	400.0	533.3	5	50.0	66.7
1101_011	100.0	133.3	2.5	250.0	333.3	4.5	450.0	599.9	5	50.0	66.7
1101_100	100.0	133.3	2.5	250.0	333.3	5	500.0	666.6	5	50.0	66.7
1101_101	125.0	166.7	2	250.0	333.3	3	375.0	500.0	5	50.0	66.7
1101_110	125.0	166.7	2	250.0	333.3	4	500.0	666.6	5	50.0	66.7
1110_000	100.0	133.3	3	300.0	400.0	3.5	350.0	466.6	6	50.0	66.7
1110_001	100.0	133.3	3	300.0	400.0	4	400.0	533.3	6	50.0	66.7
1110_010	100.0	133.3	3	300.0	400.0	4.5	450.0	599.9	6	50.0	66.7
1110_011	100.0	133.3	3	300.0	400.0	5	500.0	666.6	6	50.0	66.7
1110_100	100.0	133.3	3	300.0	400.0	5.5	550.0	733.3	6	50.0	66.7
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	Bus Clock ⁴ (MHz)		CPM Multiplication Factor ⁵	CPM Clock (MHz)		CPU Multiplication Factor ⁶	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0
1000_010	66.7	133.3	3	200.0	400.0	3.5	233.3	466.7	8	25.0	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	114.3	3.5	200.0	400.0	3.5	200.0	400.0	8	25.0	50.0
1001_011	57.1	114.3	3.5	200.0	400.0	4	228.6	457.1	8	25.0	50.0
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	42.9	85.7	3.5	150.0	300.0	5	214.3	428.6	6	25.0	50.0
1001_110	42.9	85.7	3.5	150.0	300.0	5.5	235.7	471.4	6	25.0	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0

This figure shows the pinout of the ZU and VV packages as viewed from the top surface.

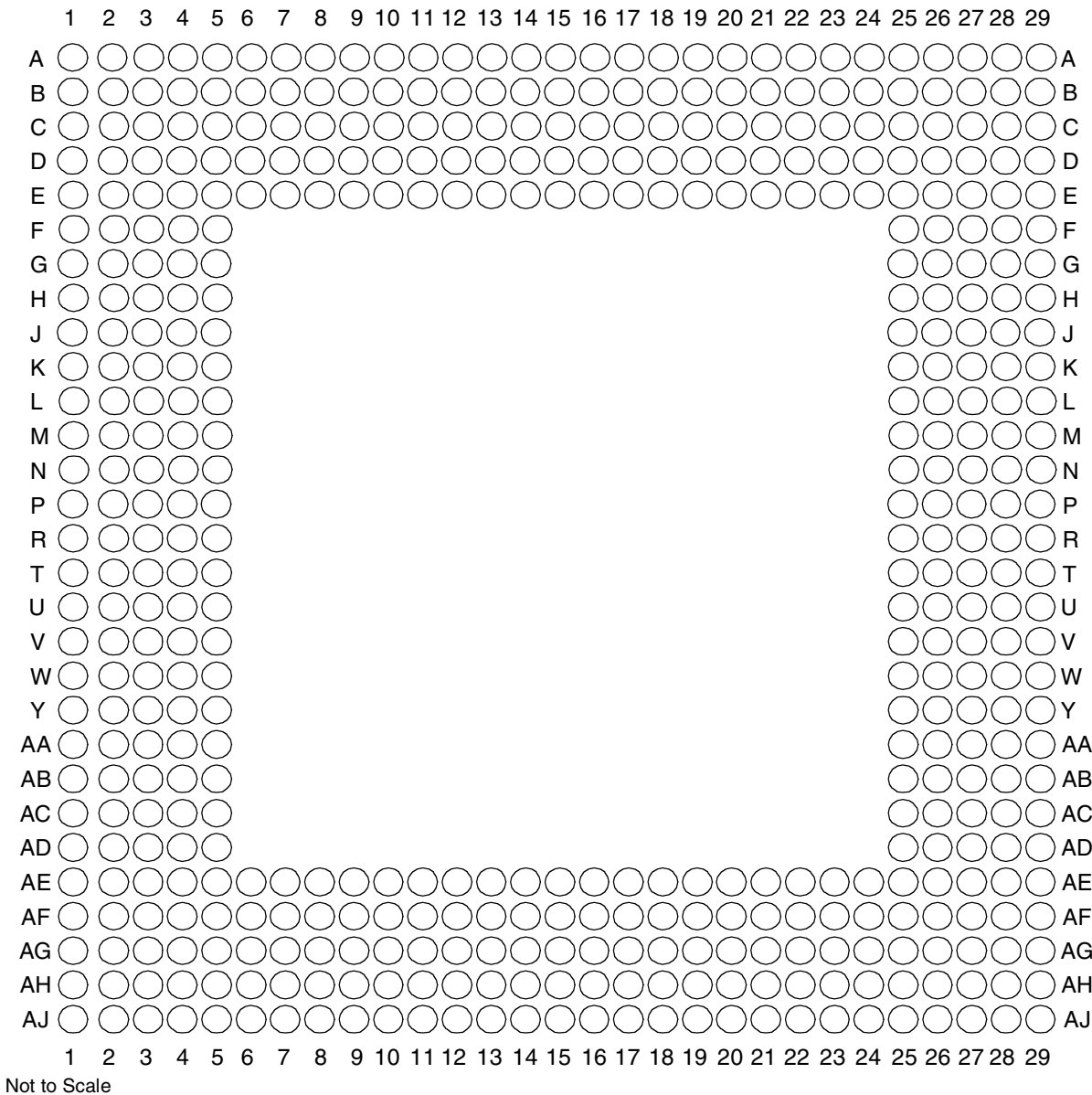


Figure 13. Pinout of the 480 TBGA Package (View from Top)

This table lists the pins of the MPC8280 and MPC8270, and [Table 24](#) defines conventions and acronyms used in this table.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{\text{BR}}$		W5
$\overline{\text{BG}}$		F4

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCCI_RMII_RXD0	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	AE16 ²
PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT8_TXD7/FCC1_UT16_TXD15	AJ16 ²
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	AG15 ²
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	AJ13 ²
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	AE13 ²
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12 ²
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11 ²
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	AH9 ²
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	AJ8 ²
PA26/FCC1_RMII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	AH7 ²
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	AF7 ²
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	AD5 ²
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	AF1 ²
PA30/FCC1_MII_CRS/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	AD3 ²
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	AB5 ²
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/FCC3_RTS	FCC2_UT8_RXD0	AD28 ²
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD26 ²
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AD25 ²
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26 ²
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3/L1RSYNCD1	AH27 ²
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2/L1TSYNCD1/ L1GNTD1	AG24 ²

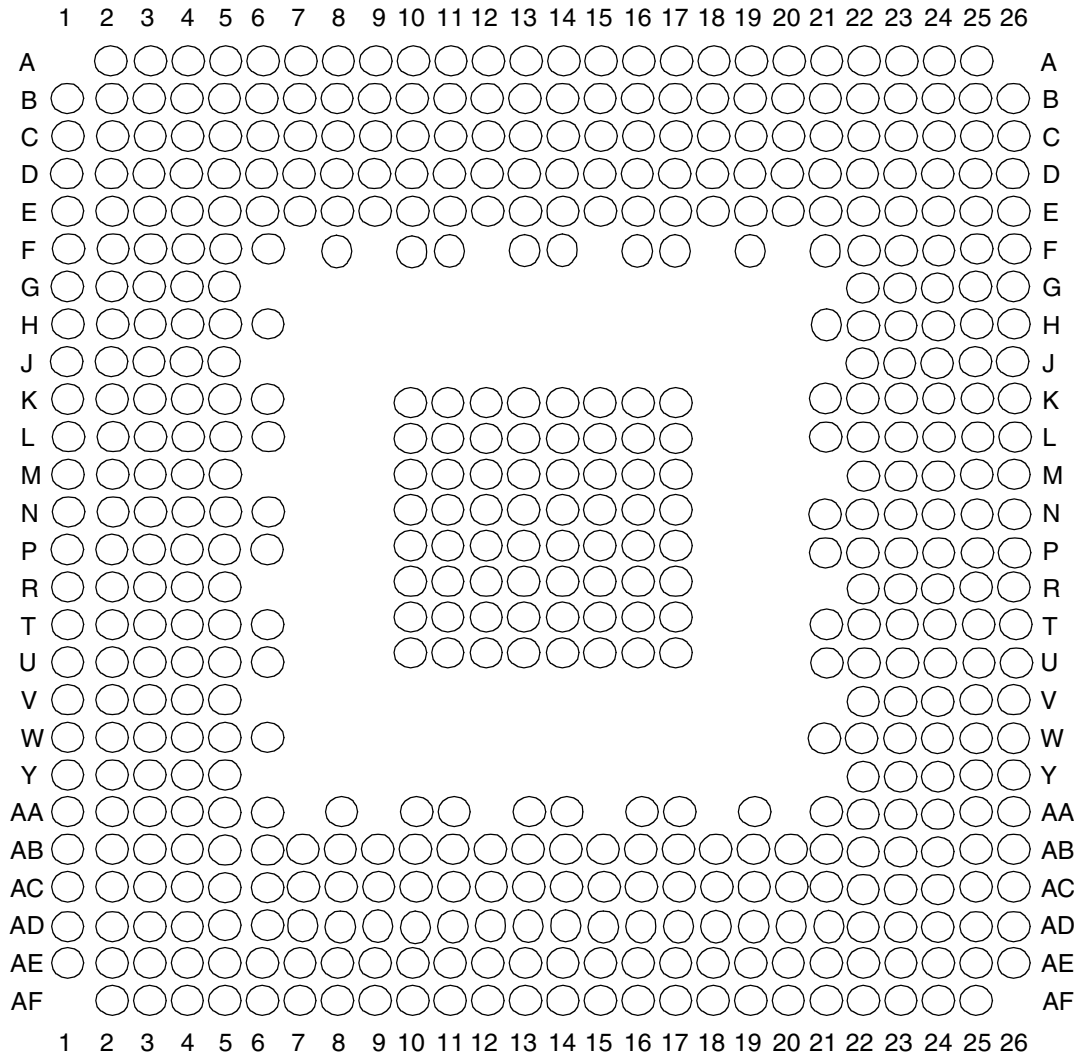
Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24 ²
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24 ²
PB12/FCC3_MII_CRS/TXD2	L1CLKOB1/L1RSYNCC1	AG22 ²
PB13/FCC3_MII_COL/L1TXD1A2	L1RQB1/L1TSYNCC1/L1GNTC1	AH21 ²
PB14/FCC3_MII_RMII_TX_EN/RXD3	L1RXDC1	AG20 ²
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19 ²
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18 ²
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV	L1RQA1	AJ17 ²
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14 ²
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13 ²
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12 ²
PB21/FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11 ²
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16 ²
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15 ²
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9 ²
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9 ²
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7 ²
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6 ²
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/FCC2_RTS/ L1TSYNCB2/L1GNTB2/TXD1		AE3 ²
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2 ²
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5 ²
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4 ²

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PD20/ $\overline{\text{RTS4}}$ /TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	AJ14 ²
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	AH13 ²
PD22/RXD4/L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	AJ12 ²
PD23/ $\overline{\text{RTS3}}$ /TENA3	FCC1_UT16_RXD4/L1RSYNCD1	AE12 ²
PD24/TXD3	FCC1_UT16_RXD5/L1RXDD1	AF10 ²
PD25/RXD3	FCC1_UT16_TXD6/L1TXDD1	AG9 ²
PD26/ $\overline{\text{RTS2}}$ /TENA2	FCC1_UT16_RXD6/L1RSYNCC1	AH8 ²
PD27/TXD2	FCC1_UT16_RXD7/L1RXDC1	AG7 ²
PD28/RXD2	FCC1_UT16_TXD7/L1TXDC1	AE4 ²
PD29/ $\overline{\text{RTS1}}$ /TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	AG1 ²
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	AD4 ²
PD31/RXD1		AD2 ²
VCCSYN		AB3
VCCSYN1		B9
CLKIN2		AE11
SPARE4 ³		U5
PCI_MODE ⁴		AF25
SPARE6 ³		V4
No connect ⁵		AA1, AG4
I/O power		AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5

This figure shows the pinout of the VR and ZQ packages as viewed from the top surface.



Not to Scale

Figure 14. Pinout of the 516 PBGA Package (View from Top)

This table shows the pinout list of the MPC8275 and MPC8270. [Table 24](#) defines conventions and acronyms used in [Table 25](#).

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
$\overline{\text{BR}}$		C16
$\overline{\text{BG}}$		D2
$\overline{\text{ABB/IRQ2}}$		C1
$\overline{\text{TS}}$		D1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
LCL_D11/AD11		AC13
LCL_D12/AD12		AC12
LCL_D13/AD13		AB13
LCL_D14/AD14		AD12
LCL_D15/AD15		AF14
LCL_D16/AD16		AF17
LCL_D17/AD17		AE16
LCL_D18/AD18		AD16
LCL_D19/AD19		AC16
LCL_D20/AD20		AB16
LCL_D21/AD21		AF18
LCL_D22/AD22		AE17
LCL_D23/AD23		AD17
LCL_D24/AD24		AB17
LCL_D25/AD25		AE18
LCL_D26/AD26		AD18
LCL_D27/AD27		AC18
LCL_D28/AD28		AE19
LCL_D29/AD29		AF20
LCL_D30/AD30		AD19
LCL_D31/AD31		AB18
LCL_DP0/C0/ $\overline{\text{BE}}0$		AE12
LCL_DP1/C1/ $\overline{\text{BE}}1$		AA13
LCL_DP2/C2/ $\overline{\text{BE}}2$		AC15
LCL_DP3/C3/ $\overline{\text{BE}}3$		AF19
$\overline{\text{IRQ}}0/\overline{\text{NMI_OUT}}$		A11
$\overline{\text{IRQ}}7/\overline{\text{INT_OUT/APE}}$		E5
$\overline{\text{TRST}}^1$		F22
TCK		A24
TMS		C24
TDI		A25
TDO		B24
$\overline{\text{TRIS}}$		C19

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PB15/FCC3_MII_TX_ER/RXD2		U24 ²
PB16/FCC3_MII_RMII_RX_ER/CLK18		R22 ²
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV		R23 ²
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	M23 ²
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	L24 ²
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6	K24 ²
PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7	L21 ²
PB22/FCC2_MII_HDLC_RMII_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7	P25 ²
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6	N25 ²
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5	E26 ²
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4	H23 ²
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	C26 ²
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	B26 ²
PB28/FCC2_MII_RX_ER/FCC2_RMII_RX_ER/ FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1		A22 ²
PB29/L1RSYNCB2/ FCC2_MII_TX_EN/FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	A21 ²
PB30/FCC2_MII_RX_DV/L1RXDB2/ FCC2_RMII_CRS_DV	FCC2_UT_TXSOC	E20 ²
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	C20 ²
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AE22 ²
PC1/DREQ2/SPISEL/BRGO6/L1RQA2		AA19 ²
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AF24 ²
PC3/FCC3_CTS/DACK2/CTS4/ USB_RP	FCC2_UT8_TXD2	AE25 ²
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AB22 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25 ²
PC6/FCC1_CD	FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25 ²
PC7/FCC1_CTS	FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24 ²
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USB_RN	FCC1_UT16_TXD0	Y24 ²
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	U22 ²
PC10/CD3/RENA3	FCC1_UT16_TXD2/FCC2_UT8_RXD3	V23 ²
PC11/CTS3/CLSN3/L1TXD3A2	FCC2_UT8_RXD2	U23 ²
PC12/CD2/RENA2	FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26 ²
PC13/CTS2/CLSN2	FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26 ²
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26 ²
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24 ²
PC16/CLK16/TIN4		M26 ²
PC17/CLK15/TIN3/BRGO8		L26 ²
PC18/CLK14/TGATE2		M24 ²
PC19/CLK13/BRGO7/SPICLK		L22 ²
PC20/CLK12/TGATE1/USB_OE		K25 ²
PC21/CLK11/BRGO6		J25 ²
PC22/CLK10/DONE1	FCC1_UT_TXPRTY	G26 ²
PC23/CLK9/BRGO5/DACK1		F26 ²
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	G24 ²
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25 ²
PC26/CLK6/TOUT3/TMCLK		G23 ²
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		B23 ²
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	FCC2_UT_RXADDR4	E22 ²
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21 ²
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	D21 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC31/CLK1/BRGO1		B20 ²
PD4/BRGO8/ $\overline{\text{FCC3_RTS}}$ /SMRXD2		AF23 ²
PD5/ $\overline{\text{DONE1}}$	FCC1_UT16_TXD3	AE23 ²
PD6/ $\overline{\text{DACK1}}$	FCC1_UT16_TXD4	AB21 ²
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AD23 ²
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AD26 ²
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22 ²
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1	AB24 ²
PD11/L1RQB2	FCC2_UT8_RXD0 L1GNTB1	Y23 ²
PD12		AA26 ²
PD13		W24 ²
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22 ²
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26 ²
PD16/SPIMISO	FCC1_UT_TXPRTY	T23 ²
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25 ²
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	P23 ²
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	N22 ²
PD20/ $\overline{\text{RTS4}}$ /TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	M25 ²
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	L25 ²
PD22/RXD4/L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	J26 ²
PD23/ $\overline{\text{RTS3}}$ /TENA3	FCC1_UT16_RXD4	K22 ²
PD24/TXD3	FCC1_UT16_RXD5	G25 ²
PD25/RXD3	FCC1_UT16_TXD6	H24 ²
PD26/ $\overline{\text{RTS2}}$ /TENA2	FCC1_UT16_RXD6	F24 ²