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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8280cvvqlda

  - Common on-chip processor (COP) test interface
  - High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
  - Supports bus snooping
  - Support for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
  - PCI host bridge or peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI

  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
  - Supports the I_2O standard
  - Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66.67/83.33/100 MHz, 3.3 V specification
  - 60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port
  - Uses the local bus signals, removing need for additional pins
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- 12-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x) and byte selects for 32-bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2_LE core through an on-chip 32 KB dual-port data RAM, an on-chip 32 KB dual-port instruction RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

This figure shows the FCC external clock.

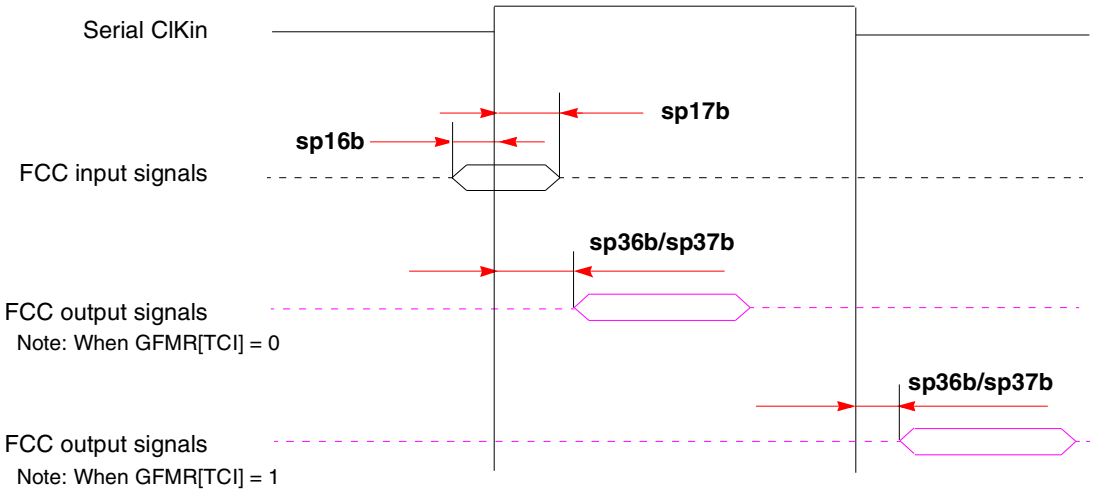
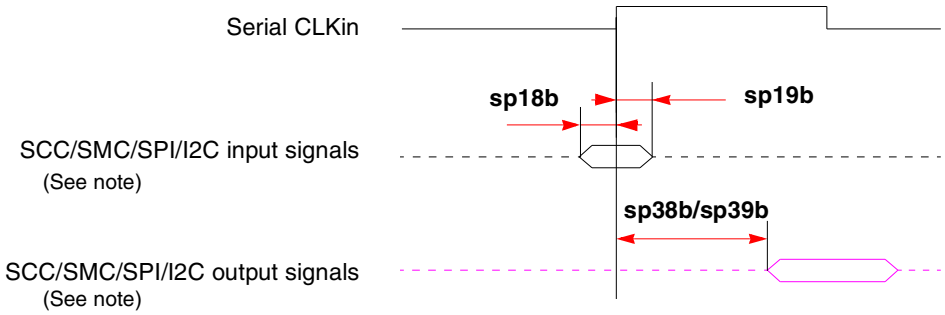


Figure 4. FCC External Clock Diagram

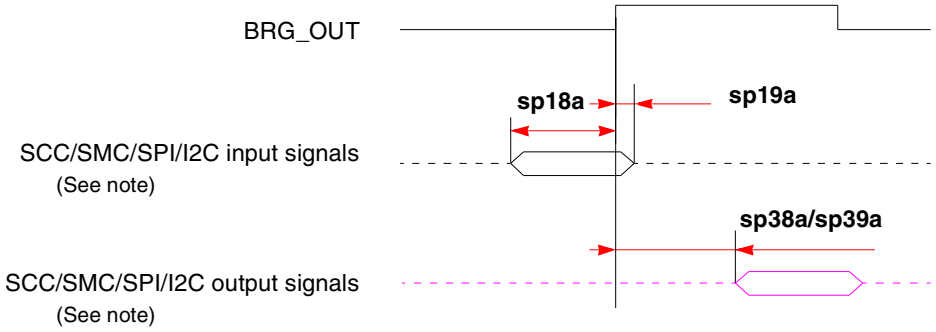
This figure shows the SCC/SMC/SPI/I^2C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^2C External Clock Diagram

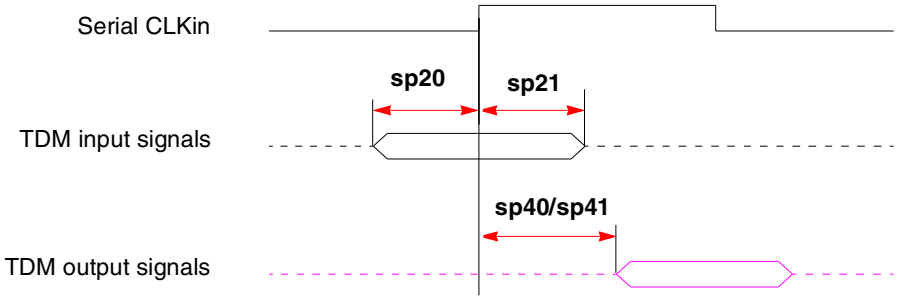
This figure shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

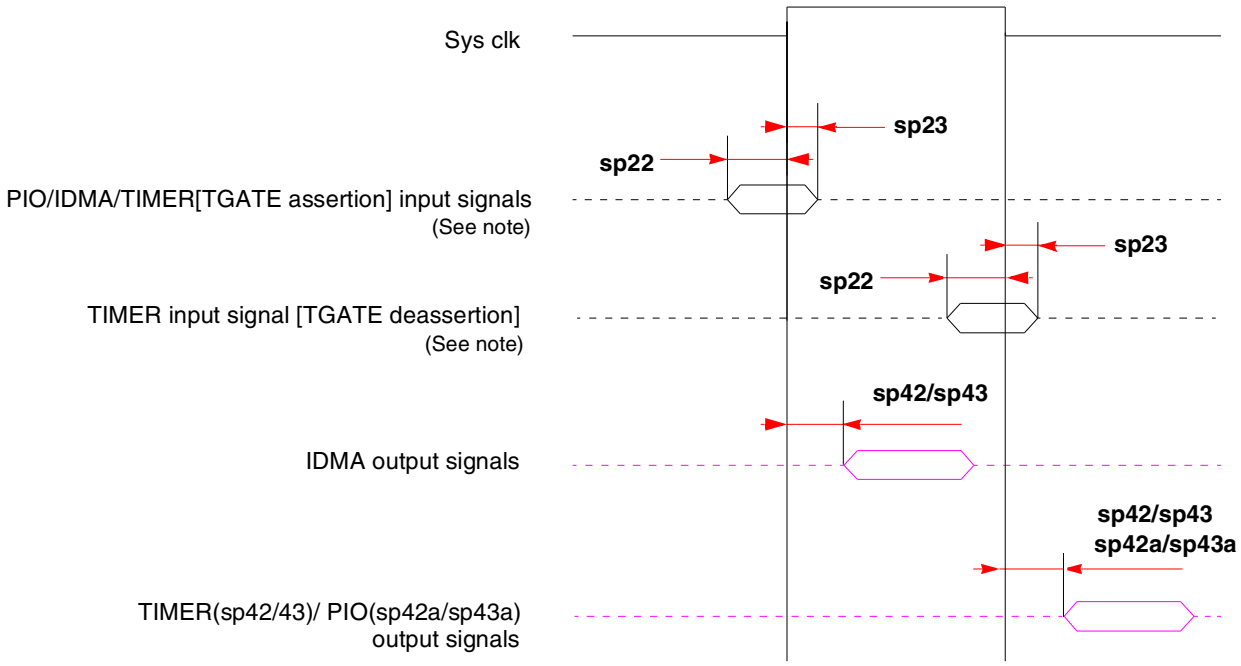
This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/file time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing.

This table lists SIU input characteristics.

Table 13. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11	sp10	$\overline{\text{AACK}}$/$\overline{\text{TA}}$/$\overline{\text{TS}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{ARTRY}}$/ $\overline{\text{TEA}}$	6	5	3.5	0.5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	7	5	3.5	0.5	0.5	0.5
sp13a	sp10	Pipeline mode—Data bus (with or without ECC/PARITY)	5	4	2.5	0.5	0.5	0.5
sp14	sp10	DP pins	7	5	3.5	0.5	0.5	0.5
sp14a	sp10	Pipeline mode—DP pins	—	4	2.5	—	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	0.5	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 14. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31	sp30	$\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$	7	6	5.5	1	1	1
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	1	1	1
sp33a	sp30	Data bus[2]	6.5	6.5	5.5	0.7	0.7	0.7
sp33b	sp30	DP	6	5.5	5.5	1	1	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	1	1	1
sp35a	sp30	AP	7	7	7	1	1	1

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2 To achieve 1 ns of hold time at 66, 83, or 100 MHz, a minimum loading of 20 pF is required.

This figure shows the interaction of several bus signals.

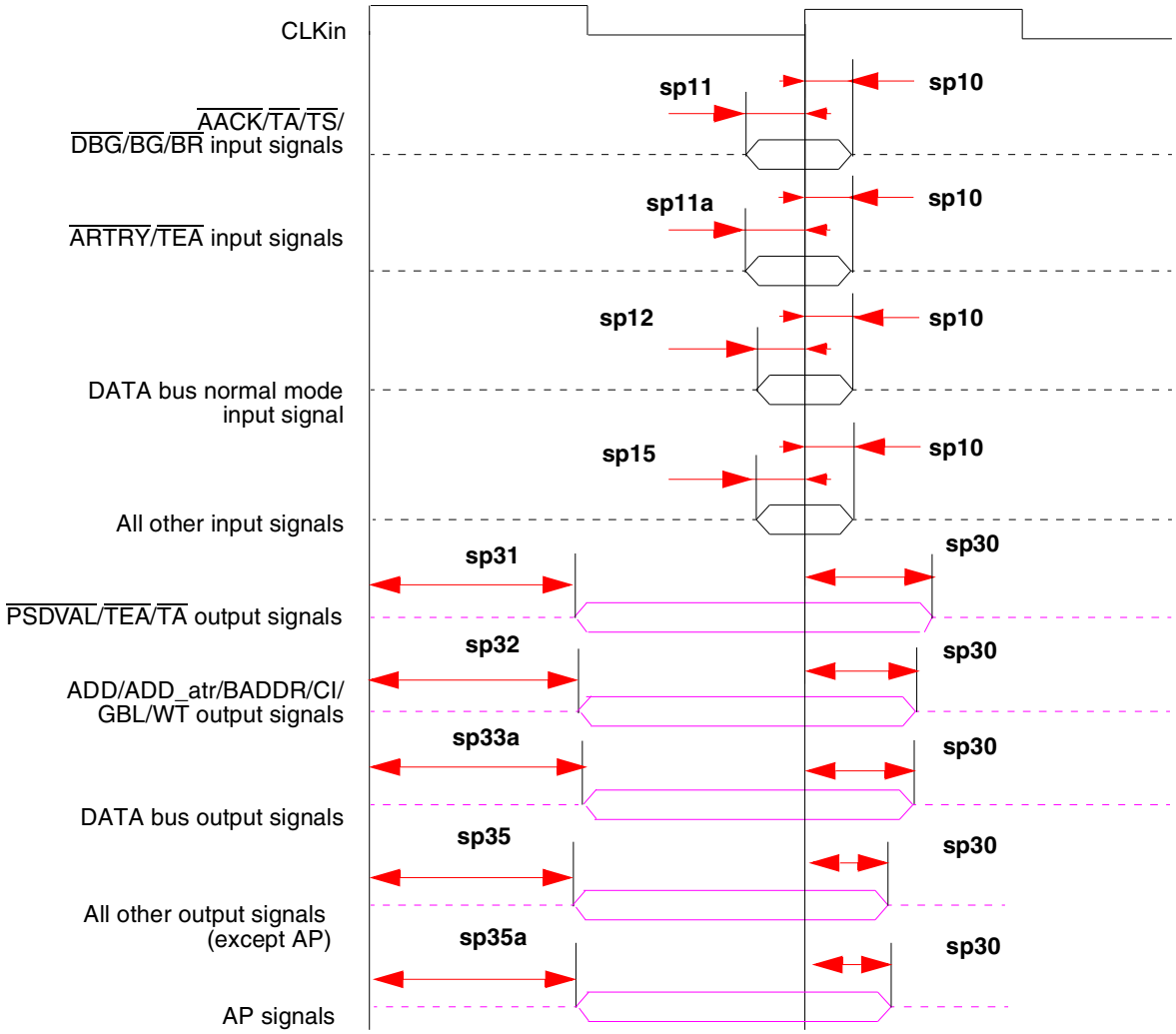


Figure 9. Bus Signals

Table 18. Clock Configurations for Local Bus Mode[1] (continued)

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
0001_001	50.0	167.0	2	100.0	334.0	5	250.0	835.0
0001_010	50.0	145.8	2	100.0	291.7	6	300.0	875.0
0001_011	Reserved							
0001_100	Reserved							
0001_101	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0001_110	33.3	133.3	3	100.0	400.0	5	166.7	666.7
1000_111	33.3	133.3	3	100.0	400.0	5.5	183.3	733.3
0001_111	33.3	133.3	3	100.0	400.0	6	200.0	800.0
0010_000	Reserved							
0010_001	Reserved							
0010_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0010_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0010_100	25.0	100.0	4	100.0	400.0	6	150.0	600.0
0010_101	25.0	100.0	4	100.0	400.0	7	175.0	700.0
0010_110	25.0	100.0	4	100.0	400.0	8	200.0	800.0
0010_111	Reserved							
0011_000	30.0	80.0	5	150.0	400.0	5	150.0	400.0
0011_001	25.0	80.0	5	125.0	400.0	6	150.0	480.0
0011_010	25.0	80.0	5	125.0	400.0	7	175.0	560.0
0011_011	25.0	80.0	5	125.0	400.0	8	200.0	640.0
0011_100	Reserved							
0011_101	Reserved							
0011_110	25.0	66.7	6	150.0	400.0	6	150.0	400.0
0011_111	25.0	66.7	6	150.0	400.0	7	175.0	466.7
0100_000	25.0	66.7	6	150.0	400.0	8	200.0	533.3
0101_101	75.0	167.0	2	150.0	334.0	2	166.7	334.0
0101_110	60.0	167.0	2	120.0	334.0	2.5	166.7	417.5
0101_111	50.0	167.0	2	100.0	334.0	3	200.0	501.0

Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
0100_000	Reserved										
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0101_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0101_010	50.0	66.7	2	100.0	133.3	3.5	175.0	233.3	2	50.0	66.7
0101_011	50.0	66.7	2	100.0	133.3	4	200.0	266.6	2	50.0	66.7
0101_100	50.0	66.7	2	100.0	133.3	4.5	225.0	300.0	2	50.0	66.7
0110_000	60.0	80.0	2.5	150.0	200.0	2.5	150.0	200.0	3	50.0	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As Table 17 shows, PCI_MODCK determines the PCI clock frequency range. See Table 20 for higher configurations.

3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

4 60x and local bus frequency. Identical to CLKIN.

5 CPM multiplication factor = CPM clock/bus clock

6 CPU multiplication factor = Core PLL multiplication factor

7.3 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI agent mode the following:

2 As shown in Table 17, PCI_MODCK determines the PCI clock range. See Table 20 for higher range configurations.
3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
4 CPM multiplication factor = CPM clock/PCI clock
5 CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This section provides the pin assignments and pinout lists for both HiP7 PowerQUICC II packages.

8.1 ZU and VV Packages—MPC8280 and MPC8270

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, see Section 8.2, “VR and ZQ Packages—MPC8275 and MPC8270.”

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/TXD2	L1CLKOB1/L1RSYNCC1	AG22[2]
PB13/FCC3_MII_COL/L1TXD1A2	$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1	AH21[2]
PB14/FCC3_MII_RMII_TX_EN//RXD3	L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19[2]
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18[2]
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV	L1RQA1	AJ17[2]
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14[2]
PB19FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13[2]
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12[2]
PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11[2]
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16[2]
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15[2]
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9[2]
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7[2]
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6[2]
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1		AE3[2]
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2[2]
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5[2]
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23[2]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26[2]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23[2]
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23[2]
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26[2]
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25[2]
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26[2]
PA26/FCC1_MII_RMII_RX_ER/	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25[2]
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	C25[2]
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	$\overline{\text{FCC1\_UTM\_RXENB}}$/ $\overline{\text{FCC1\_UTS\_RXENB}}$	C22[2]
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21[2]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20[2]
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UTM\_TXENB}}$/ $\overline{\text{FCC1\_UTS\_TXENB}}$	A19[2]
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	FCC2_UT8_RXD0	AD21[2]
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD22[2]
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22[2]
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26[2]
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23[2]
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26[2]
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25[2]
PB12/FCC3_MII_CRS/TXD2		W26[2]
PB13/FCC3_MII_COL/L1TXD1A2		W25[2]
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC31/CLK1/BRGO1		B20[2]
PD4/BRGO8/FCC3_RTS/SMRXD2		AF23[2]
PD5/DONE1	FCC1_UT16_TXD3	AE23[2]
PD6/DACK1	FCC1_UT16_TXD4	AB21[2]
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AD23[2]
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AD26[2]
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22[2]
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1	AB24[2]
PD11/L1RQB2	FCC2_UT8_RXD0 L1GNTB1	Y23[2]
PD12		AA26[2]
PD13		W24[2]
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22[2]
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26[2]
PD16/SPIMISO	FCC1_UT_TXPRTY	T23[2]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25[2]
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	P23[2]
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	N22[2]
PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	M25[2]
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	L25[2]
PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	J26[2]
PD23/RTS3/TENA3	FCC1_UT16_RXD4	K22[2]
PD24/TXD3	FCC1_UT16_RXD5	G25[2]
PD25/RXD3	FCC1_UT16_TXD6	H24[2]
PD26/RTS2/TENA2	FCC1_UT16_RXD6	F24[2]

3 Must be pulled down or left floating.
4 If PCI is not desired, must be pulled up or left floating.
5 Sphere is not connected to die.
6 GNDSYN (B18): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8275/MPC8270. New designs must connect B18 to GND and follow the suggestions in Section 4.6, "Layout Practices." Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.
7 XFC (A18) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8275/MPC8270 because there is no need for external capacitor to operate the PLL. New designs should connect A18 (XFC) pin to GND. Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to the current capacitor.

9 Package Description

This figure shows the side profile of the TBGA package to indicate the direction of the top surface view.

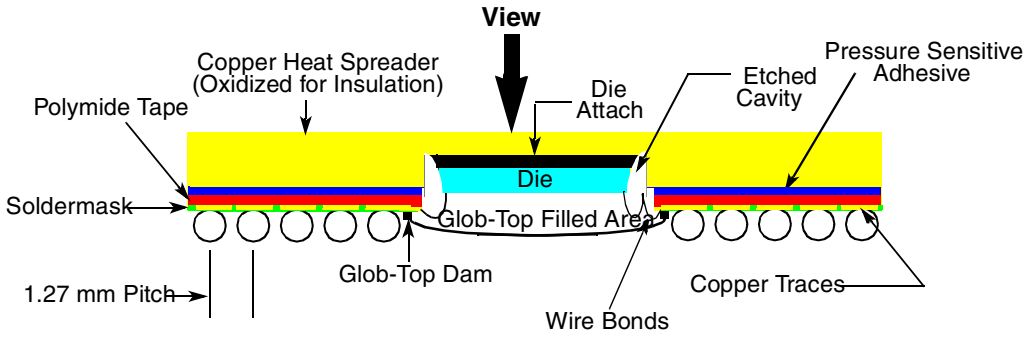


Figure 15. Side View of the TBGA Package

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

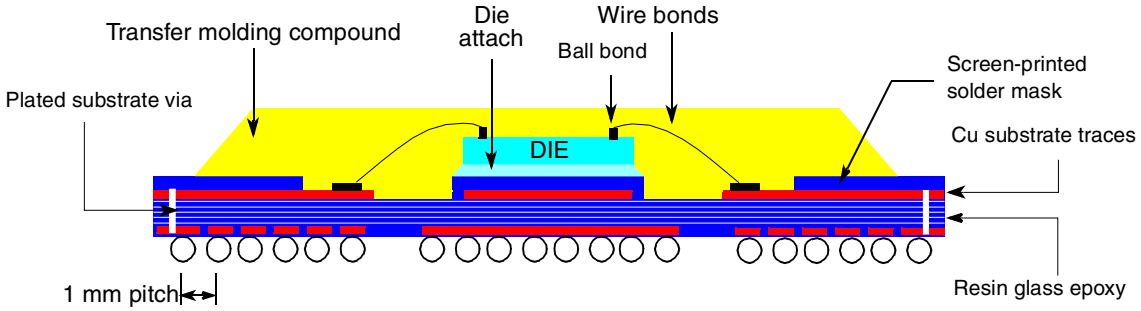
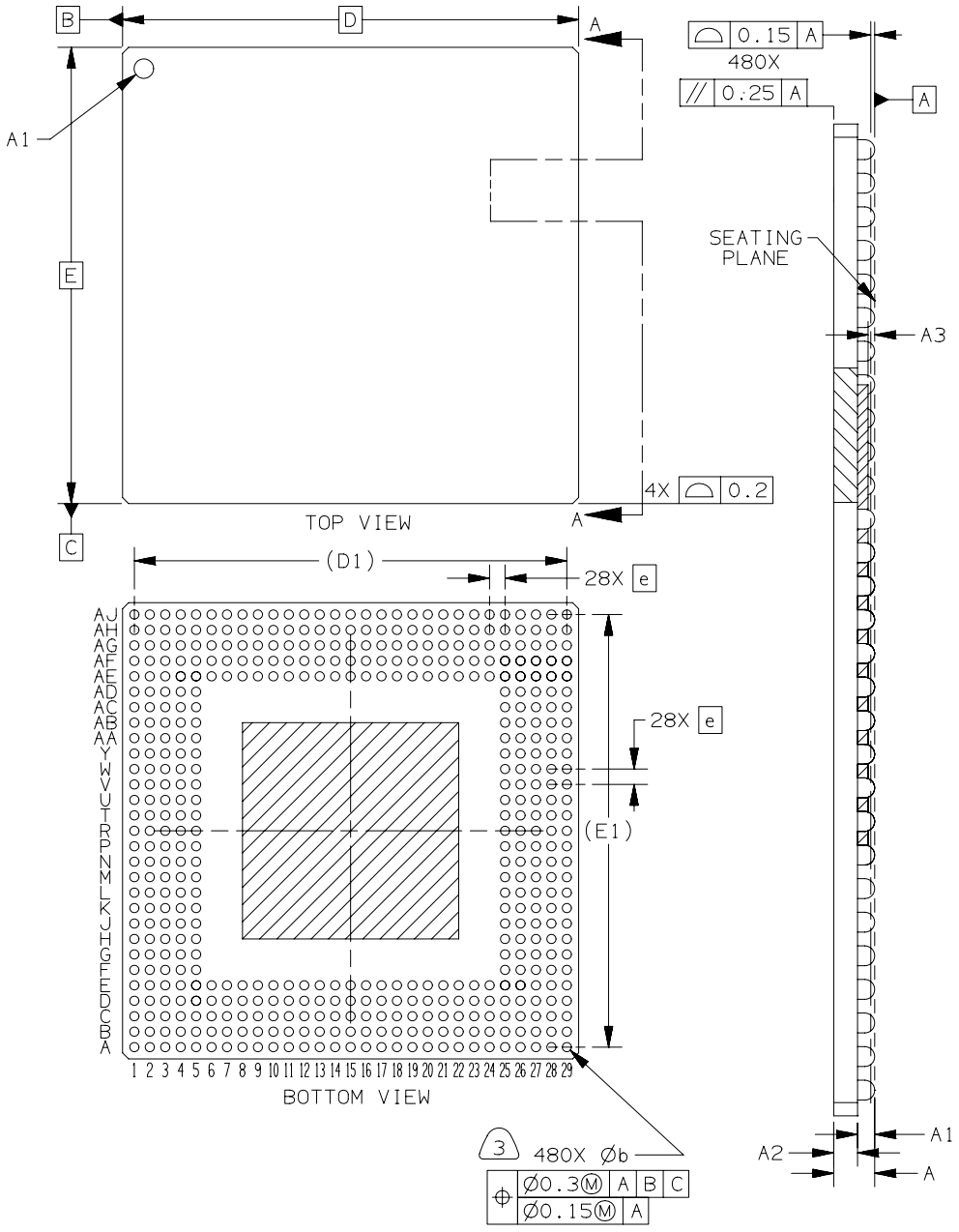


Figure 16. Side View of the PBGA Package Remove

9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA (ZU/VV) package. See Table 2, “HiP7 PowerQUICC II Device Packages.”



Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls.

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

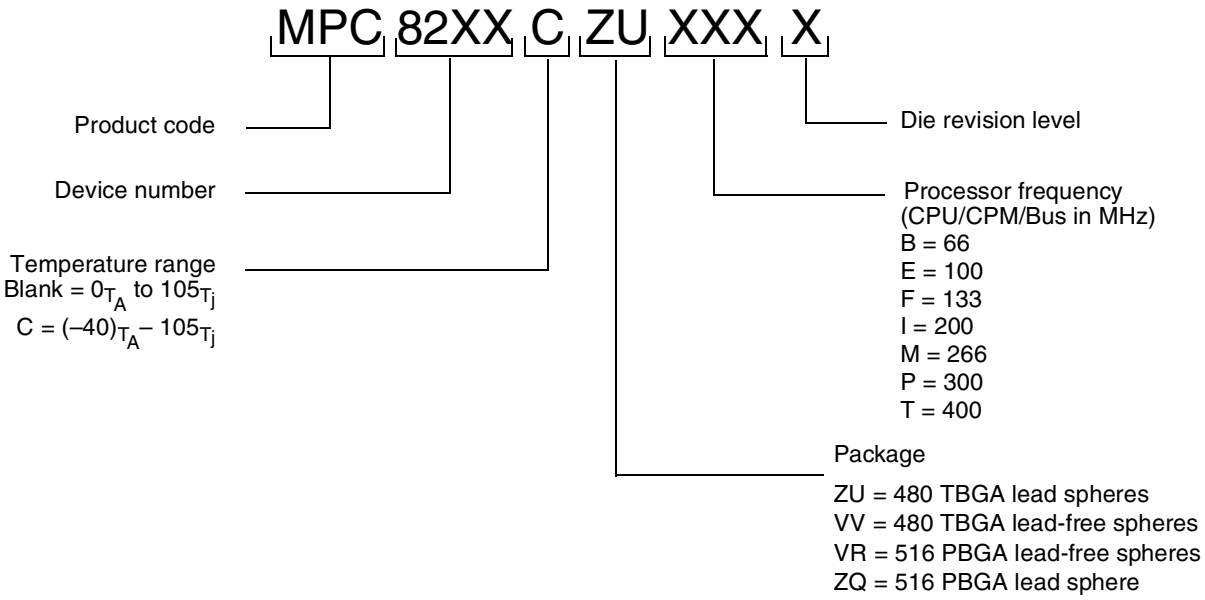


Figure 19. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 27. Document Revision History

Revision	Date	Substantive Changes
2	09/2011	In Figure 19, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
1.8	07/2007	• Updated the entire document, adding information on the VV package.
1.7	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.6	05/2006	• Table 11: Added text to clarify that Data Bus Parity is not supported at 66 Mhz. • Table 11: Added text to clarify that Data Bus ECC is supported at 66 Mhz • Table 11: Added note to DP pins to show it is not supported at 66 MHz • Table 12: Added note to support 1 ns hold time
1.5	03/2006	• Added Section 6.3, “JTAG Timings”

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
0.3	6/2003	• Removal of notes stating “no local bus” on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support. • References to “G2 core” changed to “G2_LE core.” See the *G2 Core Reference Manual* (G2CORERM/D). • Addition of VCCSYN to “Note” below Table 4, and to note 3 of Table 5 • Figure 2: New • Table 5: Addition of note 1 • Table 10: Addition of θ_{JB} and θ_{JC}. Modifications to ZU package values. • Table 12: Addition of various configurations, Modification of values. Addition of note 3. • Table 9: Addition of 66 MHZ and 100 MHz values. Addition of sp42a/sp43a. • Table 20: Addition of 66 MHZ and 100 MHz values • Table 12: sp30 values. sp33b @100 MHz value. Removal of previous note 2. Modification of current note 2. • Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes • Section 6.2: Addition of note on PCI timing • Table 18, Table 32, Table 33, Table 36, Table 37: Addition of note 1 concerning minimum operating frequencies • Addition of statement before clock tables about selection of clock configuration and input frequency • Table 23 and Table 25: Addition of note 1 to CPM pins
0.2	11/2002	Table 25, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 63)
0.1	—	Initial public release