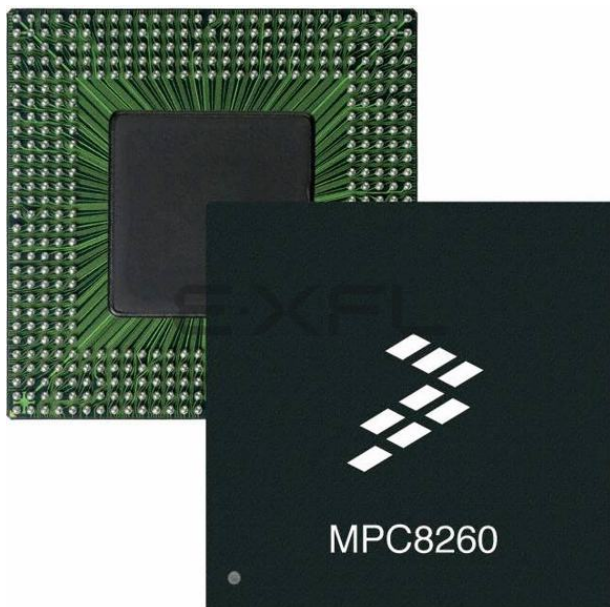




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	450MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8280vvupea

1 Overview

This table shows the functionality supported by each SoC in the MPC8280 family.

Table 1. MPC8280 PowerQUICC II Family Functionality

Functionality	Package ¹	SoCs			
		MPC8270		MPC8275	MPC8280
		480 TBGA	516 PBGA	516 PBGA	480 TBGA
Serial communications controllers (SCCs)		4	4	4	4
QUICC multi-channel controller (QMC)		—	—	—	—
Fast communication controllers (FCCs)		3	3	3	3
I-Cache (Kbyte)		16	16	16	16
D-Cache (Kbyte)		16	16	16	16
Ethernet (10/100)		3	3	3	3
UTOPIA II Ports		0	0	2	2
Multi-channel controllers (MCCs)		1	1	1	2
PCI bridge		Yes	Yes	Yes	Yes
Transmission convergence (TC) layer		—	—	—	Yes
Inverse multiplexing for ATM (IMA)		—	—	—	Yes
Universal serial bus (USB) 2.0 full/low rate		1	1	1	1
Security engine (SEC)		—	—	—	—

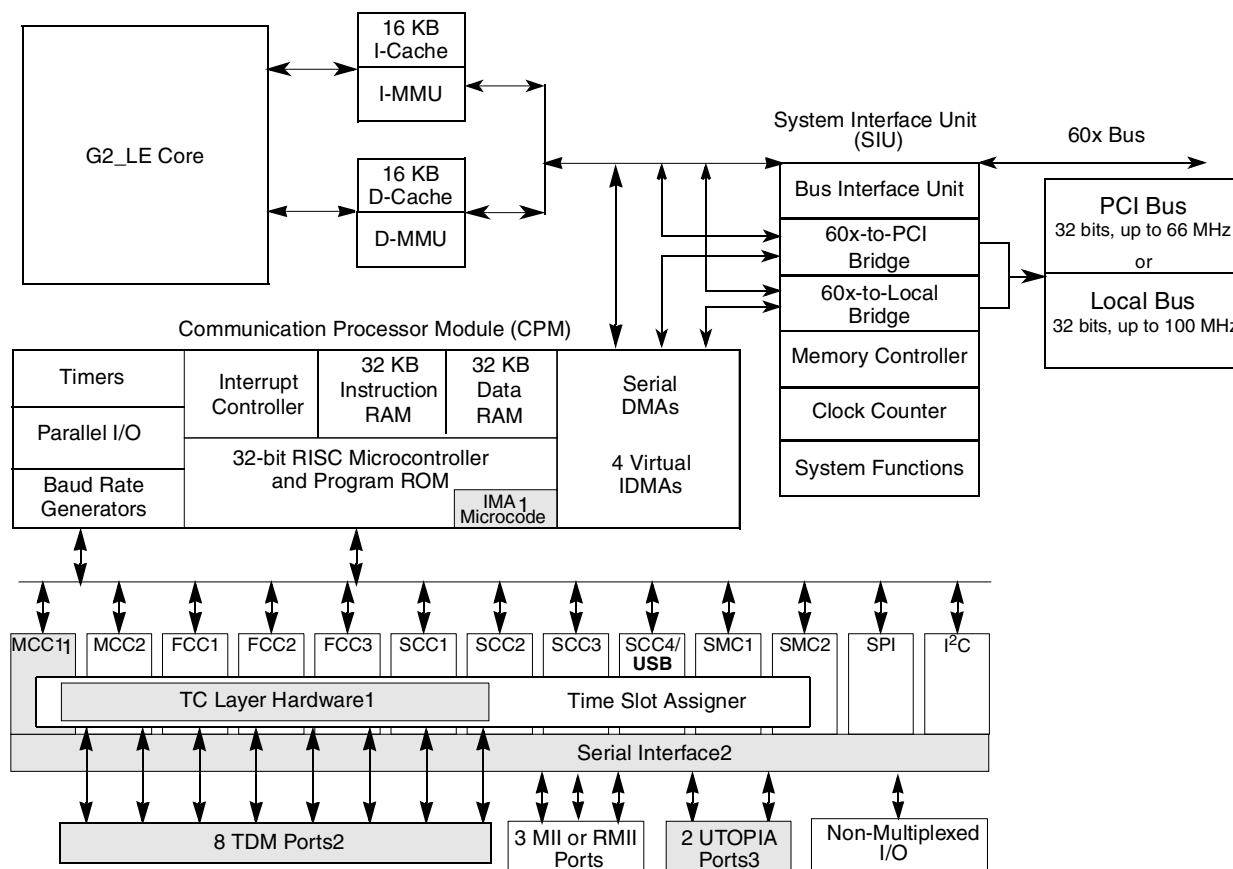
¹ See [Table 2](#).

Devices in the MPC8280 family are available in four packages—the standard ZU and VV packages and the alternate VR or ZQ packages—as shown in [Table 2](#). Note that throughout this document, references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Freescale sales office. For package ordering information, see [Section 10, “Ordering Information.”](#)

Table 2. HiP7 PowerQUICC II Device Packages

Code (Package)	ZU (480 TBGA—Leaded)	VV (480 TBGA—Lead Free)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8280	MPC8280	MPC8275VR	MPC8275ZQ
	MPC8270	MPC8270	MPC8270VR	MPC8270ZQ

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.



Notes:

¹ MPC8280 only (**not on MPC8270**, the VR package, nor the ZQ package)

² MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).

³ MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270**, MPC8270VR, nor MPC8270ZQ)

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
 - A core version of the EC603e microprocessor
 - System core microprocessor supporting frequencies of 166–450 MHz
 - Separate 16 KB data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm
 - Power Architecture®-compliant memory management unit (MMU)

- Common on-chip processor (COP) test interface
- High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
- Supports bus snooping
- Support for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
 - G2_LE core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
 - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
 - Programmable host bridge and agent
 - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- PCI bridge
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
 - PCI host bridge or peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI

- ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64 K external connections (no ATM support for the MPC8270)
 - Transparent
 - HDLC—Up to T3 rates (clear channel)
 - FCC2 can also be connected to the TC layer (MPC8280 only)
- Two multichannel controllers (MCCs) (one MCC on the MPC8270)
 - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
- Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BISYNC) communications
 - Transparent
- Universal serial bus (USB) controller
 - Supports USB 2.0 full/low rate compatible
 - USB host mode
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loopback mode for diagnostics (12 Mbps only)
 - Supports USB slave mode
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate
 - Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
 - Two serial management controllers (SMCs), identical to those of the MPC860

- ⁴ V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.
- ⁵ MPC8280, MPC8275VR, MPC8275ZQ only.

4 Thermal Characteristics

This table describes thermal characteristics for both the packages. See [Table 2](#) for information on a given SoC's package. Discussions of each characteristic are provided in [Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance,"](#) and [Section 4.5, "Experimental Determination."](#) For the these discussions, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

Table 6. Thermal Characteristics

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA	516 PBGA		
Junction to ambient—single-layer board ¹	$R_{\theta JA}$	16	27	°C/W	Natural convection
		11	21		1 m/s
Junction to ambient—four-layer board	$R_{\theta JA}$	12	19	°C/W	Natural convection
		9	16		1 m/s
Junction to board ²	$R_{\theta JB}$	6	11	°C/W	—
Junction to case ³	$R_{\theta JC}$	2	8	°C/W	—
Junction-to-package top ⁴	Ψ_{JT}	2	2	°C/W	—

¹ Assumes no thermal vias

² Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

³ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁴ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Table 8. Output Buffer Impedances¹

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27 ²
Local bus	45
Memory controller	45 or 27 ²
Parallel I/O	45
PCI	27

¹ These are typical values at 65° C. Impedance may vary by $\pm 25\%$ with process and temperature.

² On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45 Ω .
On all other revisions, impedance value is selected through the SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

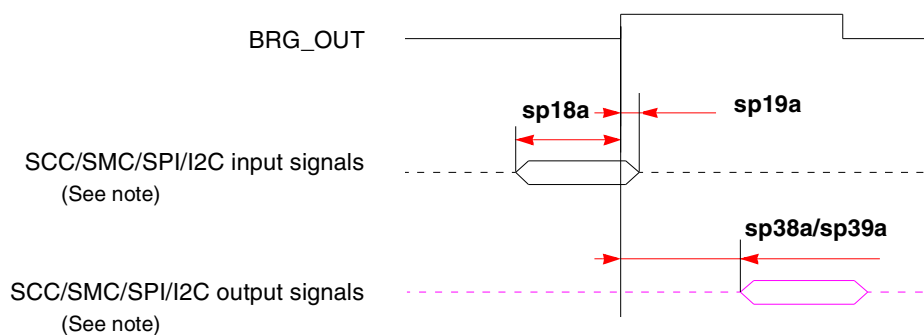
This table lists CPM output characteristics.

Table 9. AC Characteristics for CPM Outputs¹

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	0.5	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure shows the SCC/SMC/SPI/I²C internal clock.

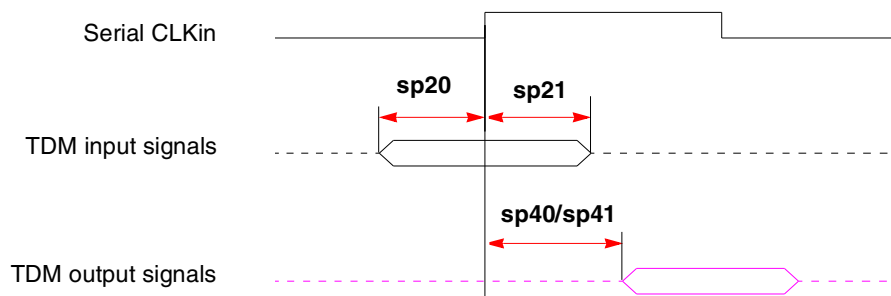


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

This figure shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

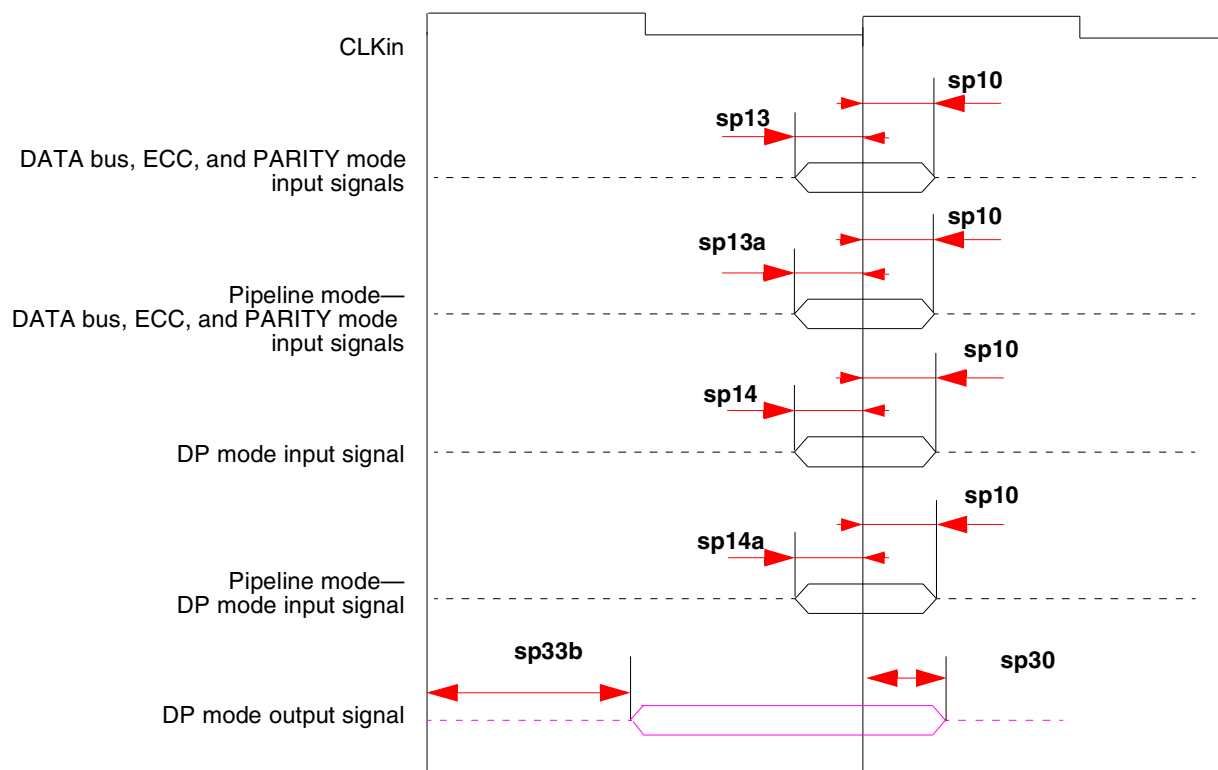


Figure 10. Parity Mode Diagram

This figure shows signal behavior in MEMC mode.

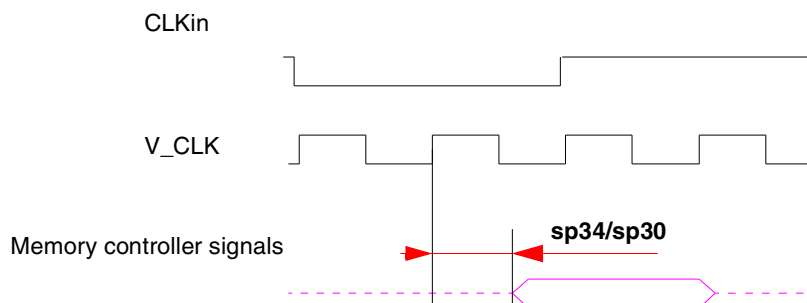


Figure 11. MEMC Mode Diagram

NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in [Table 15](#).

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0100_100	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
0101_000	30.0	50.0	5	150.0	250.0	2.5	150.0	250.0	2.5	60.0	100.0
0101_001	25.0	50.0	5	125.0	250.0	3	150.0	300.0	2.5	50.0	100.0
0101_010	25.0	50.0	5	125.0	250.0	3.5	175.0	350.0	2.5	50.0	100.0
0101_011	25.0	50.0	5	125.0	250.0	4	200.0	400.0	2.5	50.0	100.0
0101_100	25.0	50.0	5	125.0	250.0	4.5	225.0	450.0	2.5	50.0	100.0
0101_101	25.0	50.0	5	125.0	250.0	5	250.0	500.0	2.5	50.0	100.0
0101_110	25.0	50.0	5	125.0	250.0	5.5	275.0	550.0	2.5	50.0	100.0

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	25.0	50.0	5	125.0	250.0	3.5	218.8	437.5	2	62.5	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

¹ The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev 0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

This figure shows the pinout of the ZU and VV packages as viewed from the top surface.

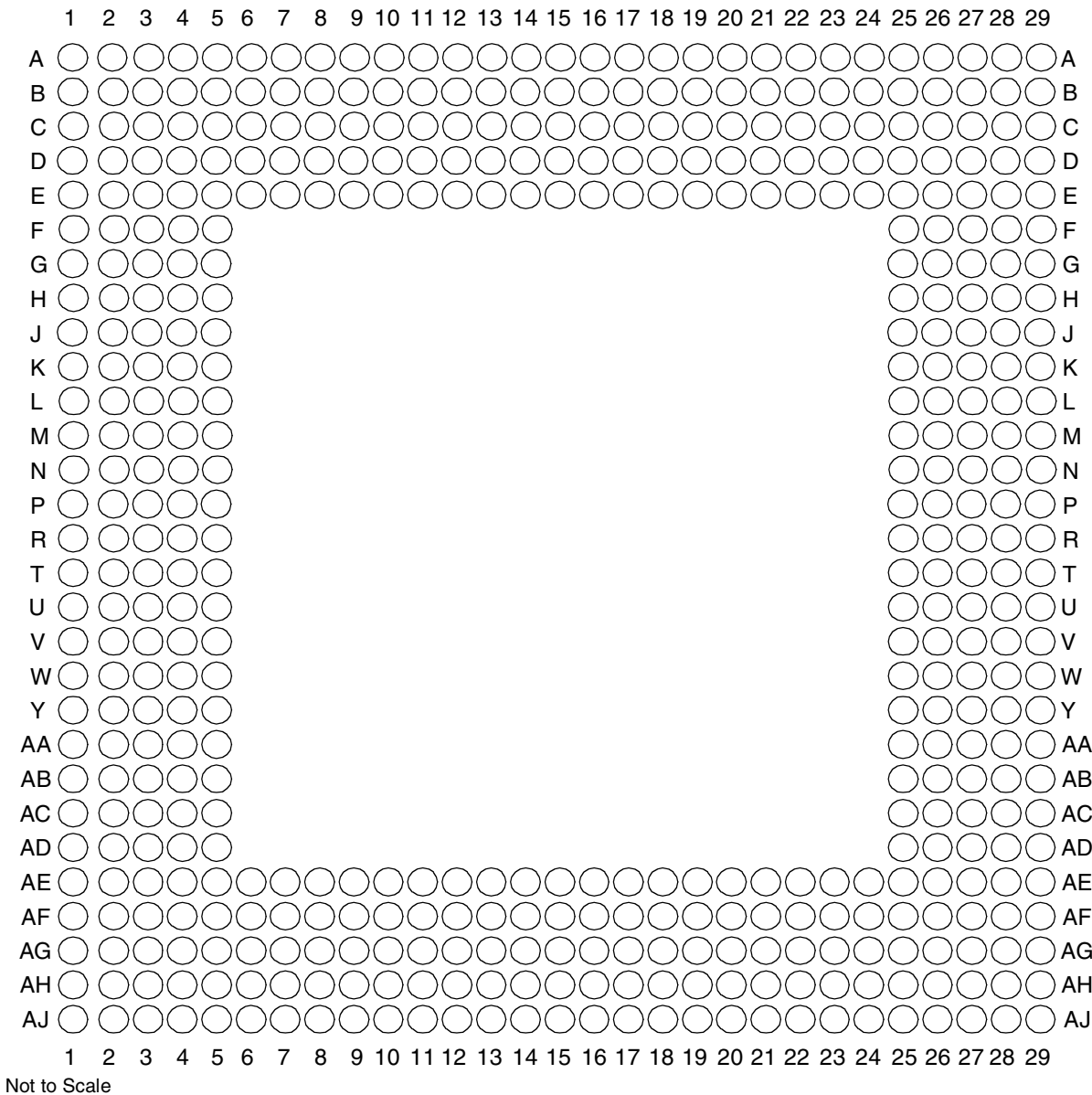


Figure 13. Pinout of the 480 TBGA Package (View from Top)

This table lists the pins of the MPC8280 and MPC8270, and [Table 24](#) defines conventions and acronyms used in this table.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{\text{BR}}$		W5
$\overline{\text{BG}}$		F4

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
ABB/IRQ2		E2
TS		E3
A0		G1
A1		H5
A2		H2
A3		H1
A4		J5
A5		J4
A6		J3
A7		J2
A8		J1
A9		K4
A10		K3
A11		K2
A12		K1
A13		L5
A14		L4
A15		L3
A16		L2
A17		L1
A18		M5
A19		N5
A20		N4
A21		N3
A22		N2
A23		N1
A24		P4
A25		P3
A26		P2
A27		P1
A28		R1
A29		R3
A30		R5

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
TBST		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
AACK		F3
ARTRY		E1
DBG		V1
DBB/IRQ3		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4
D16		D19
D17		D17

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PD20/ $\overline{\text{RTS4}}$ /TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	AJ14 ²
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	AH13 ²
PD22/RXD4/L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	AJ12 ²
PD23/ $\overline{\text{RTS3}}$ /TENA3	FCC1_UT16_RXD4/L1RSYNCD1	AE12 ²
PD24/TXD3	FCC1_UT16_RXD5/L1RXDD1	AF10 ²
PD25/RXD3	FCC1_UT16_TXD6/L1TXDD1	AG9 ²
PD26/ $\overline{\text{RTS2}}$ /TENA2	FCC1_UT16_RXD6/L1RSYNCC1	AH8 ²
PD27/TXD2	FCC1_UT16_RXD7/L1RXDC1	AG7 ²
PD28/RXD2	FCC1_UT16_TXD7/L1TXDC1	AE4 ²
PD29/ $\overline{\text{RTS1}}$ /TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	AG1 ²
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	AD4 ²
PD31/RXD1		AD2 ²
VCCSYN		AB3
VCCSYN1		B9
CLKIN2		AE11
SPARE4 ³		U5
PCI_MODE ⁴		AF25
SPARE6 ³		V4
No connect ⁵		AA1, AG4
I/O power		AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
TT1		B3
TT2		F8
TT3		A3
TT4		C3
$\overline{\text{TBST}}$		F5
TSIZ0		E3
TSIZ1		E2
TSIZ2		E1
TSIZ3		E4
$\overline{\text{AACK}}$		D3
$\overline{\text{ARTRY}}$		C2
$\overline{\text{DBG}}$		A14
$\overline{\text{DBB/IRQ3}}$		C15
D0		W4
D1		Y1
D2		V1
D3		P4
D4		N3
D5		K5
D6		J4
D7		G1
D8		AB1
D9		U4
D10		U2
D11		N6
D12		N1
D13		L1
D14		J5
D15		G3
D16		AA2
D17		W1
D18		T3
D19		T1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D53		J2
D54		H5
D55		F3
D56		V3
D57		R5
D58		R2
D59		N5
D60		L2
D61		J3
D62		H1
D63		F4
DP0/RSRV/EXT_BR2		AB3
IRQ1/DP1/EXT_BG2		W5
IRQ2/DP2/TLBISYNC/EXT_DBG2		AC2
IRQ3/DP3/CKSTP_OUT/EXT_BR3		AA3
IRQ4/DP4/CORE_SRESET/EXT_BG3		AD1
IRQ5/CINT/DP5/TBEN/EXT_DBG3		AC1
IRQ6/DP6/CSE0		AB2
IRQ7/DP7/CSE1		Y3
PSDVAL		D15
TA		Y4
TEA		D16
GBL/IRQ1		E15
CI/BADDR29/IRQ2		D14
WT/BADDR30/IRQ3		E14
L2_HIT/IRQ4		A17
CPU_BG/BADDR31/IRQ5/CINT		B14
CPU_DBG		F13
CPU_BR		B17
CS0		AC6
CS1		AD6
CS2		AE6
CS3		AB7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23 ²
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26 ²
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23 ²
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23 ²
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26 ²
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25 ²
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26 ²
PA26/FCC1_MII_RMII_RX_ER/ FCC1_RMII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25 ²
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRD_DV	FCC1_UT_RXSOC	C25 ²
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	C22 ²
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21 ²
PA30/FCC1_MII_CRD/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20 ²
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	A19 ²
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/FCC3_RTS	FCC2_UT8_RXD0	AD21 ²
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNDA2	FCC2_UT8_RXD1	AD22 ²
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22 ²
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26 ²
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23 ²
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26 ²
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26 ²
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25 ²
PB12/FCC3_MII_CRD/TXD2		W26 ²
PB13/FCC3_MII_COL/L1TXD1A2		W25 ²
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC31/CLK1/BRGO1		B20 ²
PD4/BRGO8/ $\overline{\text{FCC3_RTS}}$ /SMRXD2		AF23 ²
PD5/ $\overline{\text{DONE1}}$	FCC1_UT16_TXD3	AE23 ²
PD6/ $\overline{\text{DACK1}}$	FCC1_UT16_TXD4	AB21 ²
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AD23 ²
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AD26 ²
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22 ²
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1	AB24 ²
PD11/L1RQB2	FCC2_UT8_RXD0 L1GNTB1	Y23 ²
PD12		AA26 ²
PD13		W24 ²
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22 ²
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26 ²
PD16/SPIMISO	FCC1_UT_TXPRTY	T23 ²
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25 ²
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	P23 ²
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	N22 ²
PD20/ $\overline{\text{RTS4}}$ /TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	M25 ²
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	L25 ²
PD22/RXD4/L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	J26 ²
PD23/ $\overline{\text{RTS3}}$ /TENA3	FCC1_UT16_RXD4	K22 ²
PD24/TXD3	FCC1_UT16_RXD5	G25 ²
PD25/RXD3	FCC1_UT16_TXD6	H24 ²
PD26/ $\overline{\text{RTS2}}$ /TENA2	FCC1_UT16_RXD6	F24 ²

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA (VR/ZQ) packages.

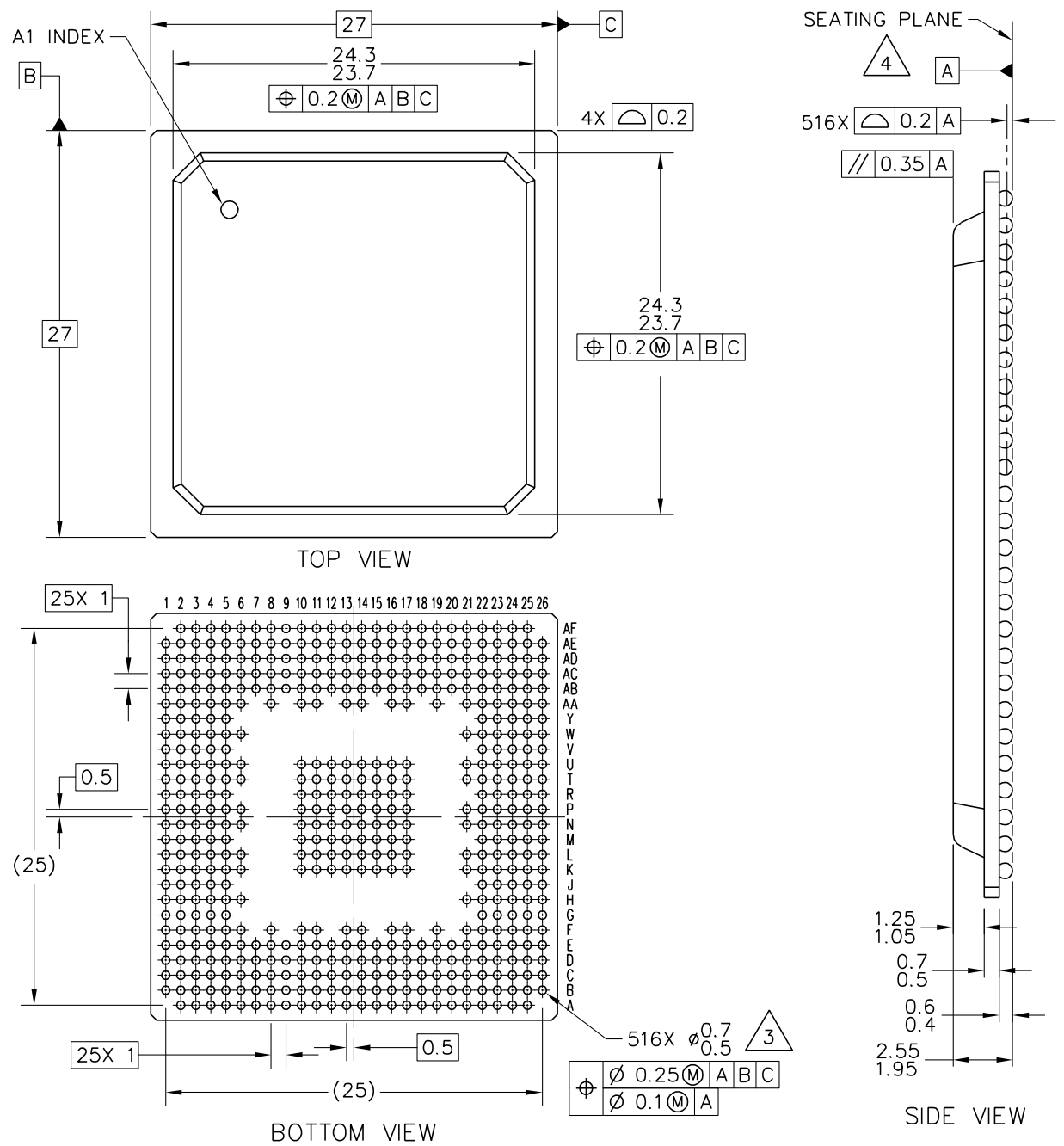


Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA