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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	450MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8280zuupea

1 Overview

This table shows the functionality supported by each SoC in the MPC8280 family.

Table 1. MPC8280 PowerQUICC II Family Functionality

Functionality	SoCs			
	MPC8270		MPC8275	MPC8280
Package[1]	480 TBGA	516 PBGA	516 PBGA	480 TBGA
Serial communications controllers (SCCs)	4	4	4	4
QUICC multi-channel controller (QMC)	—	—	—	—
Fast communication controllers (FCCs)	3	3	3	3
I-Cache (Kbyte)	16	16	16	16
D-Cache (Kbyte)	16	16	16	16
Ethernet (10/100)	3	3	3	3
UTOPIA II Ports	0	0	2	2
Multi-channel controllers (MCCs)	1	1	1	2
PCI bridge	Yes	Yes	Yes	Yes
Transmission convergence (TC) layer	—	—	—	Yes
Inverse multiplexing for ATM (IMA)	—	—	—	Yes
Universal serial bus (USB) 2.0 full/low rate	1	1	1	1
Security engine (SEC)	—	—	—	—

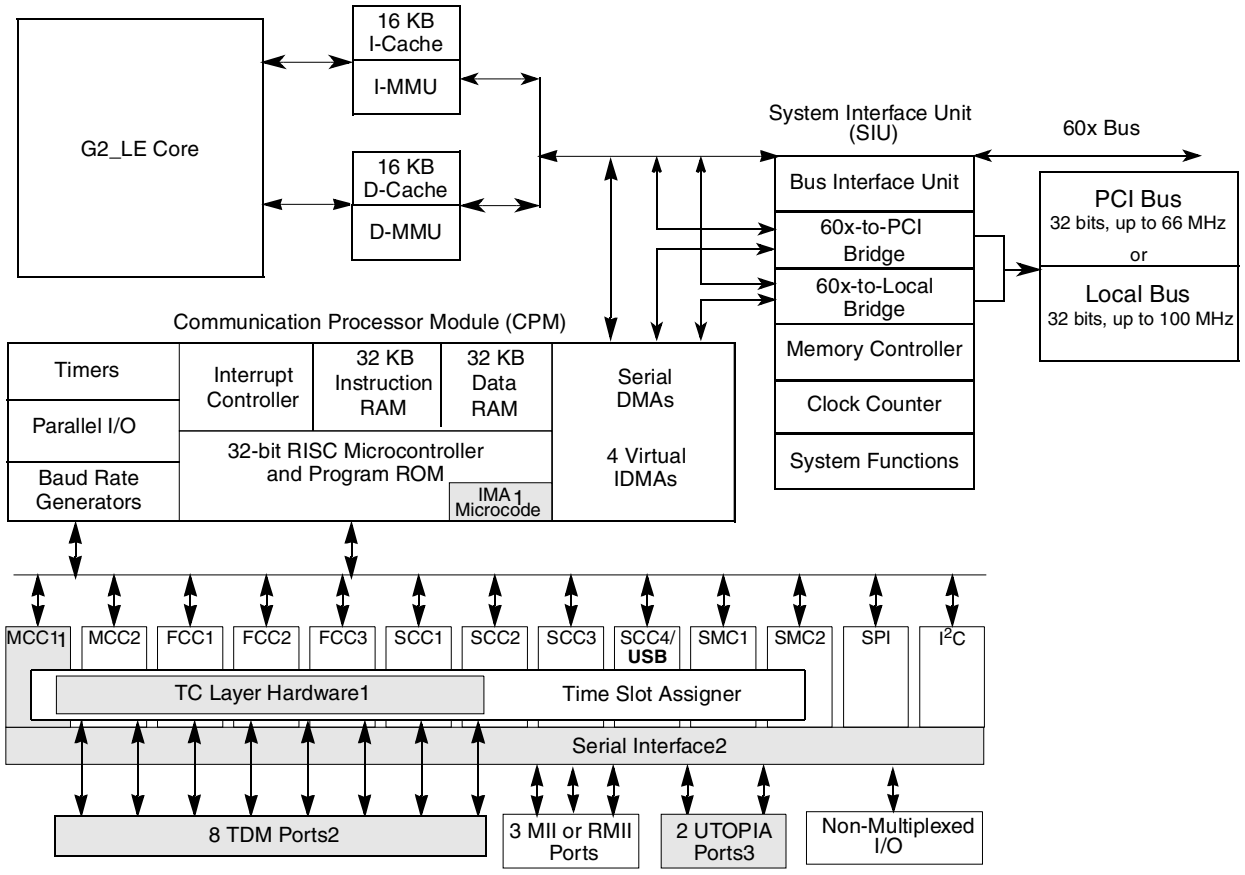
[1] See Table 2.

Devices in the MPC8280 family are available in four packages—the standard ZU and VV packages and the alternate VR or ZQ packages—as shown in Table 2. Note that throughout this document, references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Freescale sales office. For package ordering information, see Section 10, “Ordering Information.”

Table 2. HiP7 PowerQUICC II Device Packages

Code (Package)	ZU (480 TBGA—Leaded)	VV (480 TBGA—Lead Free)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8280	MPC8280	MPC8275VR	MPC8275ZQ
	MPC8270	MPC8270	MPC8270VR	MPC8270ZQ

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.



Notes:
[1] MPC8280 only (**not on MPC8270,** the VR package, nor the ZQ package)
[2] MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).
[3] MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270,** MPC8270VR, nor MPC8270ZQ)

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)

  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
  - Supports the I_2O standard
  - Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66.67/83.33/100 MHz, 3.3 V specification
  - 60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port
  - Uses the local bus signals, removing need for additional pins
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- 12-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x) and byte selects for 32-bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2_LE core through an on-chip 32 KB dual-port data RAM, an on-chip 32 KB dual-port instruction RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)

  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One I^2C controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
  - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

2 Operating Conditions

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	–0.3 – 2.25	V
PLL supply voltage[2]	VCCSYN	–0.3 – 2.25	V
I/O supply voltage[3]	VDDH	–0.3 – 4.0	V
Input voltage[4]	VIN	GND(–0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(–55) – (+150)	°C

[1] Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

This table lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions[1]

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.45 – 1.60	V
PLL supply voltage	VCCSYN	1.45 – 1.60	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T_j	105[2]	°C
Ambient temperature	T_A	0–70[2]	°C

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A} – 105_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

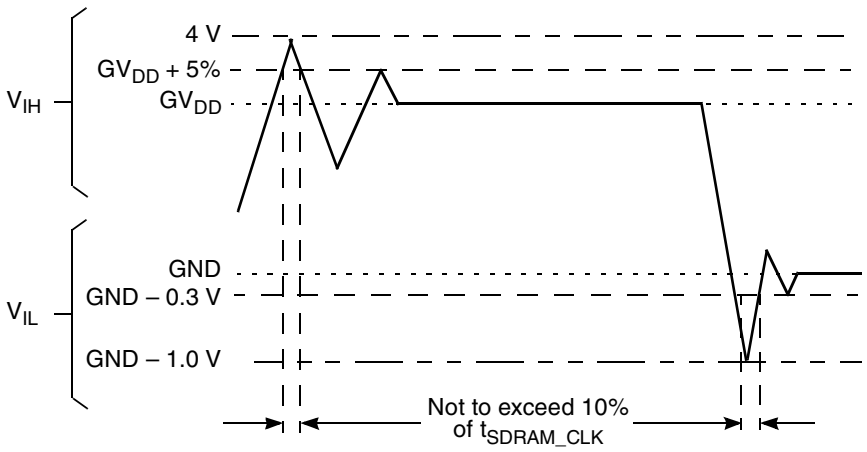


Figure 2. Overshoot/Undershoot Voltage

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Table 8. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27[2]
Local bus	45
Memory controller	45 or 27[2]
Parallel I/O	45
PCI	27

1 These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.

2 On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45 Ω.
On all other revisions, impedance value is selected through the SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

This table lists CPM output characteristics.

Table 9. AC Characteristics for CPM Outputs[1]

Spec Number		Characteristic	Value (ns)					
			Maximum Delay			Minimum Delay		
Max	Min		66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	0.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 10. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	2	2	2
sp20	sp21	TDM inputs/SI	5	5	5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	0.5	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

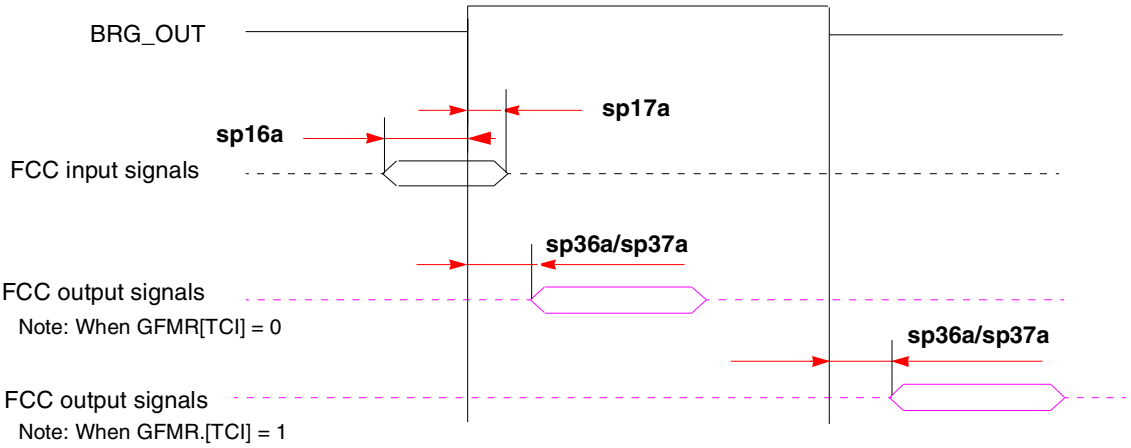


Figure 3. FCC Internal Clock Diagram

This figure shows the interaction of several bus signals.

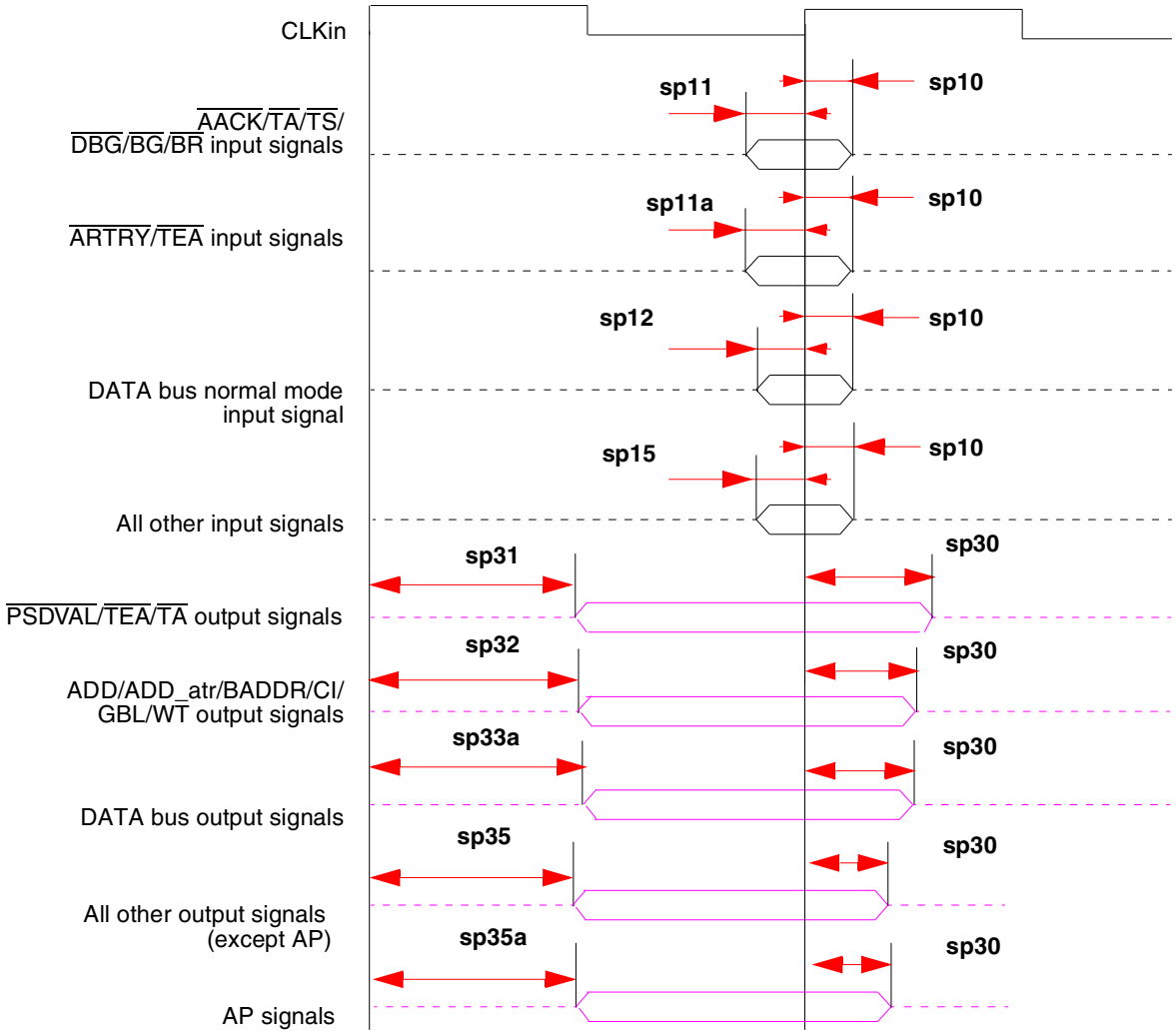


Figure 9. Bus Signals

Table 16. JTAG Timings[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Input hold times Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	 ns ns	 4, 7 4, 7
Output valid times Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 — —	 10 10	 ns ns	 5, 7 5, 7
Output hold times Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 1 1	 — —	 ns ns	 5, 7 5, 7
JTAG external clock to output high impedance Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 1 1	 10 10	 ns ns	 5, 6 5, 6

1 All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to t_{TCLK}.

5 Non-JTAG signal output timing with respect to t_{TCLK}.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

7 Clock Configuration Modes

This SoC includes the following clocking modes:

- Local
- PCI host
- PCI agent

The clocking mode is set according to the following input pins as shown in the following table:

- PCI_MODE
- PCI_CFG[0]
- PCI_MODCK

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0

Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0	266.6	4.5	225.0	300.0	4	50.0	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	25.0	50.0	5	125.0	250.0	3.5	218.8	437.5	2	62.5	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev 0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
$\overline{\text{TBST}}$		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
$\overline{\text{AACK}}$		F3
$\overline{\text{ARTRY}}$		E1
$\overline{\text{DBG}}$		V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4
D16		D19
D17		D17

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LSDWE/LGPL1/PCI_MODCKH1		C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2		E26
LSDCAS/LGPL3/PCI_MODCKH3		D25
LGTA/LUPMWAIT/LGPL4/LPBS		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
LWR		D28
L_A14/PAR		N27
L_A15/FRAME/SMI		T29
L_A16/TRDY		R27
L_A17/IRDY/CKSTP_OUT		R26
L_A18/STOP		R29
L_A19/DEVSEL		R28
L_A20/IDSEL		W29
L_A21/PERR		P28
L_A22/SERR		N26
L_A23/REQ0		AA27
L_A24/REQ1/HSEJSW		P29
L_A25/GNT0		AA26
L_A26/GNT1/HSLED		N25
L_A27/GNT2/HSENUM		AA25
L_A28/RST/CORE_SRESET		AB29
L_A29/INTA		AB28
L_A30/REQ2		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25[2]
PC6/FCC1_CD	FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25[2]
PC7/FCC1_CTS	FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24[2]
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USB_RN	FCC1_UT16_TXD0	Y24[2]
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	U22[2]
PC10/CD3/RENA3	FCC1_UT16_TXD2/FCC2_UT8_RXD3	V23[2]
PC11/CTS3/CLSN3/L1TXD3A2	FCC2_UT8_RXD2	U23[2]
PC12/CD2/RENA2	FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26[2]
PC13/CTS2/CLSN2	FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26[2]
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26[2]
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24[2]
PC16/CLK16/TIN4		M26[2]
PC17/CLK15/TIN3/BRGO8		L26[2]
PC18/CLK14/TGATE2		M24[2]
PC19/CLK13/BRGO7/SPICLK		L22[2]
PC20/CLK12/TGATE1/USB_OE		K25[2]
PC21/CLK11/BRGO6		J25[2]
PC22/CLK10/DONE1	FCC1_UT_TXPRTY	G26[2]
PC23/CLK9/BRGO5/DACK1		F26[2]
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	G24[2]
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25[2]
PC26/CLK6/TOUT3/TMCLK		G23[2]
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		B23[2]
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	FCC2_UT_RXADDR4	E22[2]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21[2]
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	D21[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC31/CLK1/BRGO1		B20[2]
PD4/BRGO8/FCC3_RTS/SMRXD2		AF23[2]
PD5/DONE1	FCC1_UT16_TXD3	AE23[2]
PD6/DACK1	FCC1_UT16_TXD4	AB21[2]
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AD23[2]
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AD26[2]
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22[2]
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1	AB24[2]
PD11/L1RQB2	FCC2_UT8_RXD0 L1GNTB1	Y23[2]
PD12		AA26[2]
PD13		W24[2]
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22[2]
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26[2]
PD16/SPIMISO	FCC1_UT_TXPRTY	T23[2]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25[2]
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	P23[2]
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	N22[2]
PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	M25[2]
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	L25[2]
PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	J26[2]
PD23/RTS3/TENA3	FCC1_UT16_RXD4	K22[2]
PD24/TXD3	FCC1_UT16_RXD5	G25[2]
PD25/RXD3	FCC1_UT16_TXD6	H24[2]
PD26/RTS2/TENA2	FCC1_UT16_RXD6	F24[2]

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

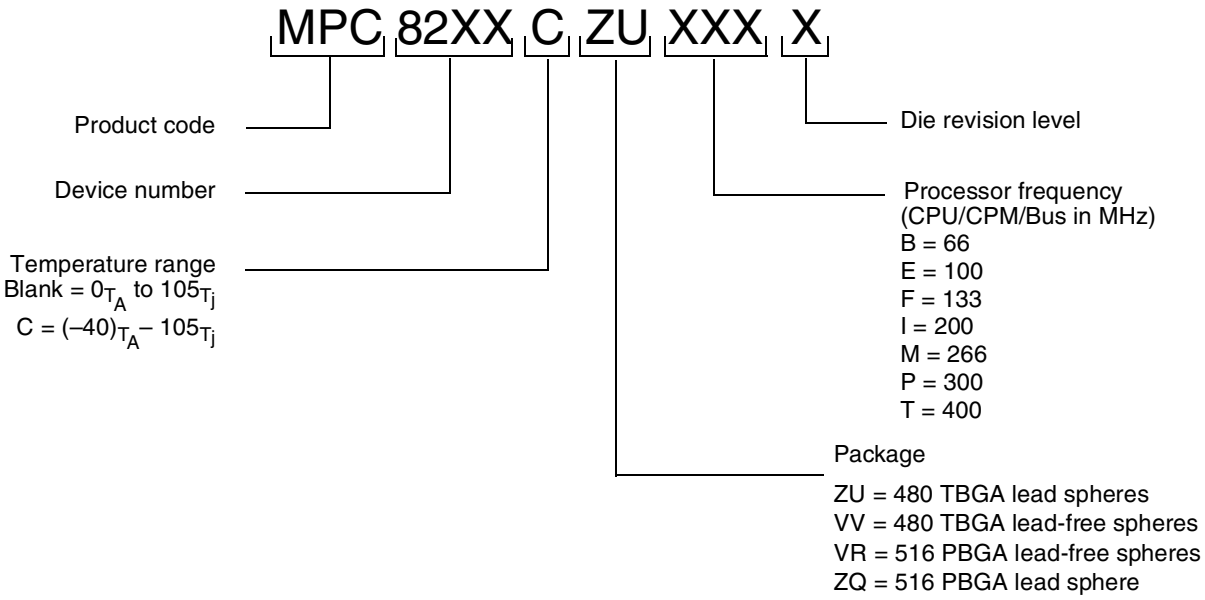


Figure 19. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 27. Document Revision History

Revision	Date	Substantive Changes
2	09/2011	In Figure 19, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
1.8	07/2007	• Updated the entire document, adding information on the VV package.
1.7	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.6	05/2006	• Table 11: Added text to clarify that Data Bus Parity is not supported at 66 Mhz. • Table 11: Added text to clarify that Data Bus ECC is supported at 66 Mhz • Table 11: Added note to DP pins to show it is not supported at 66 MHz • Table 12: Added note to support 1 ns hold time
1.5	03/2006	• Added Section 6.3, “JTAG Timings”

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.4	11/2005	• In Section 6.2, "SIU AC Characteristics", modified the note on CLKIN Jitter and Duty Cycle. • Modified Figure 17 to display all text.
1.3	01/2005	• Modification for correct display of assertion level ("overbar") for some signals
1.2	12/2004	• Section 2: removed voltage tracking note • Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset • Table 5: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pullup removed. • Table 5: Note 4 added regarding IIC compatibility • Section 4.2: New information about jumper-to-case thermal resistance • Section 4.3: New information about jumper-to-board thermal resistance • Section 4.4: New information about estimation with simulation • Section 4.6: Updated description of layout practices • Section 6: Added sentence providing derating factor • Section 6.1, "CPM AC Characteristics": added Note: Rise/Fall Time on CPM Input Pins • Table 9: updated values for following specs: sp42, sp43, sp42a • Table 20: updated values for following specs: sp16b, sp18b, sp20, sp22 • Section 6.2: added spread sprectrum clocking note • Table 11: combined specs sp11 and sp11a • Sections 7.2, 7.3: unit of ns added to Tval notes • Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
0.3	6/2003	• Removal of notes stating “no local bus” on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support. • References to “G2 core” changed to “G2_LE core.” See the *G2 Core Reference Manual* (G2CORERM/D). • Addition of VCCSYN to “Note” below Table 4, and to note 3 of Table 5 • Figure 2: New • Table 5: Addition of note 1 • Table 10: Addition of θ_{JB} and θ_{JC}. Modifications to ZU package values. • Table 12: Addition of various configurations, Modification of values. Addition of note 3. • Table 9: Addition of 66 MHZ and 100 MHz values. Addition of sp42a/sp43a. • Table 20: Addition of 66 MHZ and 100 MHz values • Table 12: sp30 values. sp33b @100 MHz value. Removal of previous note 2. Modification of current note 2. • Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes • Section 6.2: Addition of note on PCI timing • Table 18, Table 32, Table 33, Table 36, Table 37: Addition of note 1 concerning minimum operating frequencies • Addition of statement before clock tables about selection of clock configuration and input frequency • Table 23 and Table 25: Addition of note 1 to CPM pins
0.2	11/2002	Table 25, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 63)
0.1	—	Initial public release

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