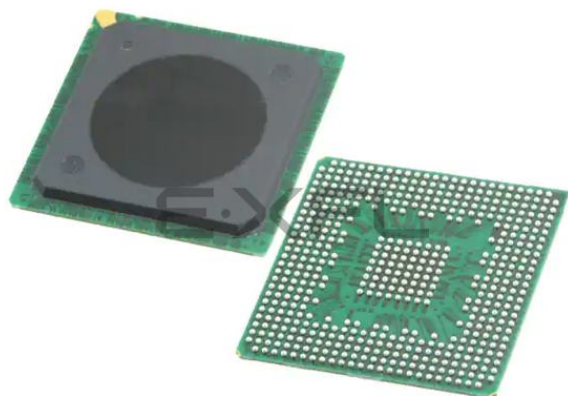




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8270cvmiba

- Common on-chip processor (COP) test interface
- High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
- Supports bus snooping
- Support for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
 - G2_LE core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
 - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
 - Programmable host bridge and agent
 - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- PCI bridge
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
 - PCI host bridge or peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI

Table 5. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}[0-7]/\overline{PSDDQM}[0-7]/\overline{PBS}[0-7]$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}$ $\overline{LWR}$ $\overline{MODCK}[1-3]/\overline{AP}[1-3]/\overline{TC}[0-2]/\overline{BNKSEL}[0-2]$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}$ $\overline{L_A15}/\overline{FRAME}/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}$ $\overline{L_A17}/\overline{IRDY}/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}$ $\overline{L_A19}/\overline{DEVSEL}$ $\overline{L_A20}/\overline{IDSEL}$ $\overline{L_A21}/\overline{PERR}$ $\overline{L_A22}/\overline{SERR}$ $\overline{L_A23}/\overline{REQ0}$ $\overline{L_A24}/\overline{REQ1}/\overline{HSEJSW}$ $\overline{L_A25}/\overline{GNT0}$ $\overline{L_A26}/\overline{GNT1}/\overline{HSLED}$ $\overline{L_A27}/\overline{GNT2}/\overline{HSENUM}$ $\overline{L_A28}/\overline{RST}/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTAL_A30}/\overline{REQ2}$ $\overline{L_A31}$ $\overline{LCL_D}[0-31]/\overline{AD}[0-31]$ $\overline{LCL_DP}[03]/\overline{C}/\overline{BE}[0-3]$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ $\overline{TDO}$ $\overline{QREQ}$	V_{OL}	—	0.4	V

¹ The default configuration of the CPM pins ($\overline{PA}[0-31]$, $\overline{PB}[4-31]$, $\overline{PC}[0-31]$, $\overline{PD}[4-31]$) is input. To prevent excessive DC current, either pull unused pins to GND or VDDH or configure them as outputs.

² TCK, TRST and PORESET have min $V_{IH} = 2.5\text{V}$.

³ The leakage current is measured for nominal VDDH, VCCSYN, and VDD.

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 10. AC Characteristics for CPM Inputs¹

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	2	2	2
sp20	sp21	TDM inputs/SI	5	5	5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	0.5	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

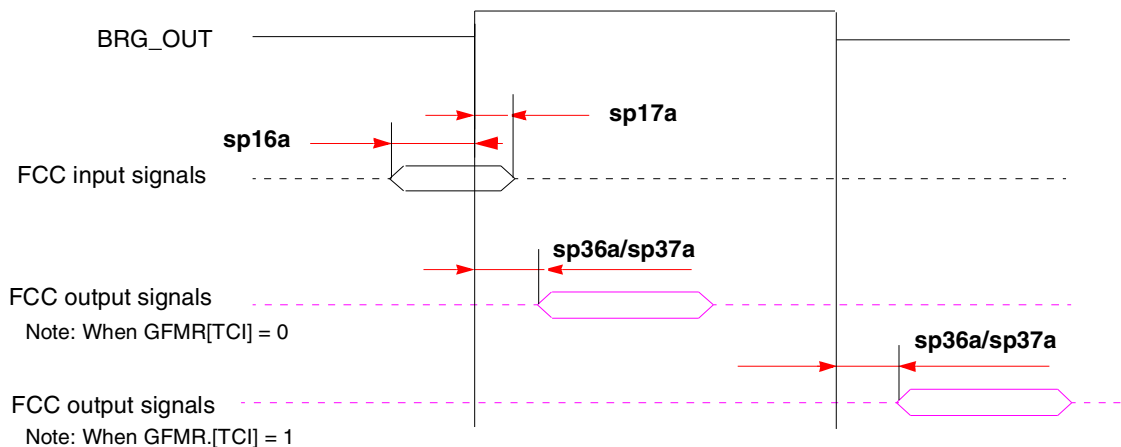
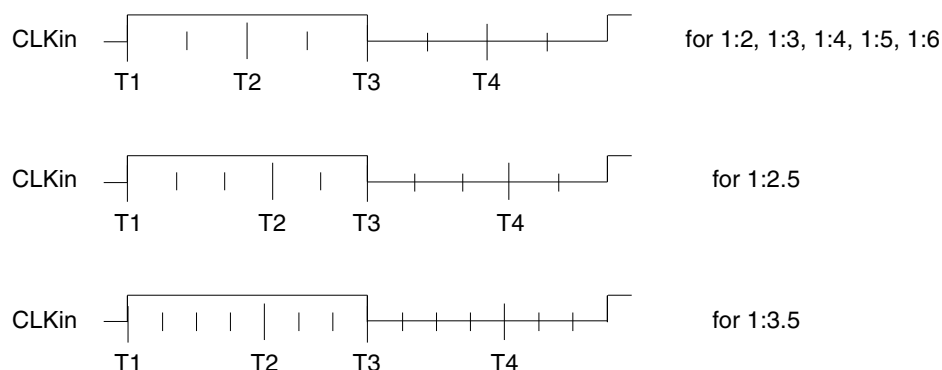


Figure 3. FCC Internal Clock Diagram

Table 15. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

This table is a representation of the information in [Table 15](#).


Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKIn's rising edge.

6.3 JTAG Timings

This table lists the JTAG timings.

Table 16. JTAG Timings¹

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	⁶
TRST assert time	t_{TRST}	25	—	ns	^{3, 6}
Input setup times Boundary-scan data TMS, TDI	t_{JTDVKH}	4	—	ns	^{4, 7}
	t_{JTIVKH}	4	—	ns	^{4, 7}

Table 16. JTAG Timings¹ (continued)

Parameter	Symbol ²	Min	Max	Unit	Notes
Input hold times Boundary-scan data TMS, TDI	t_{JTDXKH}	10	—	ns	4, 7
	t_{JTIXKH}	10	—	ns	4, 7
Output valid times Boundary-scan data TDO	t_{JTKLDV}	—	10	ns	5, 7
	t_{JTKLOV}	—	10	ns	5, 7
Output hold times Boundary-scan data TDO	t_{JTKLDX}	1	—	ns	5, 7
	t_{JTKLOX}	1	—	ns	5, 7
JTAG external clock to output high impedance Boundary-scan data TDO	t_{JTKLDZ}	1	10	ns	5, 6
	t_{JTKLOZ}	1	10	ns	5, 6

¹ All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

² The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

³ TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

⁴ Non-JTAG signal input timing with respect to t_{TCLK} .

⁵ Non-JTAG signal output timing with respect to t_{TCLK} .

⁶ Guaranteed by design.

⁷ Guaranteed by design and device characterization.

7 Clock Configuration Modes

This SoC includes the following clocking modes:

- Local
- PCI host
- PCI agent

The clocking mode is set according to the following input pins as shown in the following table:

- PCI_MODE
- PCI_CFG[0]
- PCI_MODCK

Table 17. SoC Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK ¹			
1	—	—	Local bus	—	Table 18
0	0	0	PCI host	50–66	Table 19
0	0	1		25–50	Table 20
0	1	0	PCI agent	50–66	Table 21
0	1	1		25–50	Table 22

¹ Determines PCI clock frequency range. See Section 7.2, “PCI Host Mode,” and Section 7.3, “PCI Agent Mode.”

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

7.1 Local Bus Mode

This table lists clock configurations for the SoC in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

Table 18. Clock Configurations for Local Bus Mode¹

Mode ²	Bus Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)	
	MODCK_H-MODCK[1:3]	Low		High	Low		High	Low
Default Modes (MODCK_H= 0000)								
0000_000	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0000_001	33.3	133.3	3	100.0	400.0	5	166.7	666.7
0000_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0000_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0000_100	60.0	167.0	2	120.0	334.0	2.5	150.0	417.5
0000_101	50.0	167.0	2	100.0	334.0	3	150.0	501.0
0000_110	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0000_111	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
Full Configuration Modes								
0001_000	50.0	167.0	2	100.0	334.0	4	200.0	668.0

Table 18. Clock Configurations for Local Bus Mode¹ (continued)

Mode ²	Bus Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)	
	Low	High		Low	High		Low	High
MODCK_H-MODCK[1:3]								
0001_001	50.0	167.0	2	100.0	334.0	5	250.0	835.0
0001_010	50.0	145.8	2	100.0	291.7	6	300.0	875.0
0001_011	Reserved							
0001_100	Reserved							
0001_101	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0001_110	33.3	133.3	3	100.0	400.0	5	166.7	666.7
1000_111	33.3	133.3	3	100.0	400.0	5.5	183.3	733.3
0001_111	33.3	133.3	3	100.0	400.0	6	200.0	800.0
0010_000	Reserved							
0010_001	Reserved							
0010_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0010_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0010_100	25.0	100.0	4	100.0	400.0	6	150.0	600.0
0010_101	25.0	100.0	4	100.0	400.0	7	175.0	700.0
0010_110	25.0	100.0	4	100.0	400.0	8	200.0	800.0
0010_111	Reserved							
0011_000	30.0	80.0	5	150.0	400.0	5	150.0	400.0
0011_001	25.0	80.0	5	125.0	400.0	6	150.0	480.0
0011_010	25.0	80.0	5	125.0	400.0	7	175.0	560.0
0011_011	25.0	80.0	5	125.0	400.0	8	200.0	640.0
0011_100	Reserved							
0011_101	Reserved							
0011_110	25.0	66.7	6	150.0	400.0	6	150.0	400.0
0011_111	25.0	66.7	6	150.0	400.0	7	175.0	466.7
0100_000	25.0	66.7	6	150.0	400.0	8	200.0	533.3
0101_101	75.0	167.0	2	150.0	334.0	2	166.7	334.0
0101_110	60.0	167.0	2	120.0	334.0	2.5	166.7	417.5
0101_111	50.0	167.0	2	100.0	334.0	3	200.0	501.0

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	Bus Clock ⁴ (MHz)		CPM Multiplication Factor ⁵	CPM Clock (MHz)		CPU Multiplication Factor ⁶	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0

- ² As shown in [Table 17](#), PCI_MODCK determines the PCI clock range. See [Table 20](#) for higher range configurations.
- ³ MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
- ⁴ CPM multiplication factor = CPM clock/PCI clock
- ⁵ CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This section provides the pin assignments and pinout lists for both HiP7 PowerQUICC II packages.

8.1 ZU and VV Packages—MPC8280 and MPC8270

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, see [Section 8.2, “VR and ZQ Packages—MPC8275 and MPC8270.”](#)

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
ABB/IRQ2		E2
TS		E3
A0		G1
A1		H5
A2		H2
A3		H1
A4		J5
A5		J4
A6		J3
A7		J2
A8		J1
A9		K4
A10		K3
A11		K2
A12		K1
A13		L5
A14		L4
A15		L3
A16		L2
A17		L1
A18		M5
A19		N5
A20		N4
A21		N3
A22		N2
A23		N1
A24		P4
A25		P3
A26		P2
A27		P1
A28		R1
A29		R3
A30		R5

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LSDWE/LGPL1/PCI_MODCKH1		C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2		E26
LSDCAS/LGPL3/PCI_MODCKH3		D25
LGTA/LUPMWAIT/LGPL4/LPBS		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
LWR		D28
L_A14/PAR		N27
L_A15/FRAME/SMI		T29
L_A16/TRDY		R27
L_A17/IRDY/CKSTP_OUT		R26
L_A18/STOP		R29
L_A19/DEVSEL		R28
L_A20/IDSEL		W29
L_A21/PERR		P28
L_A22/SERR		N26
L_A23/REQ0		AA27
L_A24/REQ1/HSEJSW		P29
L_A25/GNT0		AA26
L_A26/GNT1/HSLED		N25
L_A27/GNT2/HSENUM		AA25
L_A28/RST/CORE_SRESET		AB29
L_A29/INTA		AB28
L_A30/REQ2		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24 ²
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24 ²
PB12/FCC3_MII_CRS/TXD2	L1CLKOB1/L1RSYNCC1	AG22 ²
PB13/FCC3_MII_COL/L1TXD1A2	L1RQB1/L1TSYNCC1/L1GNTC1	AH21 ²
PB14/FCC3_MII_RMII_TX_EN/RXD3	L1RXDC1	AG20 ²
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19 ²
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18 ²
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV	L1RQA1	AJ17 ²
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14 ²
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13 ²
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12 ²
PB21/FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11 ²
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16 ²
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15 ²
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9 ²
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9 ²
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7 ²
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6 ²
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/FCC2_RTS/ L1TSYNCB2/L1GNTB2/TXD1		AE3 ²
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2 ²
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5 ²
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D20		M2
D21		K2
D22		J1
D23		G4
D24		U5
D25		T5
D26		P5
D27		P3
D28		M3
D29		K3
D30		H2
D31		G5
D32		AA1
D33		V2
D34		U1
D35		P2
D36		M4
D37		K4
D38		H3
D39		F2
D40		Y2
D41		U3
D42		T2
D43		N2
D44		M5
D45		K1
D46		H4
D47		F1
D48		W2
D49		T4
D50		R3
D51		N4
D52		M1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D53		J2
D54		H5
D55		F3
D56		V3
D57		R5
D58		R2
D59		N5
D60		L2
D61		J3
D62		H1
D63		F4
DP0/RSRV/EXT_BR2		AB3
IRQ1/DP1/EXT_BG2		W5
IRQ2/DP2/TLBISYNC/EXT_DBG2		AC2
IRQ3/DP3/CKSTP_OUT/EXT_BR3		AA3
IRQ4/DP4/CORE_SRESET/EXT_BG3		AD1
IRQ5/CINT/DP5/TBEN/EXT_DBG3		AC1
IRQ6/DP6/CSE0		AB2
IRQ7/DP7/CSE1		Y3
PSDVAL		D15
TA		Y4
TEA		D16
GBL/IRQ1		E15
CI/BADDR29/IRQ2		D14
WT/BADDR30/IRQ3		E14
L2_HIT/IRQ4		A17
CPU_BG/BADDR31/IRQ5/CINT		B14
CPU_DBG		F13
CPU_BR		B17
CS0		AC6
CS1		AD6
CS2		AE6
CS3		AB7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
LCL_D11/AD11		AC13
LCL_D12/AD12		AC12
LCL_D13/AD13		AB13
LCL_D14/AD14		AD12
LCL_D15/AD15		AF14
LCL_D16/AD16		AF17
LCL_D17/AD17		AE16
LCL_D18/AD18		AD16
LCL_D19/AD19		AC16
LCL_D20/AD20		AB16
LCL_D21/AD21		AF18
LCL_D22/AD22		AE17
LCL_D23/AD23		AD17
LCL_D24/AD24		AB17
LCL_D25/AD25		AE18
LCL_D26/AD26		AD18
LCL_D27/AD27		AC18
LCL_D28/AD28		AE19
LCL_D29/AD29		AF20
LCL_D30/AD30		AD19
LCL_D31/AD31		AB18
LCL_DP0/C0/ $\overline{\text{BE}}0$		AE12
LCL_DP1/C1/ $\overline{\text{BE}}1$		AA13
LCL_DP2/C2/ $\overline{\text{BE}}2$		AC15
LCL_DP3/C3/ $\overline{\text{BE}}3$		AF19
$\overline{\text{IRQ}}0/\overline{\text{NMI_OUT}}$		A11
$\overline{\text{IRQ}}7/\overline{\text{INT_OUT/APE}}$		E5
$\overline{\text{TRST}}^1$		F22
TCK		A24
TMS		C24
TDI		A25
TDO		B24
$\overline{\text{TRIS}}$		C19

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25 ²
PC6/FCC1_CD	FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25 ²
PC7/FCC1_CTS	FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24 ²
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USB_RN	FCC1_UT16_TXD0	Y24 ²
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	U22 ²
PC10/CD3/RENA3	FCC1_UT16_TXD2/FCC2_UT8_RXD3	V23 ²
PC11/CTS3/CLSN3/L1TXD3A2	FCC2_UT8_RXD2	U23 ²
PC12/CD2/RENA2	FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26 ²
PC13/CTS2/CLSN2	FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26 ²
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26 ²
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24 ²
PC16/CLK16/TIN4		M26 ²
PC17/CLK15/TIN3/BRGO8		L26 ²
PC18/CLK14/TGATE2		M24 ²
PC19/CLK13/BRGO7/SPICLK		L22 ²
PC20/CLK12/TGATE1/USB_OE		K25 ²
PC21/CLK11/BRGO6		J25 ²
PC22/CLK10/DONE1	FCC1_UT_TXPRTY	G26 ²
PC23/CLK9/BRGO5/DACK1		F26 ²
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	G24 ²
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25 ²
PC26/CLK6/TOUT3/TMCLK		G23 ²
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		B23 ²
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	FCC2_UT_RXADDR4	E22 ²
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21 ²
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	D21 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PD27/TXD2	FCC1_UT16_RXD7	H22 ²
PD28/RXD2	FCC1_UT16_TXD7	B22 ²
PD29/RTS1/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	D22 ²
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	C21 ²
PD31/RXD1		E19 ²
VCCSYN		D19
VCCSYN1		K6
CLKIN2		K21
SPARE4 ³		C14
PCI_MODE ⁴		AD24
SPARE6 ³		B15
No connect ⁵		E17, C23
I/O power		E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9
Core Power		L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground		B18 ⁶ , A18 ⁷ , A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

¹ Should be tied to VDDH via a 2K Ω external pull-up resistor.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

- ³ Must be pulled down or left floating.
- ⁴ If PCI is not desired, must be pulled up or left floating.
- ⁵ Sphere is not connected to die.
- ⁶ GNDSYN (B18): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8275/MPC8270. New designs must connect B18 to GND and follow the suggestions in [Section 4.6, "Layout Practices."](#) Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.
- ⁷ XFC (A18) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8275/MPC8270 because there is no need for external capacitor to operate the PLL. New designs should connect A18 (XFC) pin to GND. Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to the current capacitor.

9 Package Description

This figure shows the side profile of the TBGA package to indicate the direction of the top surface view.

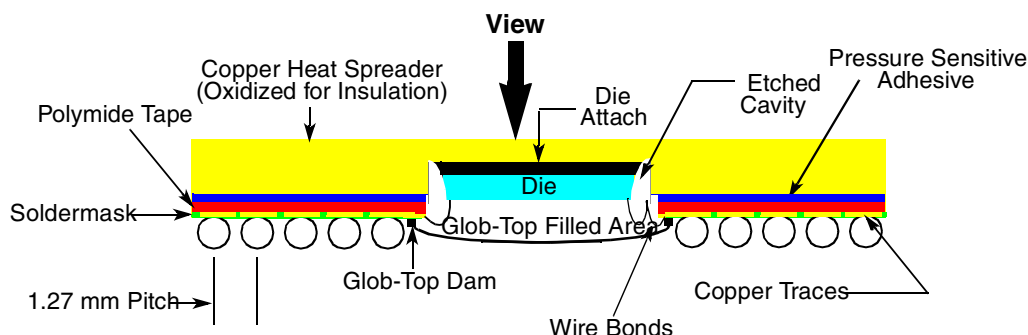


Figure 15. Side View of the TBGA Package

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

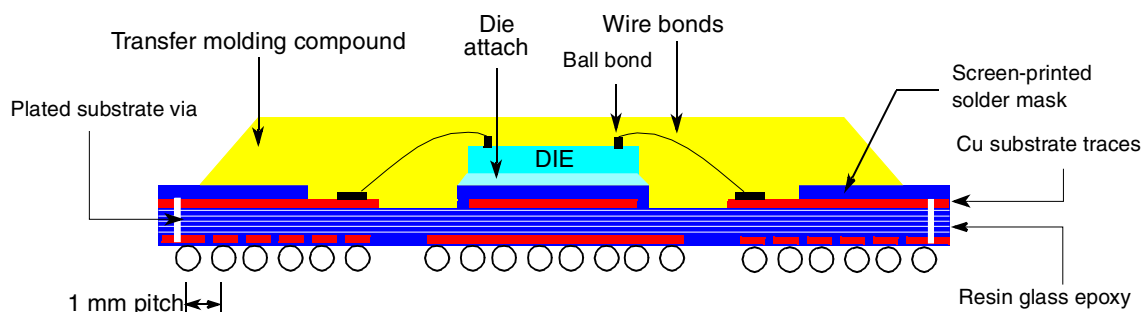


Figure 16. Side View of the PBGA Package Remove

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

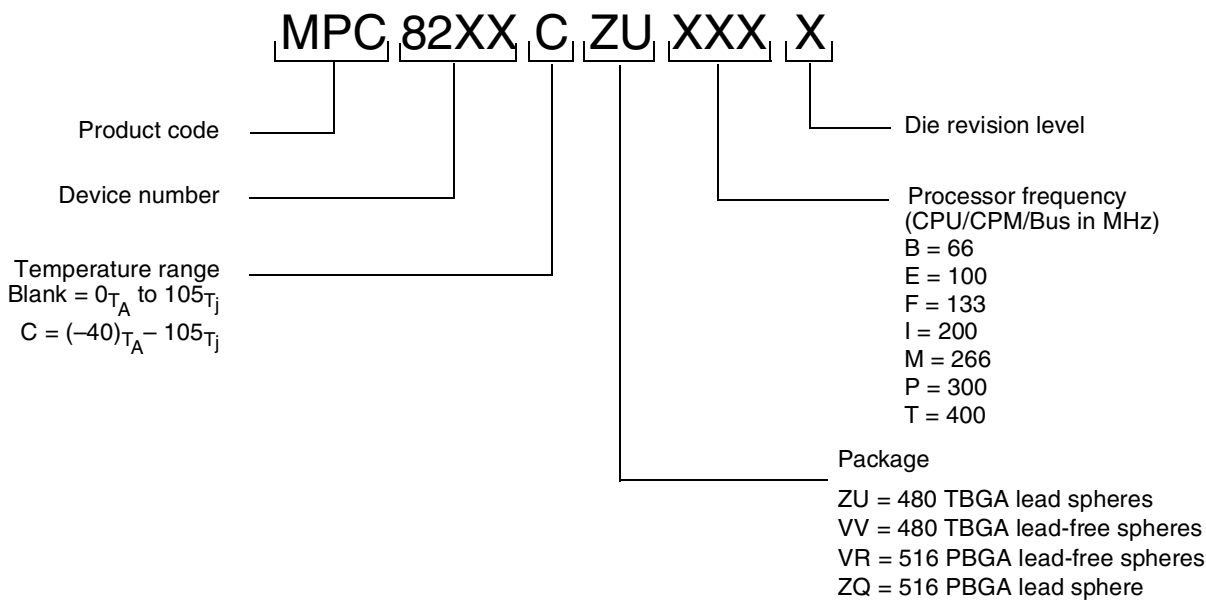


Figure 19. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 27. Document Revision History

Revision	Date	Substantive Changes
2	09/2011	In Figure 19 , "Freescale Part Number Key," added speed decoding information below processor frequency information.
1.8	07/2007	Updated the entire document, adding information on the VV package.
1.7	12/2006	Section 6, "AC Electrical Characteristics," removed deratings statement and clarified AC timing descriptions.
1.6	05/2006	Table 11: Added text to clarify that Data Bus Parity is not supported at 66 Mhz. Table 11: Added text to clarify that Data Bus ECC is supported at 66 Mhz Table 11: Added note to DP pins to show it is not supported at 66 MHz Table 12: Added note to support 1 ns hold time
1.5	03/2006	Added Section 6.3, "JTAG Timings"

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.4	11/2005	- In Section 6.2, "SIU AC Characteristics", modified the note on CLKIN Jitter and Duty Cycle. - Modified Figure 17 to display all text.
1.3	01/2005	Modification for correct display of assertion level ("overbar") for some signals
1.2	12/2004	- Section 2: removed voltage tracking note Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset Table 5: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pullup removed. Table 5: Note 4 added regarding IIC compatibility - Section 4.2: New information about jumper-to-case thermal resistance - Section 4.3: New information about jumper-to-board thermal resistance - Section 4.4: New information about estimation with simulation - Section 4.6: Updated description of layout practices - Section 6: Added sentence providing derating factor - Section 6.1, "CPM AC Characteristics": added Note: Rise/Fall Time on CPM Input Pins Table 9: updated values for following specs: sp42, sp43, sp42a - Table 20: updated values for following specs: sp16b, sp18b, sp20, sp22 - Section 6.2: added spread spectrum clocking note Table 11: combined specs sp11 and sp11a - Sections 7.2, 7.3: unit of ns added to Tval notes Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.