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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

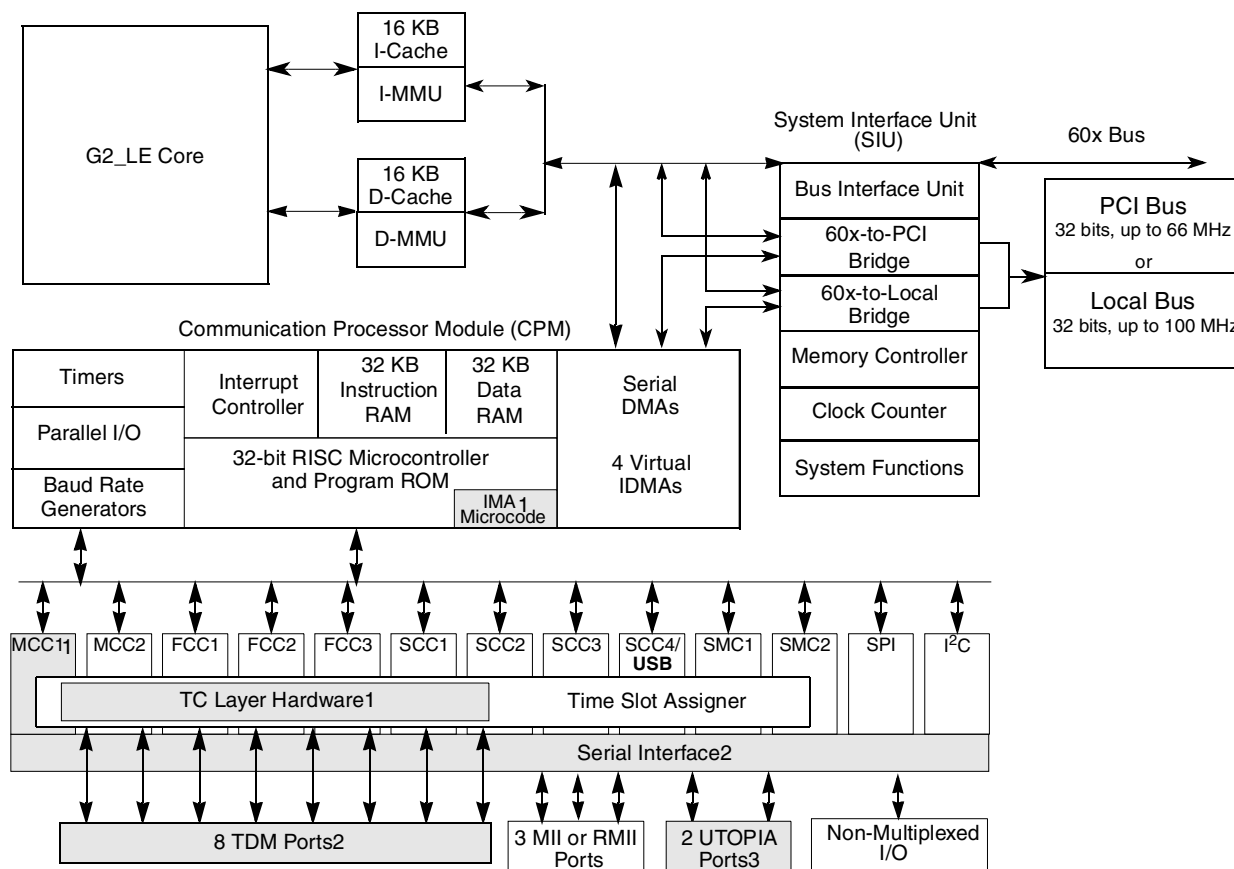
Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8270czqmiba

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.



Notes:

¹ MPC8280 only (**not on MPC8270**, the VR package, nor the ZQ package)

² MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).

³ MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270**, MPC8270VR, nor MPC8270ZQ)

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
 - A core version of the EC603e microprocessor
 - System core microprocessor supporting frequencies of 166–450 MHz
 - Separate 16 KB data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm
 - Power Architecture®-compliant memory management unit (MMU)

- Common on-chip processor (COP) test interface
- High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
- Supports bus snooping
- Support for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
 - G2_LE core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
 - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
 - Programmable host bridge and agent
 - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- PCI bridge
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
 - PCI host bridge or peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI

- Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
- Transparent
- UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One I²C controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
 - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
 - 2,048 bytes of SI RAM
 - Bit or byte resolution
 - Independent transmit and receive routing, frame synchronization
 - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers
- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

2 Operating Conditions

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	–0.3 – 2.25	V
PLL supply voltage ²	VCCSYN	–0.3 – 2.25	V
I/O supply voltage ³	VDDH	–0.3 – 4.0	V
Input voltage ⁴	VIN	GND(–0.3) – 3.6	V
Junction temperature	T _j	120	°C
Storage temperature range	T _{STG}	(–55) – (+150)	°C

¹ Absolute maximum ratings are stress ratings only; functional operation (see [Table 4](#)) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 10. AC Characteristics for CPM Inputs¹

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	2	2	2
sp20	sp21	TDM inputs/SI	5	5	5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	0.5	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

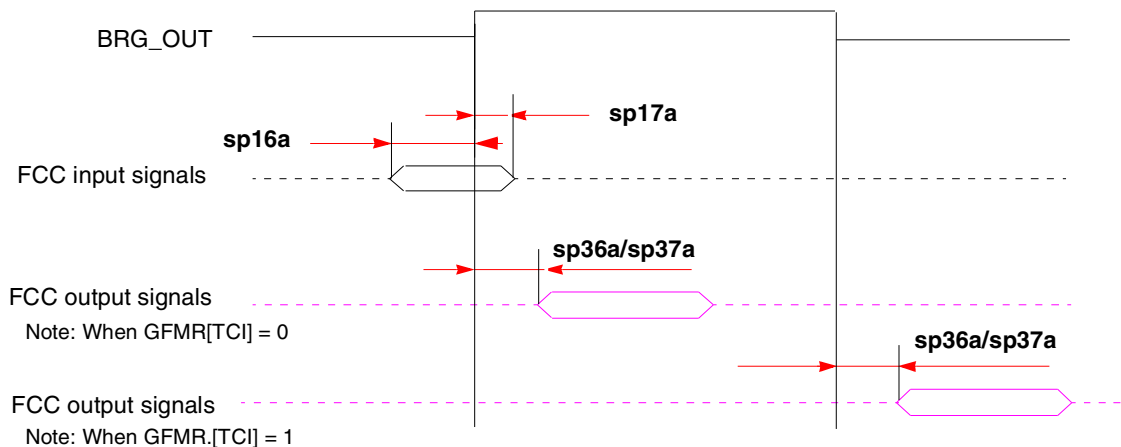


Figure 3. FCC Internal Clock Diagram

This figure shows the FCC external clock.

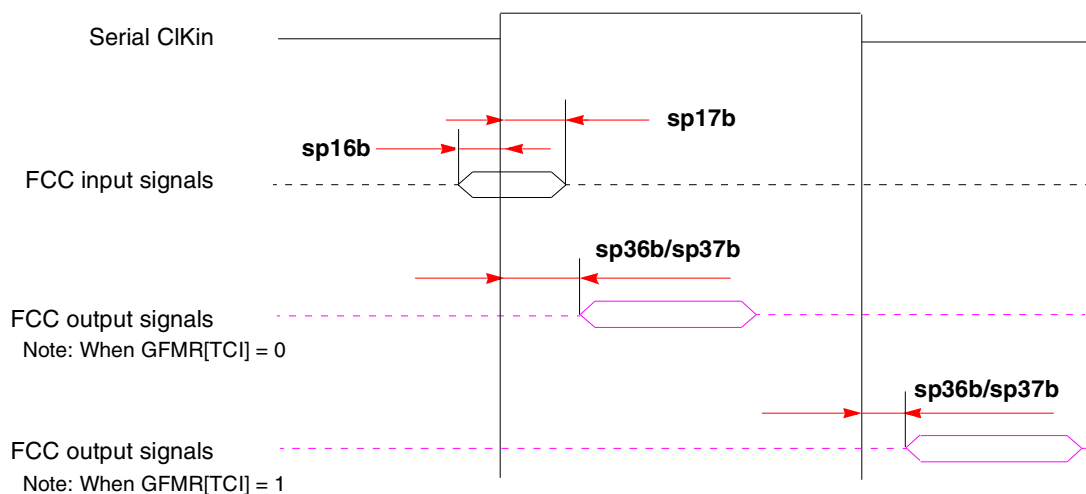
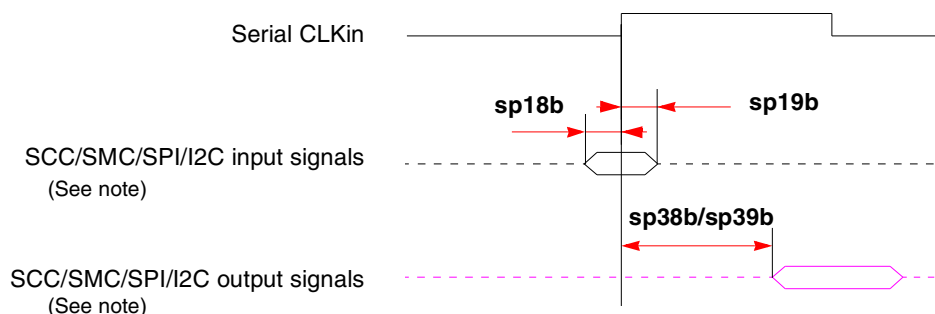


Figure 4. FCC External Clock Diagram

This figure shows the SCC/SMC/SPI/I²C external clock.



Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram

NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

Table 11. AC Characteristics for SIU Inputs¹

Spec Number		Characteristic	Value (ns)							
Setup	Hold		Setup				Hold			
			66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp11	sp10	AACK/TA/TSDBG/BG/BR/ARTRY/TEA	6	5	3.5	N/A	0.5	0.5	0.5	N/A
sp12	sp10	Data bus in normal mode	5	4	3.5	N/A	0.5	0.5	0.5	N/A
sp13	sp10	Data bus in pipeline mode (without ECC and PARITY)	N/A	4	2.5	1.5	N/A	0.5	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	N/A	0.5	0.5	0.5	N/A

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 12. AC Characteristics for SIU Outputs¹

Spec Number		Characteristic	Value (ns)							
Max	Min		Maximum Delay				Minimum Delay			
			66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp31	sp30	PSDVAL/TEA/TA	7	6	5.5	N/A	1	1	1	N/A
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	4.5 ²	1	1	1	1 ²
sp33	sp30	Data bus ³	6.5	6.5	5.5	4.5	0.8	0.8	0.8	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	4.5	1	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	N/A	1	1	1	N/A

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

² Value is for ADD only; other sp32/sp30 signals are not applicable.

³ To achieve 1 ns of hold time at 66.67/83.33/100 MHz, a minimum loading of 20 pF is required.

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing.

This table lists SIU input characteristics.

Table 13. AC Characteristics for SIU Inputs¹

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11	sp10	AACK/TA/TS/DBG/BG/BR/ARTRY/TEA	6	5	3.5	0.5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	7	5	3.5	0.5	0.5	0.5
sp13a	sp10	Pipeline mode—Data bus (with or without ECC/PARITY)	5	4	2.5	0.5	0.5	0.5
sp14	sp10	DP pins	7	5	3.5	0.5	0.5	0.5
sp14a	sp10	Pipeline mode—DP pins	—	4	2.5	—	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	0.5	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 14. AC Characteristics for SIU Outputs¹

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31	sp30	PSDVAL/TEA/TA	7	6	5.5	1	1	1
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	1	1	1
sp33a	sp30	Data bus ²	6.5	6.5	5.5	0.7	0.7	0.7
sp33b	sp30	DP	6	5.5	5.5	1	1	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	1	1	1
sp35a	sp30	AP	7	7	7	1	1	1

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

² To achieve 1 ns of hold time at 66, 83, or 100 MHz, a minimum loading of 20 pF is required.

Table 17. SoC Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK ¹			
1	—	—	Local bus	—	Table 18
0	0	0	PCI host	50–66	Table 19
0	0	1		25–50	Table 20
0	1	0	PCI agent	50–66	Table 21
0	1	1		25–50	Table 22

¹ Determines PCI clock frequency range. See [Section 7.2, “PCI Host Mode,”](#) and [Section 7.3, “PCI Agent Mode.”](#)

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

7.1 Local Bus Mode

This table lists clock configurations for the SoC in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

Table 18. Clock Configurations for Local Bus Mode¹

Mode ²	Bus Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
Default Modes (MODCK_H= 0000)								
0000_000	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0000_001	33.3	133.3	3	100.0	400.0	5	166.7	666.7
0000_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0000_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0000_100	60.0	167.0	2	120.0	334.0	2.5	150.0	417.5
0000_101	50.0	167.0	2	100.0	334.0	3	150.0	501.0
0000_110	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0000_111	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
Full Configuration Modes								
0001_000	50.0	167.0	2	100.0	334.0	4	200.0	668.0

Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)^{1,2} (continued)

Mode ³	Bus Clock ⁴ (MHz)		CPM Multiplication Factor ⁵	CPM Clock (MHz)		CPU Multiplication Factor ⁶	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
0100_000	Reserved										
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0101_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0101_010	50.0	66.7	2	100.0	133.3	3.5	175.0	233.3	2	50.0	66.7
0101_011	50.0	66.7	2	100.0	133.3	4	200.0	266.6	2	50.0	66.7
0101_100	50.0	66.7	2	100.0	133.3	4.5	225.0	300.0	2	50.0	66.7
0110_000	60.0	80.0	2.5	150.0	200.0	2.5	150.0	200.0	3	50.0	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7

This figure shows the pinout of the ZU and VV packages as viewed from the top surface.

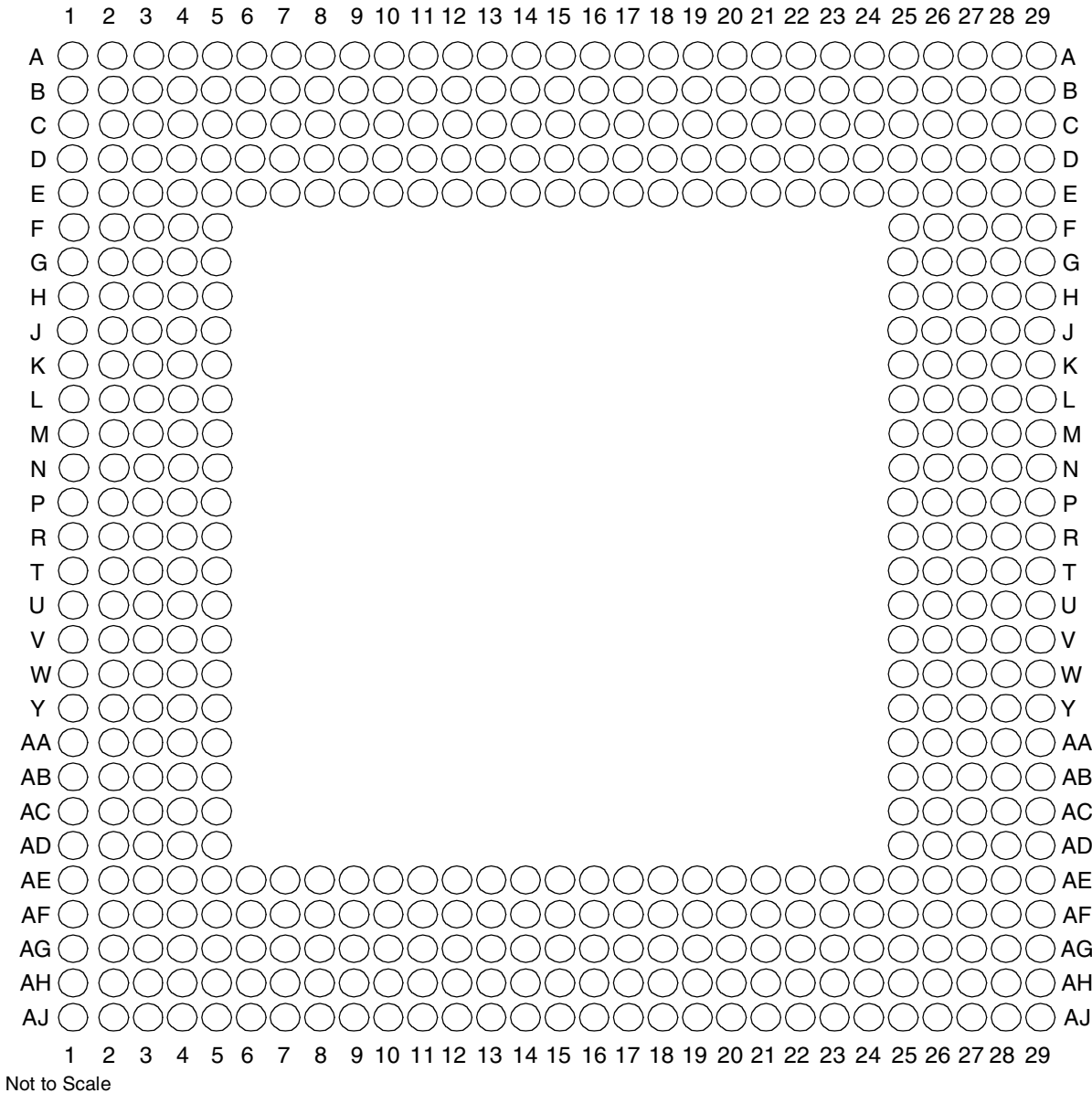


Figure 13. Pinout of the 480 TBGA Package (View from Top)

This table lists the pins of the MPC8280 and MPC8270, and [Table 24](#) defines conventions and acronyms used in this table.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{\text{BR}}$		W5
$\overline{\text{BG}}$		F4

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LSDWE/LGPL1/PCI_MODCKH1		C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2		E26
LSDCAS/LGPL3/PCI_MODCKH3		D25
LGTA/LUPMWAIT/LGPL4/LPBS		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
LWR		D28
L_A14/PAR		N27
L_A15/FRAME/SMI		T29
L_A16/TRDY		R27
L_A17/IRDY/CKSTP_OUT		R26
L_A18/STOP		R29
L_A19/DEVSEL		R28
L_A20/IDSEL		W29
L_A21/PERR		P28
L_A22/SERR		N26
L_A23/REQ0		AA27
L_A24/REQ1/HSEJSW		P29
L_A25/GNT0		AA26
L_A26/GNT1/HSLED		N25
L_A27/GNT2/HSENUM		AA25
L_A28/RST/CORE_SRESET		AB29
L_A29/INTA		AB28
L_A30/REQ2		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LCL_D9/AD9		L26
LCL_D10/AD10		L25
LCL_D11/AD11		M29
LCL_D12/AD12		M28
LCL_D13/AD13		M27
LCL_D14/AD14		M26
LCL_D15/AD15		N29
LCL_D16/AD16		T25
LCL_D17/AD17		U27
LCL_D18/AD18		U26
LCL_D19/AD19		U25
LCL_D20/AD20		V29
LCL_D21/AD21		V28
LCL_D22/AD22		V27
LCL_D23/AD23		V26
LCL_D24/AD24		W27
LCL_D25/AD25		W26
LCL_D26/AD26		W25
LCL_D27/AD27		Y29
LCL_D28/AD28		Y28
LCL_D29/AD29		Y25
LCL_D30/AD30		AA29
LCL_D31/AD31		AA28
LCL_DP0/C0/ $\overline{\text{BE}}0$		L28
LCL_DP1/C1/ $\overline{\text{BE}}1$		N28
LCL_DP2/C2/ $\overline{\text{BE}}2$		T28
LCL_DP3/C3/ $\overline{\text{BE}}3$		W28
$\overline{\text{IRQ}}0/\text{NMI_OUT}$		T1
$\overline{\text{IRQ}}7/\text{INT_OUT}/\text{APE}$		D1
$\overline{\text{TRST}}^1$		AH3
TCK		AG5
TMS		AJ3
TDI		AE6

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AB26 ²
PC1/DREQ2/BRGO6/L1RQA2/ SPISEL		AD29 ²
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AE29 ²
PC3/FCC3_CTS/DACK2/CTS4/ USB_RP	FCC2_UT8_TXD2	AE27 ²
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AF27 ²
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AF24 ²
PC6/FCC1_CD	L1CLKOC1/FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26 ²
PC7/FCC1_CTS	L1RQC1/FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25 ²
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USBRN	FCC1_UT16_TXD0	AF22 ²
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	AE21 ²
PC10/CD3/RENA3	FCC1_UT16_TXD2/SI1_L1ST4/ FCC2_UT8_RXD3	AF20 ²
PC11/CTS3/CLSN3/L1TXD3A2	L1CLKOD1/FCC2_UT8_RXD2	AE19 ²
PC12/CD2/RENA2	SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	AE18 ²
PC13/CTS2/CLSN2	L1RQD1/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	AH18 ²
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	AH17 ²
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	AG16 ²
PC16/CLK16/TIN4		AF15 ²
PC17/CLK15/TIN3/BRGO8		AJ15 ²
PC18/CLK14/TGATE2		AH14 ²
PC19/CLK13/BRGO7/SPICLK		AG13 ²
PC20/CLK12/TGATE1/USB_OE		AH12 ²
PC21/CLK11/BRGO6		AJ11 ²
PC22/CLK10/DONE1/FCC1_UT_TXPRTY		AG10 ²
PC23/CLK9/BRGO5/DACK1		AE10 ²

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PC24/CLK8/ $\overline{\text{TOUT4}}$	FCC2_UT8_TXD3	AF9 ²
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	AE8 ²
PC26/CLK6/ $\overline{\text{TOUT3}}$ /TMCLK		AJ6 ²
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		AG2 ²
PC28/CLK4/TIN1/ $\overline{\text{TOUT2}}$ / $\overline{\text{CTS2}}$ /CLSN2/ FCC2_RXADDR4		AF3 ²
PC29/CLK3/TIN2/BRGO2/ $\overline{\text{CTS1}}$ /CLSN1		AF2 ²
PC30/CLK2/ $\overline{\text{TOUT1}}$	FCC2_UT8_TXD3	AE1 ²
PC31/CLK1/BRGO1		AD1 ²
PD4/BRGO8/ $\overline{\text{FCC3_RTS}}$ /SMRDX2	L1TSYNCD1/L1GNTD1	AC28 ²
PD5/ $\overline{\text{DONE1}}$	FCC1_UT16_TXD3	AD27 ²
PD6/ $\overline{\text{DACK1}}$	FCC1_UT16_TXD4	AF29 ²
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AF28 ²
PD8/SMRDX1/BRGO5	FCC2_UT_TXPRTY	AG25 ²
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	AH26 ²
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AJ27 ²
PD11/ $\overline{\text{L1RQB2}}$	FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1	AJ23 ²
PD12	SI1_L1ST2/L1RXDB1	AG23 ²
PD13	SI1_L1ST1/L1TXDB1	AJ22 ²
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	AE20 ²
PD15/ $\overline{\text{L1RQC2}}$ /I2CSDA	FCC1_UT16_RXD1	AJ20 ²
PD16/SPIMISO	FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1	AG18 ²
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	AG17 ²
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	AF16 ²
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	AH15 ²

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
Core power		U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground		AA5, AB1 ⁶ , AB2 ⁷ , AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

¹ Should be tied to VDDH via a 2K Ω external pull-up resistor.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

³ Must be pulled down or left floating.

⁴ If PCI is not desired, must be pulled up or left floating.

⁵ Sphere is not connected to die.

⁶ GND SYN (AB1): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the SoC. New designs must connect AB1 to GND and follow the suggestions in [Section 4.6, “Layout Practices.”](#) Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.

⁷ XFC (AB2) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8280 because there is no need for external capacitor to operate the PLL. New designs should connect AB2 (XFC) pin to GND. Old designs in which the SoC is used as a drop-in replacement can leave the pin connected to the current capacitor.

This table describes symbols used in [Table 23](#).

Table 24. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.
RMII	Indicates that a signal is part of the reduced media independent interface.

8.2 VR and ZQ Packages—MPC8275 and MPC8270

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8280 and the MPC8270, see [Section 8.1, “ZU and VV Packages—MPC8280 and MPC8270.”](#)

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
$\overline{CS4}$		AF7
$\overline{CS5}$		AC7
$\overline{CS6}$		AD7
$\overline{CS7}$		AF8
$\overline{CS8}$		AE8
$\overline{CS9}$		AD8
$\overline{CS10/BCTL1}$		AC8
$\overline{CS11/AP0}$		AB8
BADDR27		C13
BADDR28		A12
ALE		D13
$\overline{BCTL0}$		AF4
$\overline{PWE0/PSDDQM0/PBS0}$		AA5
$\overline{PWE1/PSDDQM1/PBS1}$		AE4
$\overline{PWE2/PSDDQM2/PBS2}$		AD4
$\overline{PWE3/PSDDQM3/PBS3}$		AF3
$\overline{PWE4/PSDDQM4/PBS4}$		AB4
$\overline{PWE5/PSDDQM5/PBS5}$		AE3
$\overline{PWE6/PSDDQM6/PBS6}$		AF2
$\overline{PWE7/PSDDQM7/PBS7}$		AD3
$\overline{PSDA10/PGPL0}$		AE2
$\overline{PSDWE/PGPL1}$		AD2
$\overline{POE/PSDRAS/PGPL2}$		AE1
$\overline{PSDCAS/PGPL3}$		AC3
$\overline{PGTA/PUPMWAIT/PGPL4/PPBS}$		W6
$\overline{PSDAMUX/PGPL5}$		AA4
$\overline{LWE0/LSDDQM0/LBS0/PCI_CFG0}$		AC9
$\overline{LWE1/LSDDQM1/LBS1/PCI_CFG1}$		AD9
$\overline{LWE2/LSDDQM2/LBS2/PCI_CFG2}$		AE9
$\overline{LWE3/LSDDQM3/LBS3/PCI_CFG3}$		AF9
$\overline{LSDA10/LGPL0/PCI_MODCKH0}$		AB6
$\overline{LSDWE/LGPL1/PCI_MODCKH1}$		AF5
$\overline{LOE/LSDRAS/LGPL2/PCI_MODCKH2}$		AE5

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23 ²
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26 ²
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23 ²
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23 ²
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26 ²
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25 ²
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26 ²
PA26/FCC1_MII_RMII_RX_ER/ FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25 ²
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	C25 ²
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	C22 ²
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21 ²
PA30/FCC1_MII_CRS/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20 ²
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	A19 ²
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/FCC3_RTS	FCC2_UT8_RXD0	AD21 ²
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GN2A2	FCC2_UT8_RXD1	AD22 ²
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22 ²
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26 ²
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23 ²
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26 ²
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26 ²
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25 ²
PB12/FCC3_MII_CRS/TXD2		W26 ²
PB13/FCC3_MII_COL/L1TXD1A2		W25 ²
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PB15/FCC3_MII_TX_ER/RXD2		U24 ²
PB16/FCC3_MII_RMII_RX_ER/CLK18		R22 ²
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV		R23 ²
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	M23 ²
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	L24 ²
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6	K24 ²
PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7	L21 ²
PB22/FCC2_MII_HDLC_RMII_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7	P25 ²
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6	N25 ²
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5	E26 ²
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4	H23 ²
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	C26 ²
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	B26 ²
PB28/FCC2_MII_RX_ER/FCC2_RMII_RX_ER/ FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1		A22 ²
PB29/L1RSYNCB2/ FCC2_MII_TX_EN/FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	A21 ²
PB30/FCC2_MII_RX_DV/L1RXDB2/ FCC2_RMII_CRS_DV	FCC2_UT_TXSOC	E20 ²
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	C20 ²
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AE22 ²
PC1/DREQ2/SPISEL/BRGO6/L1RQA2		AA19 ²
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AF24 ²
PC3/FCC3_CTS/DACK2/CTS4/ USB_RP	FCC2_UT8_TXD2	AE25 ²
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AB22 ²

9.1 Package Parameters

This table provides package parameters.

NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see [Table 2](#)). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

Table 26. Package Parameters

Package	SoCs	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8280 MPC8270	37.5 × 37.5	TBGA	480	1.27	1.55
VV	MPC8280 MPC8270	37.5 × 37.5	TBGA	480	1.27	1.55
VR	MPC8275VR MPC8270VR	27 × 27	PBGA	516	1	2.25
ZQ	MPC8275ZQ MPC8270ZQ	27 × 27	PBGA	516	1	2.25