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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8270czuqlda

1 Overview

This table shows the functionality supported by each SoC in the MPC8280 family.

Table 1. MPC8280 PowerQUICC II Family Functionality

Functionality	SoCs			
	MPC8270		MPC8275	MPC8280
Package[1]	480 TBGA	516 PBGA	516 PBGA	480 TBGA
Serial communications controllers (SCCs)	4	4	4	4
QUICC multi-channel controller (QMC)	—	—	—	—
Fast communication controllers (FCCs)	3	3	3	3
I-Cache (Kbyte)	16	16	16	16
D-Cache (Kbyte)	16	16	16	16
Ethernet (10/100)	3	3	3	3
UTOPIA II Ports	0	0	2	2
Multi-channel controllers (MCCs)	1	1	1	2
PCI bridge	Yes	Yes	Yes	Yes
Transmission convergence (TC) layer	—	—	—	Yes
Inverse multiplexing for ATM (IMA)	—	—	—	Yes
Universal serial bus (USB) 2.0 full/low rate	1	1	1	1
Security engine (SEC)	—	—	—	—

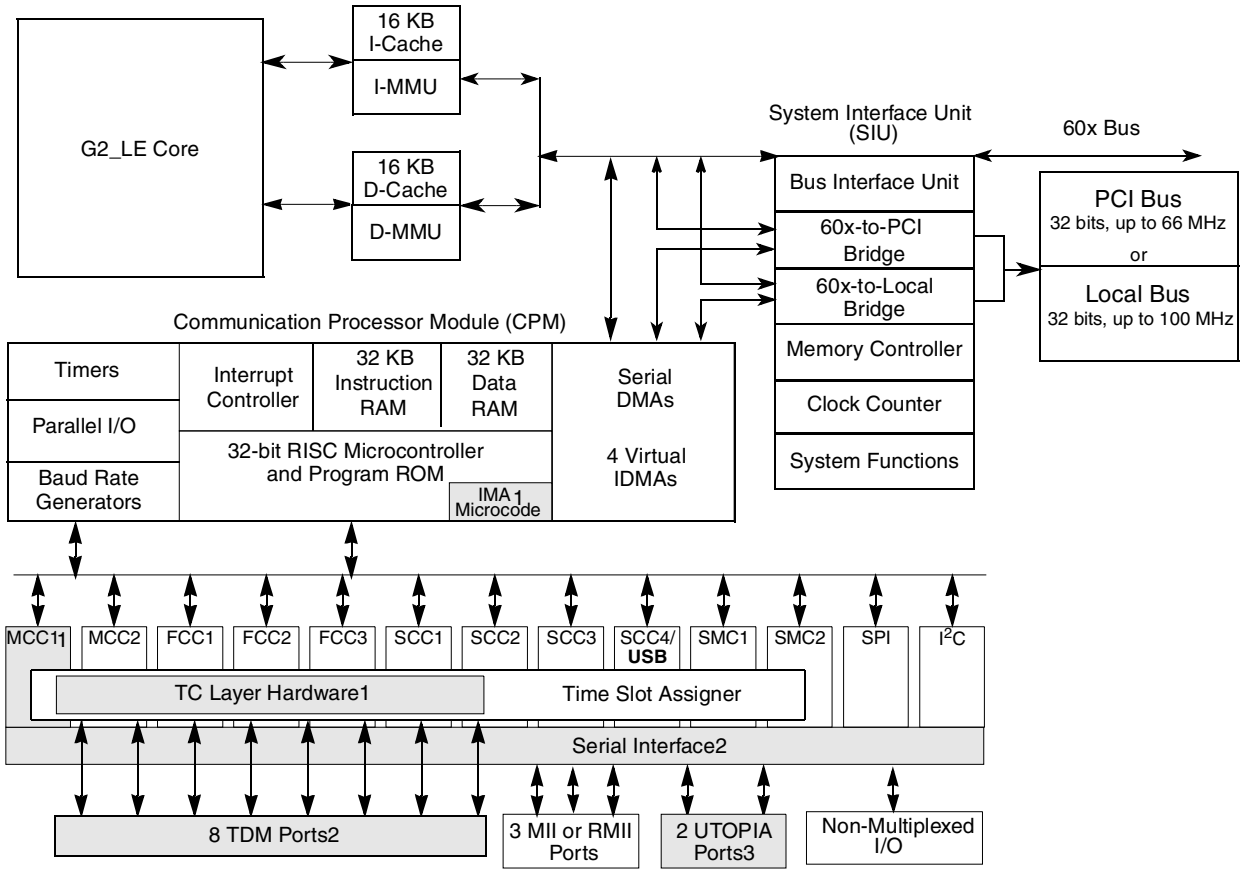
[1] See Table 2.

Devices in the MPC8280 family are available in four packages—the standard ZU and VV packages and the alternate VR or ZQ packages—as shown in Table 2. Note that throughout this document, references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Freescale sales office. For package ordering information, see Section 10, “Ordering Information.”

Table 2. HiP7 PowerQUICC II Device Packages

Code (Package)	ZU (480 TBGA—Leaded)	VV (480 TBGA—Lead Free)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8280	MPC8280	MPC8275VR	MPC8275ZQ
	MPC8270	MPC8270	MPC8270VR	MPC8270ZQ

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.



Notes:
[1] MPC8280 only (**not on MPC8270,** the VR package, nor the ZQ package)
[2] MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).
[3] MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270,** MPC8270VR, nor MPC8270ZQ)

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.0	2/2004	• Removal of “Advance Information” and “Preliminary.” The MPC8280 is fully qualified. • Table 2: New • Figure 1: Modification to note 2 • Section 1.1: Core frequency range is 166–450 MHz • Addition of ZQ (516 PBGA with Lead spheres) package references • Table 4: VDD and VCCSYN modified to 1.45–1.60 V • Note following Table 4: Modified • Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5) • Table 5: Changed I_{OL} for 60x signals to 6.0 mA • Table 5: Moved QREQ to V_{OL}: I_{OL}= 3.2 mA • Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for V_{OL} (I_{OL} = 6.0mA) • Table 10: Addition of $_{JT}$ and note 4 • Sections 4.1–4.5: New • Table 12: Modified power values (+ 150mW to each) • Table 14: Addition of note 2. Changed PCI impedance to 27 . • Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41 • Table 20: Changes to sp16a, sp18a, sp20 and sp21 • Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle • Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz • Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2. • Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables. • Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6) • Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted. • Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted. • Table 23: Addition of note 5 to ‘No connect’ (AA1, AG4) • Addition of “Note: Temperature Reflow for the VR Package" on page 76 • Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25) • Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins: PA6—FCC2_UT_RXADDR3 PA7—FCC2_UT_TXADDR3 PA8—FCC2_UT_TXADDR4 PB14—RXD3 PC19—SPICLK PC22—FCC1_UT_TXPRTY PC28—FCC2_UT_RXADDR4 • Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1): PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28] • Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted. • Table 25: Addition of note 5 to ‘No connect’ (E17, C23)