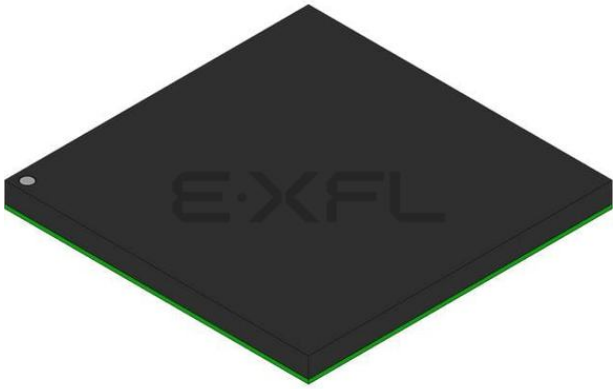

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8275czqmiba

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

This table lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions[1]

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.45 – 1.60	V
PLL supply voltage	VCCSYN	1.45 – 1.60	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T_j	105[2]	°C
Ambient temperature	T_A	0–70[2]	°C

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A} – 105_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

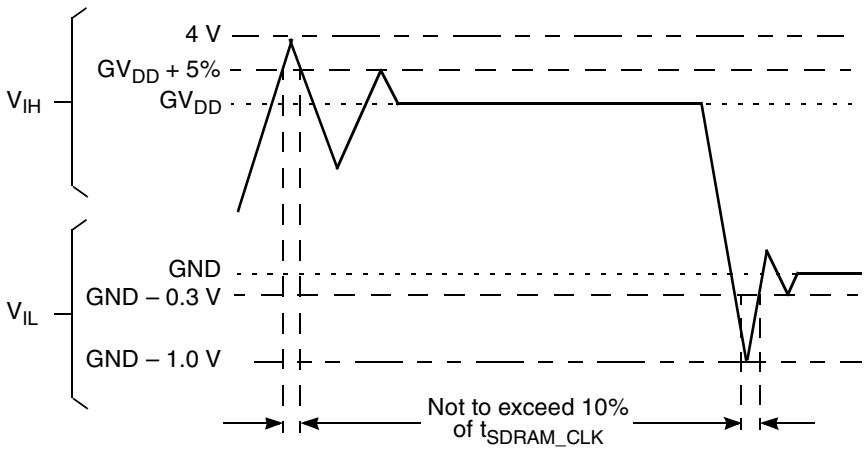

Figure 2. Overshoot/Undershoot Voltage

3 DC Electrical Characteristics

This table shows DC electrical characteristics.

Table 5. DC Electrical Characteristics[1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH[3]	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, V_{IN} = VDDH[3]	I_{OZ}	—	10	μA
Signal low input current, V_{IL} = 0.8 V[4]	I_L	—	1	μA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	μA
Output high voltage, I_{OH} = –2 mA except UTOPIA mode, and open drain pins In UTOPIA mode[5] (UTOPIA pins only): I_{OH} = -8.0mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	—	V
In UTOPIA mode[5] (UTOPIA pins only): I_{OL} = 8.0mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	—	0.5	V

NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

Table 11. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Value (ns)							
			Setup				Hold			
Setup	Hold		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp11	sp10	$\overline{AACK}/\overline{TA}/\overline{TS}/\overline{DBG}/\overline{BG}/\overline{BR}/\overline{ARTRY}/\overline{TEA}$	6	5	3.5	N/A	0.5	0.5	0.5	N/A
sp12	sp10	Data bus in normal mode	5	4	3.5	N/A	0.5	0.5	0.5	N/A
sp13	sp10	Data bus in pipeline mode (without ECC and PARITY)	N/A	4	2.5	1.5	N/A	0.5	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	N/A	0.5	0.5	0.5	N/A

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 12. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Value (ns)							
			Maximum Delay				Minimum Delay			
Max	Min		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp31	sp30	$\overline{PSDVAL}/\overline{TEA}/\overline{TA}$	7	6	5.5	N/A	1	1	1	N/A
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	4.5[2]	1	1	1	1 [2]
sp33	sp30	Data bus[3]	6.5	6.5	5.5	4.5	0.8	0.8	0.8	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	4.5	1	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	N/A	1	1	1	N/A

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2 Value is for ADD only; other sp32/sp30 signals are not applicable.
3 To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.

Table 15. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

This table is a representation of the information in Table 15.

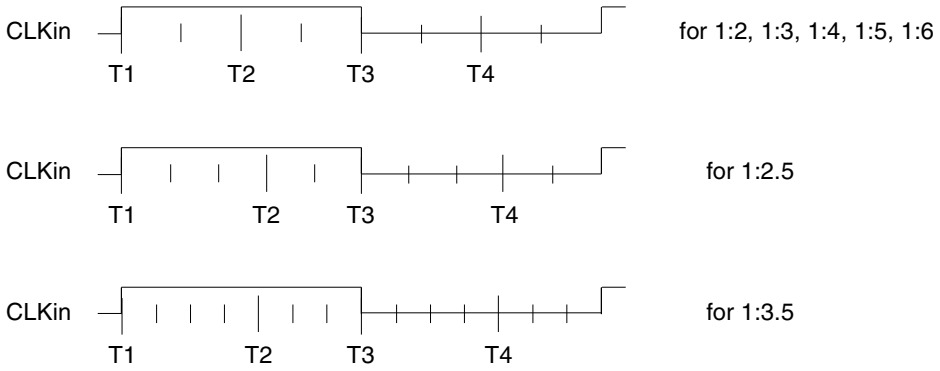

Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

6.3 JTAG Timings

This table lists the JTAG timings.

Table 16. JTAG Timings[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	 ns ns	 4, 7 4, 7

Table 18. Clock Configurations for Local Bus Mode[1] (continued)

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
0110_000	50.0	167.0	2	100.0	334.0	3.5	250.0	584.5
0110_001	50.0	167.0	2	100.0	334.0	4	250.0	668.0
0110_010	50.0	167.0	2	100.0	334.0	4.5	250.0	751.5
0110_011	Reserved							
0110_100	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0110_101	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
0110_110	42.9	160.0	2.5	107.1	400.0	3.5	150.0	560.0
0110_111	40.0	160.0	2.5	100.0	400.0	4	160.0	640.0
0111_000	40.0	160.0	2.5	100.0	400.0	4.5	180.0	720.0
0111_001	Reserved							
0111_010	Reserved							
0111_011	50.0	133.3	3	150.0	400.0	3	150.0	400.0
0111_100	42.9	133.3	3	128.6	400.0	3.5	150.0	466.7
0111_101	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0111_110	33.3	133.3	3	100.0	400.0	4.5	150.0	600.0
0111_111	Reserved							
1000_000	Reserved							
1000_001	Reserved							
1000_010	42.9	114.3	3.5	150.0	400.0	3.5	150.0	400.0
1000_011	37.5	114.3	3.5	131.3	400.0	4	150.0	457.1
1000_100	33.3	114.3	3.5	116.7	400.0	4.5	150.0	514.3
1000_101	30.0	114.3	3.5	105.0	400.0	5	150.0	571.4
1000_110	28.6	114.3	3.5	100.0	400.0	5.5	150.0	628.6
1100_000	Reserved							
1100_001	Reserved							
1100_010	Reserved							
1101_000	Reserved							

Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0110_011	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7
0111_000	Reserved										
0111_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0111_010	50.0	66.7	3	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0111_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0111_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
1000_000	Reserved										
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7
1000_010	66.7	88.9	3	200.0	266.6	3.5	233.3	311.1	4	50.0	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200.0	266.6	3.5	200.0	266.6	4	50.0	66.7
1001_011	57.1	76.2	3.5	200.0	266.6	4	228.6	304.7	4	50.0	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0
1000_010	66.7	133.3	3	200.0	400.0	3.5	233.3	466.7	8	25.0	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	114.3	3.5	200.0	400.0	3.5	200.0	400.0	8	25.0	50.0
1001_011	57.1	114.3	3.5	200.0	400.0	4	228.6	457.1	8	25.0	50.0
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	42.9	85.7	3.5	150.0	300.0	5	214.3	428.6	6	25.0	50.0
1001_110	42.9	85.7	3.5	150.0	300.0	5.5	235.7	471.4	6	25.0	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0

Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0	266.6	4.5	225.0	300.0	4	50.0	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{ABB}$/$\overline{IRQ2}$		E2
$\overline{TS}$		E3
A0		G1
A1		H5
A2		H2
A3		H1
A4		J5
A5		J4
A6		J3
A7		J2
A8		J1
A9		K4
A10		K3
A11		K2
A12		K1
A13		L5
A14		L4
A15		L3
A16		L2
A17		L1
A18		M5
A19		N5
A20		N4
A21		N3
A22		N2
A23		N1
A24		P4
A25		P3
A26		P2
A27		P1
A28		R1
A29		R3
A30		R5

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
D18		D15
D19		C13
D20		B11
D21		A8
D22		A5
D23		C5
D24		C19
D25		C17
D26		C15
D27		D13
D28		C11
D29		B8
D30		A4
D31		E6
D32		E18
D33		B17
D34		A15
D35		A12
D36		D11
D37		C8
D38		E7
D39		A3
D40		D18
D41		A17
D42		A14
D43		B12
D44		A10
D45		D8
D46		B6
D47		C4
D48		C18
D49		E16
D50		B14

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
TDO		AF5
TRIS		AB4
$\overline{\text{PORESET}}$[1]		AG6
$\overline{\text{HRESET}}$		AH5
$\overline{\text{SRESET}}$		AF6
$\overline{\text{QREQ}}$		AA3
$\overline{\text{RSTCONF}}$		AJ4
MODCK1/AP1/TC0/BNKSEL0		W2
MODCK2/AP2/TC1/BNKSEL1		W3
MODCK3/AP3/TC2/BNKSEL2		W4
CLKIN1		AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3	FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	FCC2_UTM_TXADDR1	AC25[2]
PA2/CLK20/$\overline{\text{DACK3}}$	FCC2_UTM_TXADDR0	AE28[2]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	FCC2_UTM_RXADDR0	AG29[2]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	FCC2_UTM_RXADDR1	AG28[2]
PA5/$\overline{\text{RESTART2}}$/DREQ4	FCC2_UTM_RXADDR2/FCC1_UT_RXPRTY	AG26[2]
PA6/FCC2_RXADDR3	L1RSYNCA1	AE24[2]
PA7/SMSYN2/FCC2_TXADDR3	L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/FCC2_TXADDR4	L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2	L1TXD0A1	AH23[2]
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	AE22[2]
PA11/MSNUM4	FCC1_UT8_RXD1/FCC1_UT16_RXD9	AH22[2]
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	AJ21[2]
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	AH20[2]
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	AG19[2]
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT8_RXD5/ FCC1_UT16_RXD13	AF18[2]
PA16/FCC1_MII_HDLC_RXD1/ FCCI_RMII_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	AF17[2]

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/TXD2	L1CLKOB1/L1RSYNCC1	AG22[2]
PB13/FCC3_MII_COL/L1TXD1A2	$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1	AH21[2]
PB14/FCC3_MII_RMII_TX_EN//RXD3	L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19[2]
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18[2]
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV	L1RQA1	AJ17[2]
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14[2]
PB19FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13[2]
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12[2]
PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11[2]
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16[2]
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15[2]
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9[2]
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7[2]
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6[2]
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1		AE3[2]
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2[2]
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5[2]
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4[2]

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	AF9[2]
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	AE8[2]
PC26/CLK6/TOUT3/TMCLK		AJ6[2]
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		AG2[2]
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2/ FCC2_RXADDR4		AF3[2]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		AF2[2]
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	AE1[2]
PC31/CLK1/BRGO1		AD1[2]
PD4/BRGO8/FCC3_RTS/SMRXD2	L1TSYNCD1/L1GNTD1	AC28[2]
PD5/DONE1	FCC1_UT16_TXD3	AD27[2]
PD6/DACK1	FCC1_UT16_TXD4	AF29[2]
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AF28[2]
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AG25[2]
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	AH26[2]
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AJ27[2]
PD11/L1RQB2	FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1	AJ23[2]
PD12	SI1_L1ST2/L1RXDB1	AG23[2]
PD13	SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	AE20[2]
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	AJ20[2]
PD16/SPIMISO	FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1	AG18[2]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	AG17[2]
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	AF16[2]
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	AH15[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
LCL_D11/AD11		AC13
LCL_D12/AD12		AC12
LCL_D13/AD13		AB13
LCL_D14/AD14		AD12
LCL_D15/AD15		AF14
LCL_D16/AD16		AF17
LCL_D17/AD17		AE16
LCL_D18/AD18		AD16
LCL_D19/AD19		AC16
LCL_D20/AD20		AB16
LCL_D21/AD21		AF18
LCL_D22/AD22		AE17
LCL_D23/AD23		AD17
LCL_D24/AD24		AB17
LCL_D25/AD25		AE18
LCL_D26/AD26		AD18
LCL_D27/AD27		AC18
LCL_D28/AD28		AE19
LCL_D29/AD29		AF20
LCL_D30/AD30		AD19
LCL_D31/AD31		AB18
LCL_DP0/C0/$\overline{\text{BE0}}$		AE12
LCL_DP1/C1/$\overline{\text{BE1}}$		AA13
LCL_DP2/C2/$\overline{\text{BE2}}$		AC15
LCL_DP3/C3/$\overline{\text{BE3}}$		AF19
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$		A11
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$		E5
$\overline{\text{TRST}}$[1]		F22
TCK		A24
TMS		C24
TDI		A25
TDO		B24
$\overline{\text{TRIS}}$		C19

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23[2]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26[2]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23[2]
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23[2]
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26[2]
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25[2]
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26[2]
PA26/FCC1_MII_RMII_RX_ER/	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25[2]
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	C25[2]
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	$\overline{\text{FCC1\_UTM\_RXENB}}$/ $\overline{\text{FCC1\_UTS\_RXENB}}$	C22[2]
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21[2]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20[2]
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UTM\_TXENB}}$/ $\overline{\text{FCC1\_UTS\_TXENB}}$	A19[2]
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	FCC2_UT8_RXD0	AD21[2]
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD22[2]
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22[2]
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26[2]
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23[2]
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26[2]
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25[2]
PB12/FCC3_MII_CRS/TXD2		W26[2]
PB13/FCC3_MII_COL/L1TXD1A2		W25[2]
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25[2]
PC6/FCC1_CD	FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25[2]
PC7/FCC1_CTS	FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24[2]
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USB_RN	FCC1_UT16_TXD0	Y24[2]
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	U22[2]
PC10/CD3/RENA3	FCC1_UT16_TXD2/FCC2_UT8_RXD3	V23[2]
PC11/CTS3/CLSN3/L1TXD3A2	FCC2_UT8_RXD2	U23[2]
PC12/CD2/RENA2	FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26[2]
PC13/CTS2/CLSN2	FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26[2]
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26[2]
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24[2]
PC16/CLK16/TIN4		M26[2]
PC17/CLK15/TIN3/BRGO8		L26[2]
PC18/CLK14/TGATE2		M24[2]
PC19/CLK13/BRGO7/SPICLK		L22[2]
PC20/CLK12/TGATE1/USB_OE		K25[2]
PC21/CLK11/BRGO6		J25[2]
PC22/CLK10/DONE1	FCC1_UT_TXPRTY	G26[2]
PC23/CLK9/BRGO5/DACK1		F26[2]
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	G24[2]
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25[2]
PC26/CLK6/TOUT3/TMCLK		G23[2]
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		B23[2]
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	FCC2_UT_RXADDR4	E22[2]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21[2]
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	D21[2]

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC31/CLK1/BRGO1		B20[2]
PD4/BRGO8/FCC3_RTS/SMRXD2		AF23[2]
PD5/DONE1	FCC1_UT16_TXD3	AE23[2]
PD6/DACK1	FCC1_UT16_TXD4	AB21[2]
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AD23[2]
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AD26[2]
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22[2]
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1	AB24[2]
PD11/L1RQB2	FCC2_UT8_RXD0 L1GNTB1	Y23[2]
PD12		AA26[2]
PD13		W24[2]
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22[2]
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26[2]
PD16/SPIMISO	FCC1_UT_TXPRTY	T23[2]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25[2]
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	P23[2]
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	N22[2]
PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	M25[2]
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	L25[2]
PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	J26[2]
PD23/RTS3/TENA3	FCC1_UT16_RXD4	K22[2]
PD24/TXD3	FCC1_UT16_RXD5	G25[2]
PD25/RXD3	FCC1_UT16_TXD6	H24[2]
PD26/RTS2/TENA2	FCC1_UT16_RXD6	F24[2]

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.4	11/2005	• In Section 6.2, "SIU AC Characteristics", modified the note on CLKIN Jitter and Duty Cycle. • Modified Figure 17 to display all text.
1.3	01/2005	• Modification for correct display of assertion level ("overbar") for some signals
1.2	12/2004	• Section 2: removed voltage tracking note • Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset • Table 5: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pullup removed. • Table 5: Note 4 added regarding IIC compatibility • Section 4.2: New information about jumper-to-case thermal resistance • Section 4.3: New information about jumper-to-board thermal resistance • Section 4.4: New information about estimation with simulation • Section 4.6: Updated description of layout practices • Section 6: Added sentence providing derating factor • Section 6.1, "CPM AC Characteristics": added Note: Rise/Fall Time on CPM Input Pins • Table 9: updated values for following specs: sp42, sp43, sp42a • Table 20: updated values for following specs: sp16b, sp18b, sp20, sp22 • Section 6.2: added spread sprectrum clocking note • Table 11: combined specs sp11 and sp11a • Sections 7.2, 7.3: unit of ns added to Tval notes • Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
0.3	6/2003	• Removal of notes stating “no local bus” on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support. • References to “G2 core” changed to “G2_LE core.” See the *G2 Core Reference Manual* (G2CORERM/D). • Addition of VCCSYN to “Note” below Table 4, and to note 3 of Table 5 • Figure 2: New • Table 5: Addition of note 1 • Table 10: Addition of θ_{JB} and θ_{JC}. Modifications to ZU package values. • Table 12: Addition of various configurations, Modification of values. Addition of note 3. • Table 9: Addition of 66 MHZ and 100 MHz values. Addition of sp42a/sp43a. • Table 20: Addition of 66 MHZ and 100 MHz values • Table 12: sp30 values. sp33b @100 MHz value. Removal of previous note 2. Modification of current note 2. • Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes • Section 6.2: Addition of note on PCI timing • Table 18, Table 32, Table 33, Table 36, Table 37: Addition of note 1 concerning minimum operating frequencies • Addition of statement before clock tables about selection of clock configuration and input frequency • Table 23 and Table 25: Addition of note 1 to CPM pins
0.2	11/2002	Table 25, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 63)
0.1	—	Initial public release