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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8280cvvqlda

  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One I^2C controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
  - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

2 Operating Conditions

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	–0.3 – 2.25	V
PLL supply voltage[2]	VCCSYN	–0.3 – 2.25	V
I/O supply voltage[3]	VDDH	–0.3 – 4.0	V
Input voltage[4]	VIN	GND(–0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(–55) – (+150)	°C

[1] Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

This table lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions[1]

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.45 – 1.60	V
PLL supply voltage	VCCSYN	1.45 – 1.60	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T_j	105[2]	°C
Ambient temperature	T_A	0–70[2]	°C

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A} – 105_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

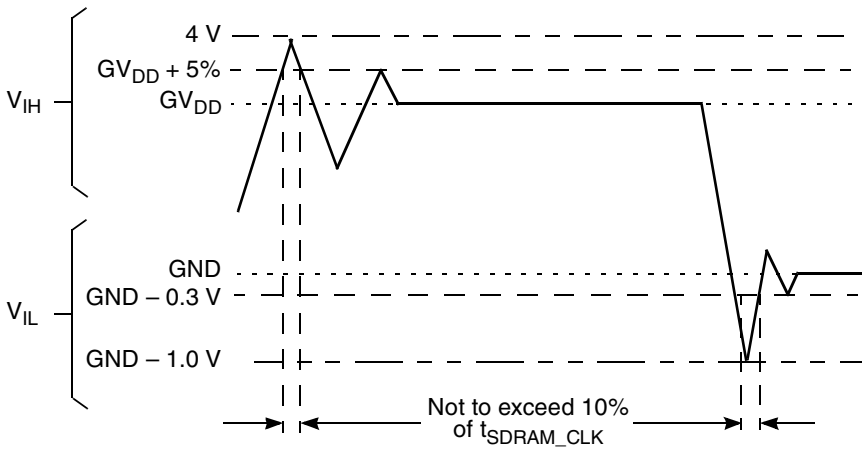


Figure 2. Overshoot/Undershoot Voltage

Table 5. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 6.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/EXT_DBG3/IRQ5/CINT DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5/CINT CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/PCI_RSTINT_OUT/APE PORESET HRESET SRESET RSTCONF	V_{OL}	—	0.4	V

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Table 8. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27[2]
Local bus	45
Memory controller	45 or 27[2]
Parallel I/O	45
PCI	27

1 These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.

2 On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45 Ω.
On all other revisions, impedance value is selected through the SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

This table lists CPM output characteristics.

Table 9. AC Characteristics for CPM Outputs[1]

Spec Number		Characteristic	Value (ns)					
			Maximum Delay			Minimum Delay		
Max	Min		66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	0.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure shows the FCC external clock.

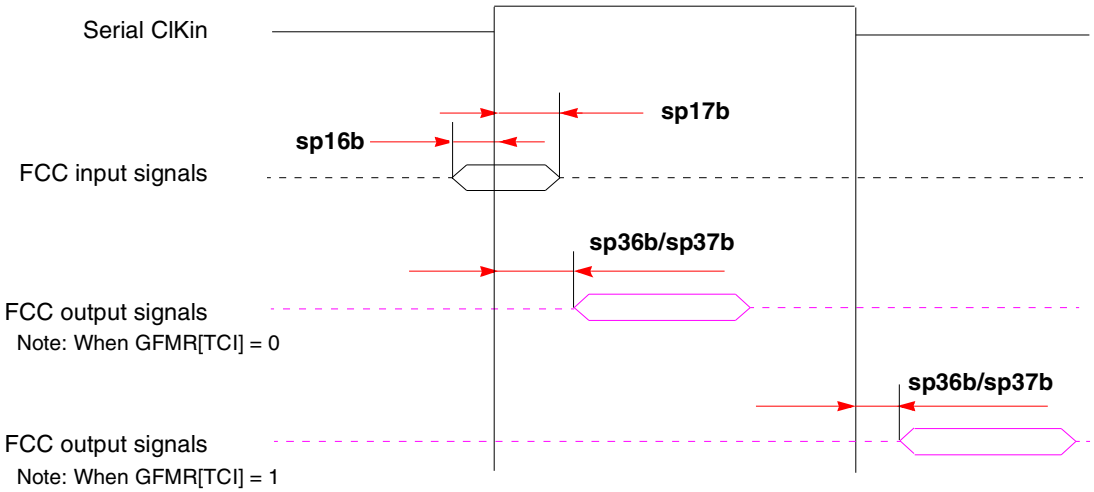
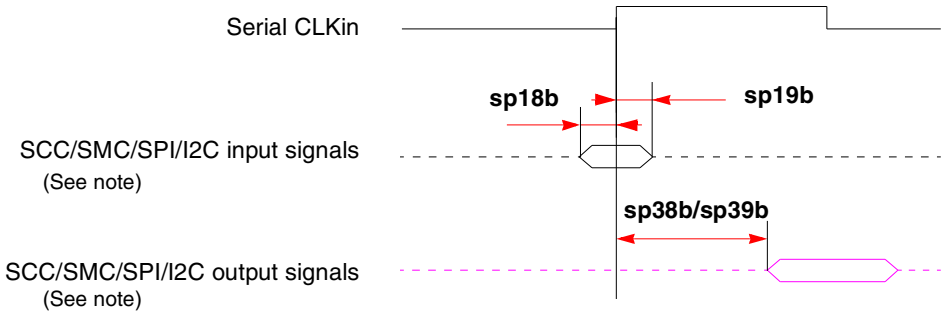


Figure 4. FCC External Clock Diagram

This figure shows the SCC/SMC/SPI/I^2C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^2C External Clock Diagram

NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

Table 11. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Value (ns)							
			Setup				Hold			
Setup	Hold		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp11	sp10	$\overline{AACK}/\overline{TA}/\overline{TS}/\overline{DBG}/\overline{BG}/\overline{BR}/\overline{ARTRY}/\overline{TEA}$	6	5	3.5	N/A	0.5	0.5	0.5	N/A
sp12	sp10	Data bus in normal mode	5	4	3.5	N/A	0.5	0.5	0.5	N/A
sp13	sp10	Data bus in pipeline mode (without ECC and PARITY)	N/A	4	2.5	1.5	N/A	0.5	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	N/A	0.5	0.5	0.5	N/A

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 12. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Value (ns)							
			Maximum Delay				Minimum Delay			
Max	Min		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp31	sp30	$\overline{PSDVAL}/\overline{TEA}/\overline{TA}$	7	6	5.5	N/A	1	1	1	N/A
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	4.5[2]	1	1	1	1 [2]
sp33	sp30	Data bus[3]	6.5	6.5	5.5	4.5	0.8	0.8	0.8	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	4.5	1	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	N/A	1	1	1	N/A

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2 Value is for ADD only; other sp32/sp30 signals are not applicable.
3 To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.

This figure shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

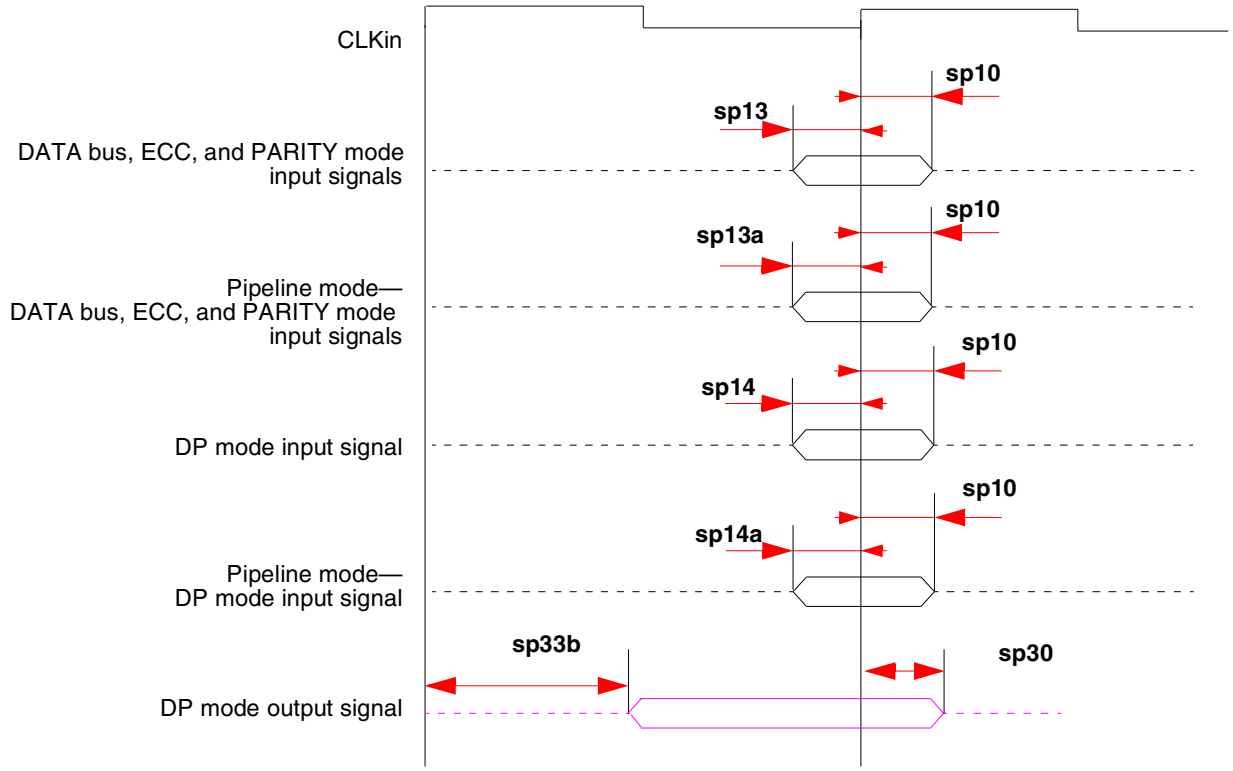


Figure 10. Parity Mode Diagram

This figure shows signal behavior in MEMC mode.

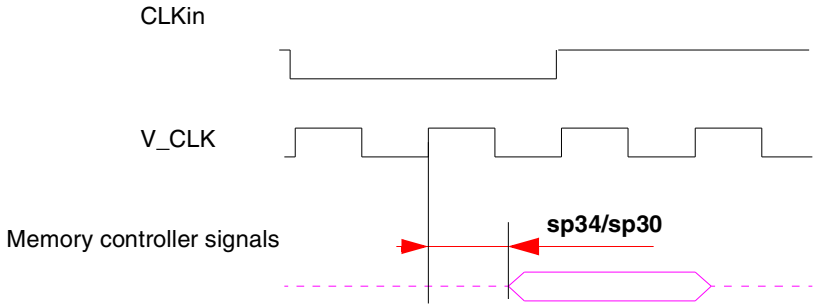


Figure 11. MEMC Mode Diagram

NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 15.

Table 16. JTAG Timings[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Input hold times Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	 ns ns	 4, 7 4, 7
Output valid times Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 — —	 10 10	 ns ns	 5, 7 5, 7
Output hold times Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 1 1	 — —	 ns ns	 5, 7 5, 7
JTAG external clock to output high impedance Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 1 1	 10 10	 ns ns	 5, 6 5, 6

1 All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to t_{TCLK}.

5 Non-JTAG signal output timing with respect to t_{TCLK}.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

7 Clock Configuration Modes

This SoC includes the following clocking modes:

- Local
- PCI host
- PCI agent

The clocking mode is set according to the following input pins as shown in the following table:

- PCI_MODE
- PCI_CFG[0]
- PCI_MODCK

Table 17. SoC Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK[1]			
1	—	—	Local bus	—	Table 18
0	0	0	PCI host	50–66	Table 19
0	0	1		25–50	Table 20
0	1	0	PCI agent	50–66	Table 21
0	1	1		25–50	Table 22

[1] Determines PCI clock frequency range. See Section 7.2, "PCI Host Mode," and Section 7.3, "PCI Agent Mode."

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

7.1 Local Bus Mode

This table lists clock configurations for the SoC in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

Table 18. Clock Configurations for Local Bus Mode[1]

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1:3]	Low	High		Low	High		Low	High
Default Modes (MODCK_H= 0000)								
0000_000	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0000_001	33.3	133.3	3	100.0	400.0	5	166.7	666.7
0000_010	37.5	100.0	4	150.0	400.0	4	150.0	400.0
0000_011	30.0	100.0	4	120.0	400.0	5	150.0	500.0
0000_100	60.0	167.0	2	120.0	334.0	2.5	150.0	417.5
0000_101	50.0	167.0	2	100.0	334.0	3	150.0	501.0
0000_110	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0000_111	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
Full Configuration Modes								
0001_000	50.0	167.0	2	100.0	334.0	4	200.0	668.0

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.
2 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
3 60x and local bus frequency. Identical to CLKIN.
4 CPM multiplication factor = CPM clock/bus clock
5 CPU multiplication factor = Core PLL multiplication factor

7.2 PCI Host Mode

These tables show clock configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI host mode the input clock is the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2]

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0000_011	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0000_100	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0000_101	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_110	50.0	66.7	3.5	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0000_111	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
Full Configuration Modes											
0001_000	50.0	66.7	3	150.0	200.0	5	250.0	333.3	3	50.0	66.7

Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	25.0	50.0	5	125.0	250.0	3.5	218.8	437.5	2	62.5	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev 0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
$\overline{\text{TBST}}$		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
$\overline{\text{AACK}}$		F3
$\overline{\text{ARTRY}}$		E1
$\overline{\text{DBG}}$		V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4
D16		D19
D17		D17

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
CS2		E27
CS3		E28
CS4		F26
CS5		F27
CS6		F28
CS7		G25
CS8		D29
CS9		E29
CS10/BCTL1		F29
CS11/AP0		G28
BADDR27		T5
BADDR28		U1
ALE		T2
BCTL0		A27
PWE0/PSDDQM0/PBS0		C25
PWE1/PSDDQM1/PBS1		E24
PWE2/PSDDQM2/PBS2		D24
PWE3/PSDDQM3/PBS3		C24
PWE4/PSDDQM4/PBS4		B26
PWE5/PSDDQM5/PBS5		A26
PWE6/PSDDQM6/PBS6		B25
PWE7/PSDDQM7/PBS7		A25
PSDA10/PGPL0		E23
PSDWE/PGPL1		B24
POE/PSDRAS/PGPL2		A24
PSDCAS/PGPL3		B23
PGTA/PUPMWAIT/PGPL4/PPBS		A23
PSDAMUX/PGPL5		D22
LWE0/LSDDQM0/LBS0/PCI_CFG0		H28
LWE1/LSDDQM1/LBS1/PCI_CFG1		H27
LWE2/LSDDQM2/LBS2/PCI_CFG2		H26
LWE3/LSDDQM3/LBS3/PCI_CFG3		G29
LSDA10/LGPL0/PCI_MODCKH0		D27

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LCL_D9/AD9		L26
LCL_D10/AD10		L25
LCL_D11/AD11		M29
LCL_D12/AD12		M28
LCL_D13/AD13		M27
LCL_D14/AD14		M26
LCL_D15/AD15		N29
LCL_D16/AD16		T25
LCL_D17/AD17		U27
LCL_D18/AD18		U26
LCL_D19/AD19		U25
LCL_D20/AD20		V29
LCL_D21/AD21		V28
LCL_D22/AD22		V27
LCL_D23/AD23		V26
LCL_D24/AD24		W27
LCL_D25/AD25		W26
LCL_D26/AD26		W25
LCL_D27/AD27		Y29
LCL_D28/AD28		Y28
LCL_D29/AD29		Y25
LCL_D30/AD30		AA29
LCL_D31/AD31		AA28
LCL_DP0/C0/$\overline{\text{BE0}}$		L28
LCL_DP1/C1/$\overline{\text{BE1}}$		N28
LCL_DP2/C2/$\overline{\text{BE2}}$		T28
LCL_DP3/C3/$\overline{\text{BE3}}$		W28
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$		T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$		D1
$\overline{\text{TRST}}$[1]		AH3
TCK		AG5
TMS		AJ3
TDI		AE6

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

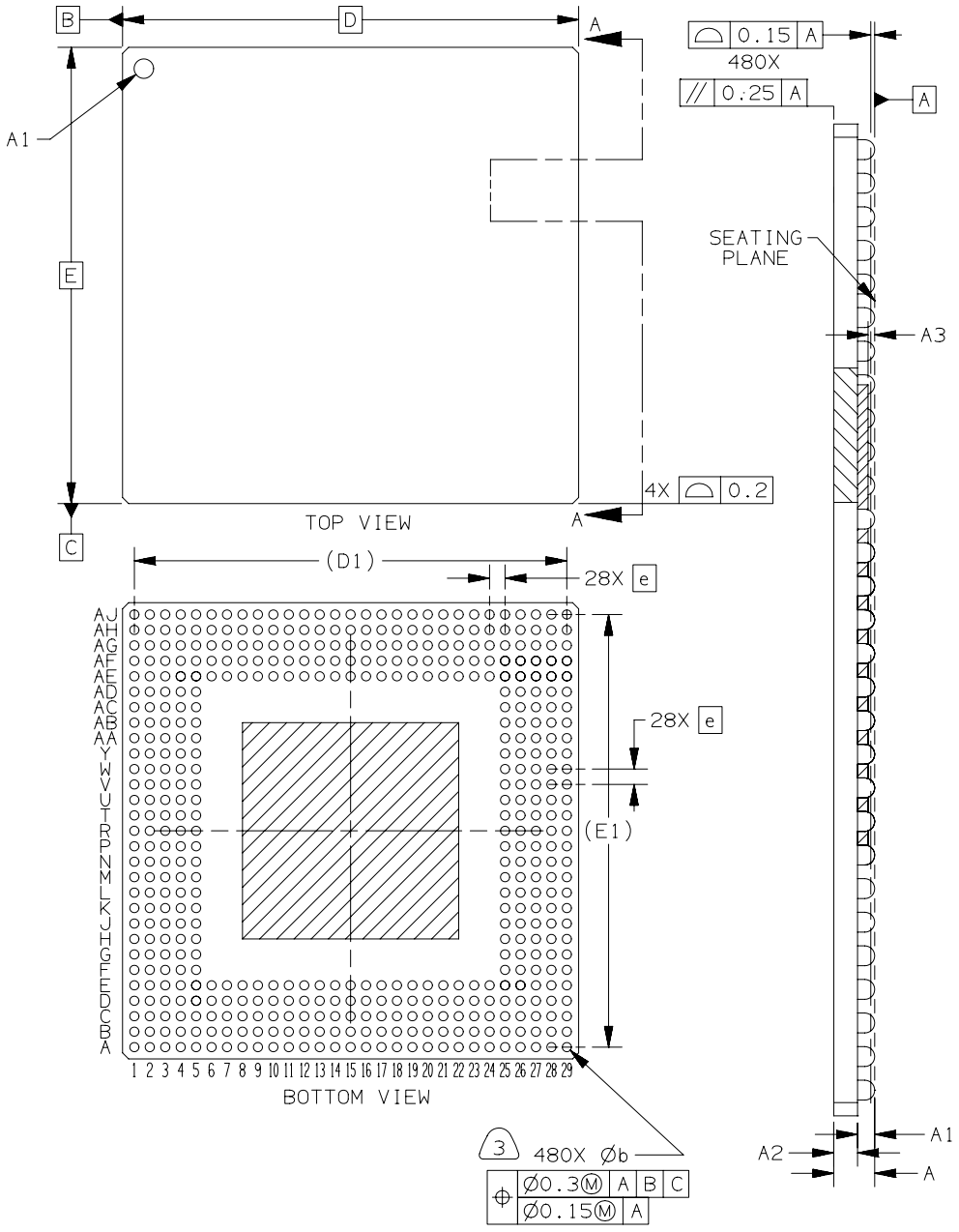
Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
TT1		B3
TT2		F8
TT3		A3
TT4		C3
$\overline{\text{TBST}}$		F5
TSIZ0		E3
TSIZ1		E2
TSIZ2		E1
TSIZ3		E4
$\overline{\text{AACK}}$		D3
$\overline{\text{ARTRY}}$		C2
$\overline{\text{DBG}}$		A14
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$		C15
D0		W4
D1		Y1
D2		V1
D3		P4
D4		N3
D5		K5
D6		J4
D7		G1
D8		AB1
D9		U4
D10		U2
D11		N6
D12		N1
D13		L1
D14		J5
D15		G3
D16		AA2
D17		W1
D18		T3
D19		T1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D53		J2
D54		H5
D55		F3
D56		V3
D57		R5
D58		R2
D59		N5
D60		L2
D61		J3
D62		H1
D63		F4
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$		AB3
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$		W5
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$		AC2
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$		AA3
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$		AD1
$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$		AC1
$\overline{\text{IRQ6}}$/DP6/CSE0		AB2
$\overline{\text{IRQ7}}$/DP7/CSE1		Y3
$\overline{\text{PSDVAL}}$		D15
$\overline{\text{TA}}$		Y4
$\overline{\text{TEA}}$		D16
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		E15
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		D14
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		E14
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$		A17
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		B14
$\overline{\text{CPU\_DBG}}$		F13
$\overline{\text{CPU\_BR}}$		B17
$\overline{\text{CS0}}$		AC6
$\overline{\text{CS1}}$		AD6
$\overline{\text{CS2}}$		AE6
$\overline{\text{CS3}}$		AB7

9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA (ZU/VV) package. See Table 2, “HiP7 PowerQUICC II Device Packages.”



Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls.

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

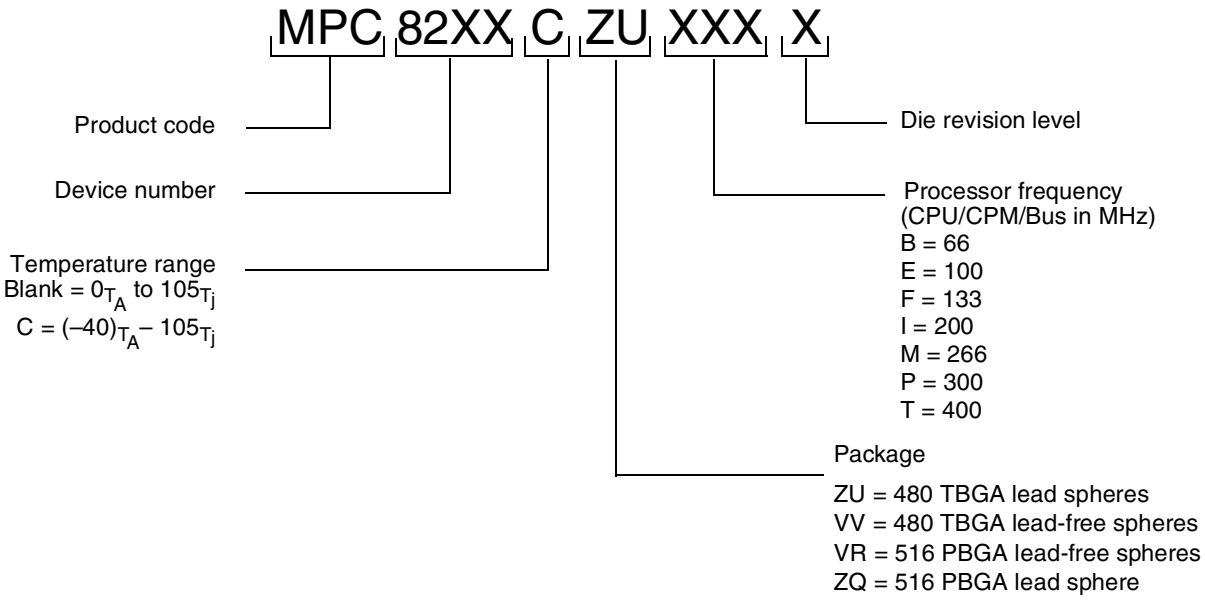


Figure 19. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 27. Document Revision History

Revision	Date	Substantive Changes
2	09/2011	In Figure 19, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
1.8	07/2007	• Updated the entire document, adding information on the VV package.
1.7	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.6	05/2006	• Table 11: Added text to clarify that Data Bus Parity is not supported at 66 Mhz. • Table 11: Added text to clarify that Data Bus ECC is supported at 66 Mhz • Table 11: Added note to DP pins to show it is not supported at 66 MHz • Table 12: Added note to support 1 ns hold time
1.5	03/2006	• Added Section 6.3, “JTAG Timings”

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.0	2/2004	• Removal of “Advance Information” and “Preliminary.” The MPC8280 is fully qualified. • Table 2: New • Figure 1: Modification to note 2 • Section 1.1: Core frequency range is 166–450 MHz • Addition of ZQ (516 PBGA with Lead spheres) package references • Table 4: VDD and VCCSYN modified to 1.45–1.60 V • Note following Table 4: Modified • Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5) • Table 5: Changed I_{OL} for 60x signals to 6.0 mA • Table 5: Moved QREQ to V_{OL}: I_{OL}= 3.2 mA • Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for V_{OL} (I_{OL} = 6.0mA) • Table 10: Addition of Ψ_{JT} and note 4 • Sections 4.1–4.5: New • Table 12: Modified power values (+ 150mW to each) • Table 14: Addition of note 2. Changed PCI impedance to 27 Ω. • Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41 • Table 20: Changes to sp16a, sp18a, sp20 and sp21 • Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle • Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz • Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2. • Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables. • Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6) • Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted. • Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted. • Table 23: Addition of note 5 to ‘No connect’ (AA1, AG4) • Addition of “Note: Temperature Reflow for the VR Package" on page 76 • Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25) • Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins: PA6—FCC2_UT_RXADDR3 PA7—FCC2_UT_TXADDR3 PA8—FCC2_UT_TXADDR4 PB14—RXD3 PC19—SPICLK PC22—FCC1_UT_TXPRTY PC28—FCC2_UT_RXADDR4 • Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1): PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28] • Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted. • Table 25: Addition of note 5 to ‘No connect’ (E17, C23)