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## Understanding Embedded - Microprocessors

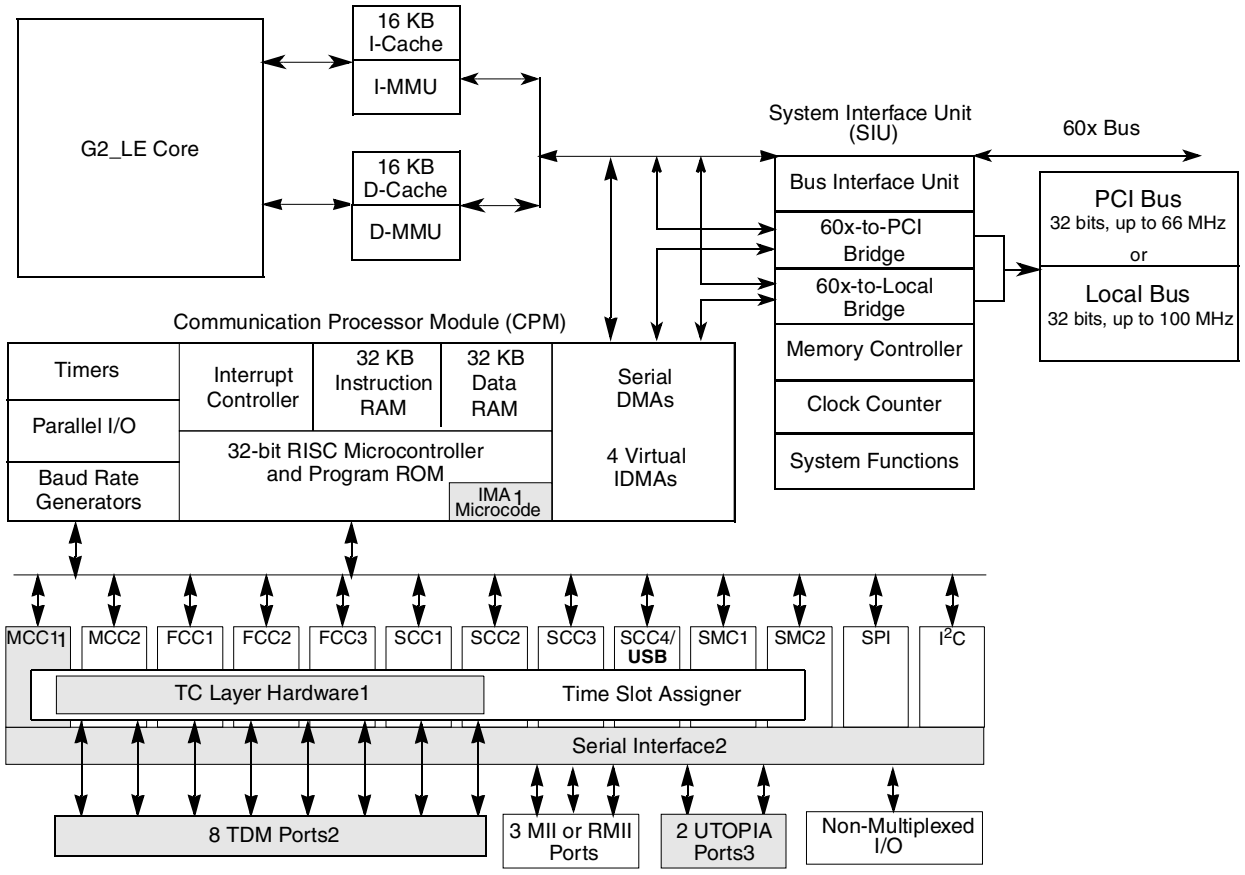
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Number of Cores/Bus Width | - |
| Speed | - |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | - |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | - |
| Operating Temperature | - |
| Security Features | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8280cvvupea |

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.




**Notes:**
[1] MPC8280 only (**not on MPC8270,** the VR package, nor the ZQ package)
[2] MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).
[3] MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270,** MPC8270VR, nor MPC8270ZQ)

**Figure 1. SoC Block Diagram**

## 1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)

  - Common on-chip processor (COP) test interface
  - High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
  - Supports bus snooping
  - Support for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
  - PCI host bridge or peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI

  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
  - Supports the $I_2O$ standard
  - Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66.67/83.33/100 MHz, 3.3 V specification
  - 60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port
  - Uses the local bus signals, removing need for additional pins
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- 12-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x) and byte selects for 32-bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2_LE core through an on-chip 32 KB dual-port data RAM, an on-chip 32 KB dual-port instruction RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)

- ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64 K external connections (no ATM support for the MPC8270)
- Transparent
- HDLC—Up to T3 rates (clear channel)
- FCC2 can also be connected to the TC layer (MPC8280 only)

— Two multichannel controllers (MCCs) (one MCC on the MPC8270)

- Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
- Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC

— Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:

- Ethernet/IEEE 802.3 CDMA/CS
- HDLC/SDLC and HDLC bus
- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Binary synchronous (BISYNC) communications
- Transparent

• Universal serial bus (USB) controller

— Supports USB 2.0 full/low rate compatible

— USB host mode

- Supports control, bulk, interrupt, and isochronous data transfers
- CRC16 generation and checking
- NRZI encoding/decoding with bit stuffing
- Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
- Flexible data buffers with multiple buffers per frame
- Supports local loopback mode for diagnostics (12 Mbps only)

— Supports USB slave mode

- Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
- CRC16 generation and checking
- CRC5 checking
- NRZI encoding/decoding with bit stuffing
- 12- or 1.5-Mbps data rate
- Flexible data buffers with multiple buffers per frame
- Automatic retransmission upon transmit error

— Two serial management controllers (SMCs), identical to those of the MPC860

# 3 DC Electrical Characteristics

This table shows DC electrical characteristics.

**Table 5. DC Electrical Characteristics[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[3] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[3] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V[4] | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[5] (UTOPIA pins only): $I_{OH}$ = -8.0mA<br>PA[0-31]<br>PB[4-31]<br>PC[0-31]<br>PD[4-31] | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[5] (UTOPIA pins only): $I_{OL}$ = 8.0mA<br>PA[0-31]<br>PB[4-31]<br>PC[0-31]<br>PD[4-31] | $V_{OL}$ | — | 0.5 | V |

# 5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

**Table 7. Estimated Power Dissipation for Various Configurations[1]**

| Bus (MHz) | CPM Multiplication Factor | CPM (MHz) | CPU Multiplication Factor | CPU (MHz) | $P_{INT}$(W)[2,3] | |
|---|---|---|---|---|---|---|
| | | | | | Vddl 1.5 Volts | |
| | | | | | Nominal | Maximum |
| 66.67 | 2.5 | 166 | 3.5 | 233 | 0.95 | 1.0 |
| 66.67 | 2.5 | 166 | 4 | 266 | 1.0 | 1.05 |
| 66.67 | 3 | 200 | 4 | 266 | 1.05 | 1.1 |
| 66.67 | 3.5 | 233 | 4.5 | 300 | 1.05 | 1.15 |
| 83.33 | 3 | 250 | 4 | 333 | 1.25 | 1.35 |
| 83.33 | 3 | 250 | 4.5 | 375 | 1.3 | 1.4 |
| 83.33 | 3.5 | 292 | 5 | 417 | 1.45 | 1.55 |
| 100 | 3 | 300 | 4 | 400 | 1.5 | 1.6 |
| 100 | 3 | 300 | 4.5 | 450 | 1.55 | 1.65 |

1 Test temperature = 105° C

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

3 Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.45 W (nominal), 0.5 W (maximum)
83.3 MHz = 0.5W (nominal), 0.6 W (maximum)
100 MHz = 0.6 W (nominal), 0.7 W (maximum)

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 10. AC Characteristics for CPM Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | |
|---|---|---|---|---|---|---|---|---|
| Setup | Hold | | Setup | | | Hold | | |
| | | | 66 MHz | 83 MHz | 100 MHz | 66 MHz | 83 MHz | 100 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 6 | 6 | 6 | 0 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 2.5 | 2.5 | 2.5 | 2 | 2 | 2 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 6 | 6 | 6 | 0 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 4 | 4 | 4 | 2 | 2 | 2 |
| sp20 | sp21 | TDM inputs/SI | 5 | 5 | 5 | 2.5 | 2.5 | 2.5 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 8 | 8 | 8 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

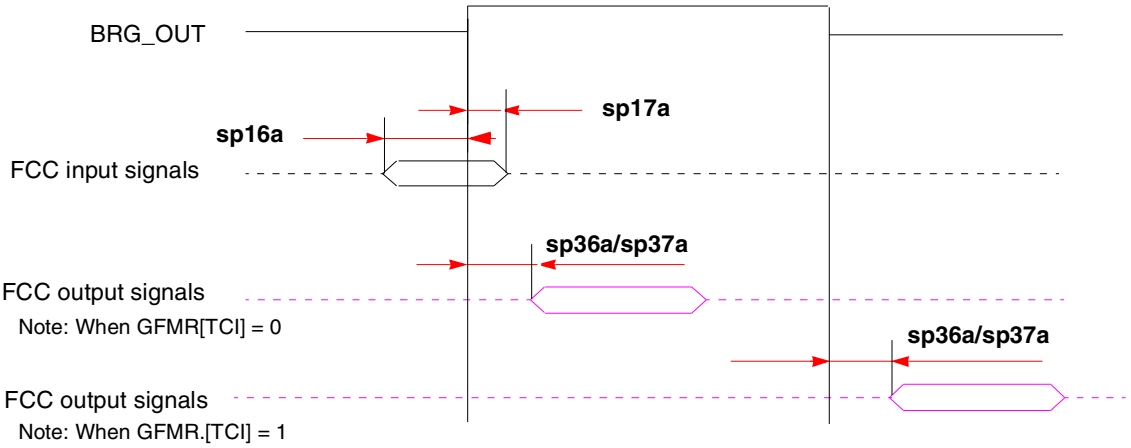
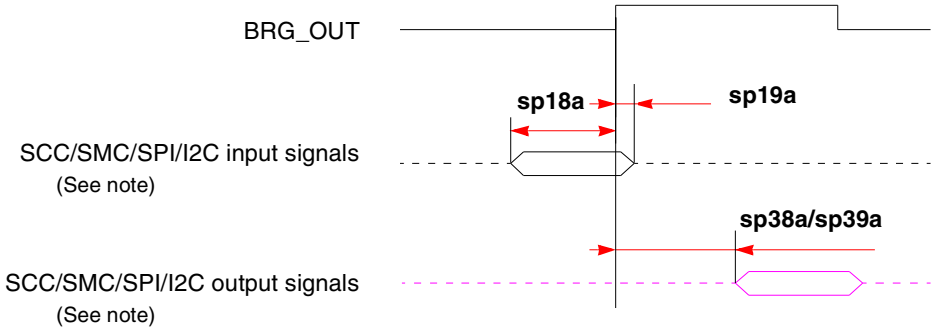



**Figure 3. FCC Internal Clock Diagram**

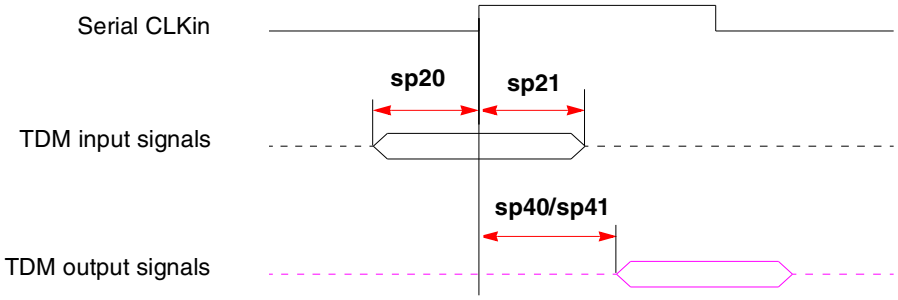
This figure shows the SCC/SMC/SPI/I$^2$C internal clock.




**Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I$^2$C Internal Clock Diagram**

This figure shows TDM input and output signals.




**Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

This figure shows the interaction of several bus signals.

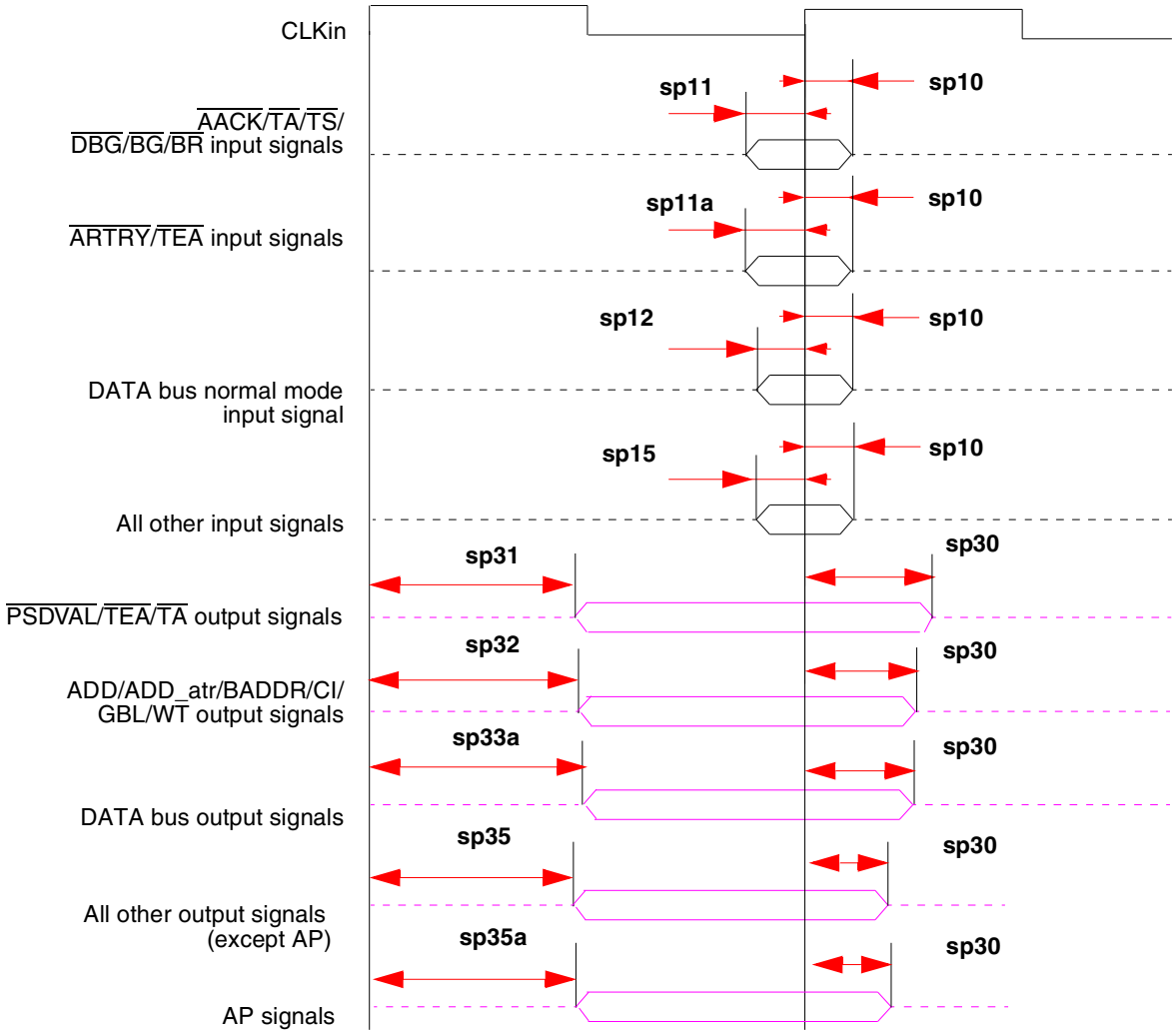



**Figure 9. Bus Signals**

**Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |
| 1011_101 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4.5 | 360.0 | 720.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_000 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |

**Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0100_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 250.0 | 333.3 | 2.5 | 100.0 | 133.3 |
| 0101_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 2.5 | 100.0 | 133.3 |
| 0101_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 2.5 | 100.0 | 133.3 |
| 0101_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 2.5 | 100.0 | 133.3 |
| 0101_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 2.5 | 100.0 | 133.3 |
| 0101_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 2.5 | 100.0 | 133.3 |
| 0101_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 550.0 | 733.3 | 2.5 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 0110_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0110_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 0110_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 0111_000 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 2 | 75.0 | 100.0 |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 2 | 75.0 | 100.0 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 2 | 75.0 | 100.0 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 2 | 75.0 | 100.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 150.0 | 166.7 | 2.5 | 60.0 | 80.0 |
| 1000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 1000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 1000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 1000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| $\overline{ABB}$/$\overline{IRQ2}$ | | E2 |
| $\overline{TS}$ | | E3 |
| A0 | | G1 |
| A1 | | H5 |
| A2 | | H2 |
| A3 | | H1 |
| A4 | | J5 |
| A5 | | J4 |
| A6 | | J3 |
| A7 | | J2 |
| A8 | | J1 |
| A9 | | K4 |
| A10 | | K3 |
| A11 | | K2 |
| A12 | | K1 |
| A13 | | L5 |
| A14 | | L4 |
| A15 | | L3 |
| A16 | | L2 |
| A17 | | L1 |
| A18 | | M5 |
| A19 | | N5 |
| A20 | | N4 |
| A21 | | N3 |
| A22 | | N2 |
| A23 | | N1 |
| A24 | | P4 |
| A25 | | P3 |
| A26 | | P2 |
| A27 | | P1 |
| A28 | | R1 |
| A29 | | R3 |
| A30 | | R5 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| D18 | | D15 |
| D19 | | C13 |
| D20 | | B11 |
| D21 | | A8 |
| D22 | | A5 |
| D23 | | C5 |
| D24 | | C19 |
| D25 | | C17 |
| D26 | | C15 |
| D27 | | D13 |
| D28 | | C11 |
| D29 | | B8 |
| D30 | | A4 |
| D31 | | E6 |
| D32 | | E18 |
| D33 | | B17 |
| D34 | | A15 |
| D35 | | A12 |
| D36 | | D11 |
| D37 | | C8 |
| D38 | | E7 |
| D39 | | A3 |
| D40 | | D18 |
| D41 | | A17 |
| D42 | | A14 |
| D43 | | B12 |
| D44 | | A10 |
| D45 | | D8 |
| D46 | | B6 |
| D47 | | C4 |
| D48 | | C18 |
| D49 | | E16 |
| D50 | | B14 |

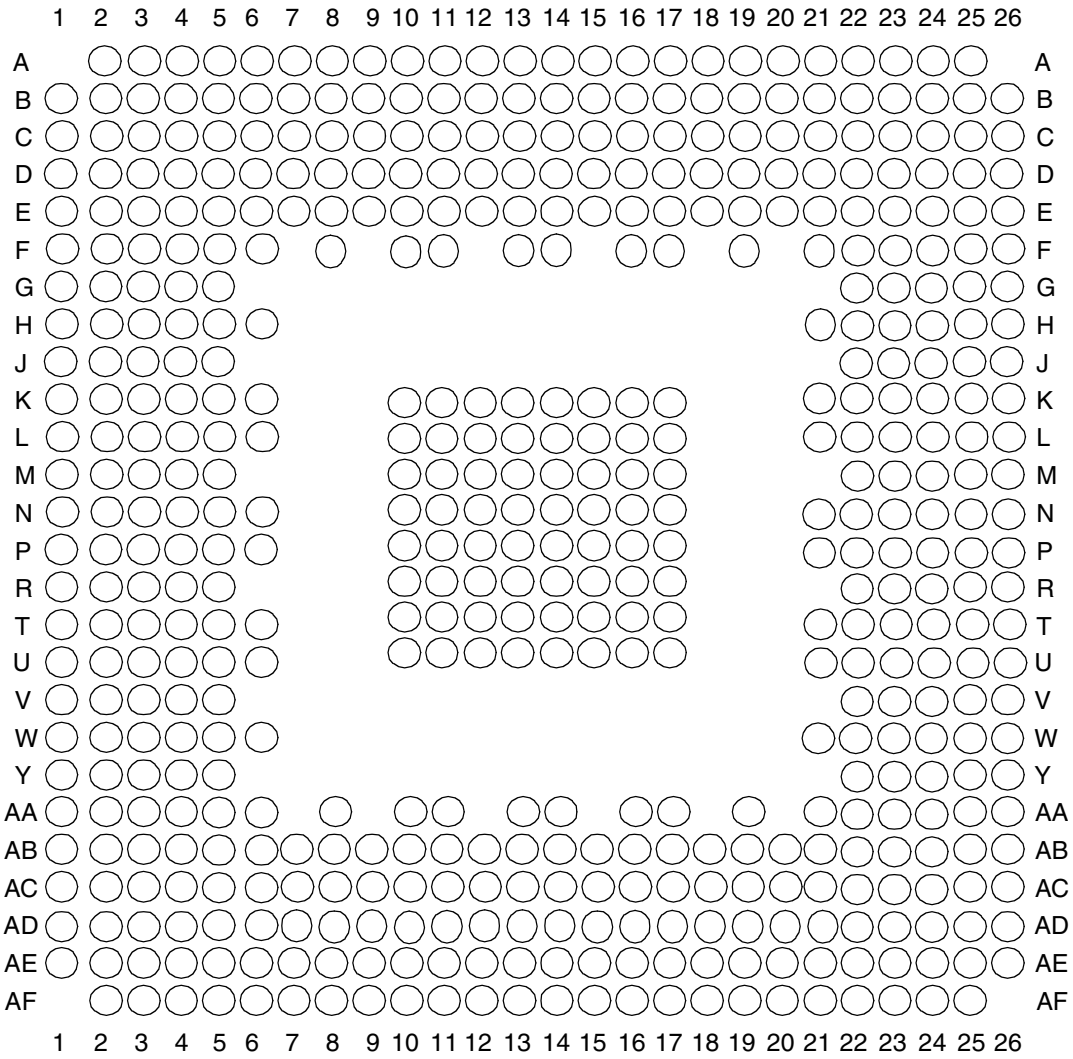
**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| CS2 | | E27 |
| CS3 | | E28 |
| CS4 | | F26 |
| CS5 | | F27 |
| CS6 | | F28 |
| CS7 | | G25 |
| CS8 | | D29 |
| CS9 | | E29 |
| CS10/BCTL1 | | F29 |
| CS11/AP0 | | G28 |
| BADDR27 | | T5 |
| BADDR28 | | U1 |
| ALE | | T2 |
| BCTL0 | | A27 |
| PWE0/PSDDQM0/PBS0 | | C25 |
| PWE1/PSDDQM1/PBS1 | | E24 |
| PWE2/PSDDQM2/PBS2 | | D24 |
| PWE3/PSDDQM3/PBS3 | | C24 |
| PWE4/PSDDQM4/PBS4 | | B26 |
| PWE5/PSDDQM5/PBS5 | | A26 |
| PWE6/PSDDQM6/PBS6 | | B25 |
| PWE7/PSDDQM7/PBS7 | | A25 |
| PSDA10/PGPL0 | | E23 |
| PSDWE/PGPL1 | | B24 |
| POE/PSDRAS/PGPL2 | | A24 |
| PSDCAS/PGPL3 | | B23 |
| PGTA/PUPMWAIT/PGPL4/PPBS | | A23 |
| PSDAMUX/PGPL5 | | D22 |
| LWE0/LSDDQM0/LBS0/PCI_CFG0 | | H28 |
| LWE1/LSDDQM1/LBS1/PCI_CFG1 | | H27 |
| LWE2/LSDDQM2/LBS2/PCI_CFG2 | | H26 |
| LWE3/LSDDQM3/LBS3/PCI_CFG3 | | G29 |
| LSDA10/LGPL0/PCI_MODCKH0 | | D27 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8280/MPC8270** | **MPC8280 only** | |
| PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP | FCC1_UT16_RXD2 | AJ14[2] |
| PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN | FCC1_UT16_RXD3 | AH13[2] |
| PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD | FCC1_UT16_TXD5 | AJ12[2] |
| PD23/RTS3/TENA3 | FCC1_UT16_RXD4/L1RSYNCD1 | AE12[2] |
| PD24/TXD3 | FCC1_UT16_RXD5/L1RXDD1 | AF10[2] |
| PD25/RXD3 | FCC1_UT16_TXD6/L1TXDD1 | AG9[2] |
| PD26/RTS2/TENA2 | FCC1_UT16_RXD6/L1RSYNCC1 | AH8[2] |
| PD27/TXD2 | FCC1_UT16_RXD7/L1RXDC1 | AG7[2] |
| PD28/RXD2 | FCC1_UT16_TXD7/L1TXDC1 | AE4[2] |
| PD29/RTS1/TENA1 | FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1 | AG1[2] |
| PD30/TXD1 | FCC2_UTM_TXENB/ FCC2_UTS_TXENB | AD4[2] |
| PD31/RXD1 | | AD2[2] |
| VCCSYN | | AB3 |
| VCCSYN1 | | B9 |
| CLKIN2 | | AE11 |
| SPARE4[3] | | U5 |
| PCI_MODE[4] | | AF25 |
| SPARE6[3] | | V4 |
| No connect[5] | | AA1, AG4 |
| I/O power | | AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5 |

This figure shows the pinout of the VR and ZQ packages as viewed from the top surface.




Not to Scale

**Figure 14. Pinout of the 516 PBGA Package (View from Top)**

This table shows the pinout list of the MPC8275 and MPC8270. Table 24 defines conventions and acronyms used in Table 25.

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| $\overline{\text{BR}}$ | | C16 |
| $\overline{\text{BG}}$ | | D2 |
| $\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$ | | C1 |
| $\overline{\text{TS}}$ | | D1 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| A0 | | D5 |
| A1 | | E8 |
| A2 | | C4 |
| A3 | | B4 |
| A4 | | A4 |
| A5 | | D7 |
| A6 | | D8 |
| A7 | | C6 |
| A8 | | B5 |
| A9 | | B6 |
| A10 | | C7 |
| A11 | | C8 |
| A12 | | A6 |
| A13 | | D9 |
| A14 | | F11 |
| A15 | | B7 |
| A16 | | B8 |
| A17 | | C9 |
| A18 | | A7 |
| A19 | | B9 |
| A20 | | E11 |
| A21 | | A8 |
| A22 | | D11 |
| A23 | | B10 |
| A24 | | C11 |
| A25 | | A9 |
| A26 | | B11 |
| A27 | | C12 |
| A28 | | D12 |
| A29 | | A10 |
| A30 | | B12 |
| A31 | | B13 |
| TT0 | | E7 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PORESET[2] | | B25 |
| HRESET | | D24 |
| SRESET | | E23 |
| QREQ | | D18 |
| RSTCONF | | E24 |
| MODCK1/AP1/TC0/BNKSEL0 | | B16 |
| MODCK2/AP2/TC1/BNKSEL1 | | F16 |
| MODCK3/AP3/TC2/BNKSEL2 | | A15 |
| CLKIN1 | | G22 |
| PA0/RESTART1/DREQ3 | FCC2_UTM_TXADDR2 | AC20[2] |
| PA1/REJECT1/DONE3 | FCC2_UTM_TXADDR1 | AC21[2] |
| PA2/CLK20/DACK3 | FCC2_UTM_TXADDR0 | AF25[2] |
| PA3/CLK19/DACK4/L1RXD1A2 | FCC2_UTM_RXADDR0 | AE24[2] |
| PA4/REJECT2/DONE4 | FCC2_UTM_RXADDR1 | AA21[2] |
| PA5/RESTART2/DREQ4 | FCC2_UTM_RXADDR2 | AD25[2] |
| PA6 | FCC2_UT_RXADDR3 | AC24[2] |
| PA7/SMSYN2 | FCC2_UT_TXADDR3 | AA22[2] |
| PA8/SMRXD2 | FCC2_UT_TXADDR4 | AA23[2] |
| PA9/SMTXD2 | | Y26[2] |
| PA10/MSNUM5 | FCC1_UT8_RXD0/FCC1_UT16_RXD8 | W22[2] |
| PA11/MSNUM4 | FCC1_UT8_RXD1/FCC1_UT16_RXD9 | W23[2] |
| PA12/MSNUM3 | FCC1_UT8_RXD2/<br>FCC1_UT16_RXD10 | V26[2] |
| PA13/MSNUM2 | FCC1_UT8_RXD3/<br>FCC1_UT16_RXD11 | V25[2] |
| PA14/FCC1_MII_HDLC_RXD3 | FCC1_UT8_RXD4/<br>FCC1_UT16_RXD12 | T22[2] |
| PA15/FCC1_MII_HDLC_RXD2 | /FCC1_UT8_RXD5/<br>FCC1_UT16_RXD13 | T25[2] |
| PA16/FCC1_MII_HDLC_RXD1/<br>FCC1_RMII_RXD1 | FCC1_UT8_RXD6/<br>FCC1_UT16_RXD14 | R24[2] |
| PA17/FCC_MII_HDLC_RXD0/<br>FCC1_MII_TRAN_RXD/<br>FCCI_RMII_RXD0 | FCC1_UT8_RXD7/<br>FCC1_UT16_RXD15 | P22[2] |
| PA18/FCC1_MII_HDLC_TXD0/<br>FCC1_MII_TRAN_TXD/<br>FCC1_RMII_TXD0 | FCC1_UT8_TXD7/FCC1_UT16_TXD15 | N26[2] |

**Table 27. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.0 | 2/2004 | • Removal of “Advance Information” and “Preliminary.” The MPC8280 is fully qualified.<br>• Table 2: New<br>• Figure 1: Modification to note 2<br>• Section 1.1: Core frequency range is 166–450 MHz<br>• Addition of ZQ (516 PBGA with Lead spheres) package references<br>• Table 4: VDD and VCCSYN modified to 1.45–1.60 V<br>• Note following Table 4: Modified<br>• Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5)<br>• Table 5: Changed $I_{OL}$ for 60x signals to 6.0 mA<br>• Table 5: Moved QREQ to $V_{OL}$: $I_{OL}$= 3.2 mA<br>• Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for $V_{OL}$ ($I_{OL}$ = 6.0mA)<br>• Table 10: Addition of $\Psi_{JT}$ and note 4<br>• Sections 4.1–4.5: New<br>• Table 12: Modified power values (+ 150mW to each)<br>• Table 14: Addition of note 2. Changed PCI impedance to 27 Ω.<br>• Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41<br>• Table 20: Changes to sp16a, sp18a, sp20 and sp21<br>• Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle<br>• Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz<br>• Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2.<br>• Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables.<br>• Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6)<br>• Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted.<br>• Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted.<br>• Table 23: Addition of note 5 to ‘No connect’ (AA1, AG4)<br>• Addition of “Note: Temperature Reflow for the VR Package" on page 76<br>• Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25)<br>• Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins:<br>PA6—FCC2_UT_RXADDR3<br>PA7—FCC2_UT_TXADDR3<br>PA8—FCC2_UT_TXADDR4<br>PB14—RXD3<br>PC19—SPICLK<br>PC22—FCC1_UT_TXPRTY<br>PC28—FCC2_UT_RXADDR4<br>• Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1):<br>PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28]<br>• Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted.<br>• Table 25: Addition of note 5 to ‘No connect’ (E17, C23) |

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