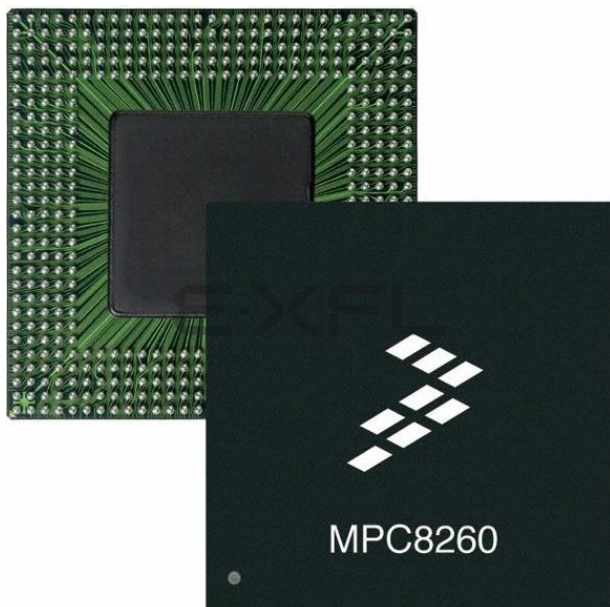




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8280zuqlda

1 Overview

This table shows the functionality supported by each SoC in the MPC8280 family.

Table 1. MPC8280 PowerQUICC II Family Functionality

Functionality	Package ¹	SoCs			
		MPC8270		MPC8275	MPC8280
		480 TBGA	516 PBGA	516 PBGA	480 TBGA
Serial communications controllers (SCCs)		4	4	4	4
QUICC multi-channel controller (QMC)		—	—	—	—
Fast communication controllers (FCCs)		3	3	3	3
I-Cache (Kbyte)		16	16	16	16
D-Cache (Kbyte)		16	16	16	16
Ethernet (10/100)		3	3	3	3
UTOPIA II Ports		0	0	2	2
Multi-channel controllers (MCCs)		1	1	1	2
PCI bridge		Yes	Yes	Yes	Yes
Transmission convergence (TC) layer		—	—	—	Yes
Inverse multiplexing for ATM (IMA)		—	—	—	Yes
Universal serial bus (USB) 2.0 full/low rate		1	1	1	1
Security engine (SEC)		—	—	—	—

¹ See [Table 2](#).

Devices in the MPC8280 family are available in four packages—the standard ZU and VV packages and the alternate VR or ZQ packages—as shown in [Table 2](#). Note that throughout this document, references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Freescale sales office. For package ordering information, see [Section 10, “Ordering Information.”](#)

Table 2. HiP7 PowerQUICC II Device Packages

Code (Package)	ZU (480 TBGA—Leaded)	VV (480 TBGA—Lead Free)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8280	MPC8280	MPC8275VR	MPC8275ZQ
	MPC8270	MPC8270	MPC8270VR	MPC8270ZQ

- Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
- Supports the I₂O standard
- Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)
- Support for 66.67/83.33/100 MHz, 3.3 V specification
- 60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port
- Uses the local bus signals, removing need for additional pins
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE 1149.1 JTAG test access port
- 12-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
 - Byte write enables and selectable parity generation
 - 32-bit address decodes with programmable bank size
 - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
 - Byte selects for 64-bit bus width (60x) and byte selects for 32-bus width (local)
 - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
 - Interfaces to G2_LE core through an on-chip 32 KB dual-port data RAM, an on-chip 32 KB dual-port instruction RAM and DMA controller
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Three fast communications controllers supporting the following protocols:
 - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)

- Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
- Transparent
- UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One I²C controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
 - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
 - 2,048 bytes of SI RAM
 - Bit or byte resolution
 - Independent transmit and receive routing, frame synchronization
 - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers
- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

2 Operating Conditions

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	–0.3 – 2.25	V
PLL supply voltage ²	VCCSYN	–0.3 – 2.25	V
I/O supply voltage ³	VDDH	–0.3 – 4.0	V
Input voltage ⁴	VIN	GND(–0.3) – 3.6	V
Junction temperature	T _j	120	°C
Storage temperature range	T _{STG}	(–55) – (+150)	°C

¹ Absolute maximum ratings are stress ratings only; functional operation (see [Table 4](#)) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

3 DC Electrical Characteristics

This table shows DC electrical characteristics.

Table 5. DC Electrical Characteristics¹

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ ²	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}$ ³	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}$ ³	I_{OZ}	—	10	μA
Signal low input current, $V_{IL} = 0.8 \text{ V}$ ⁴	I_L	—	1	μA
Signal high input current, $V_{IH} = 2.0 \text{ V}$	I_H	—	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except UTOPIA mode, and open drain pins In UTOPIA mode ⁵ (UTOPIA pins only): $I_{OH} = -8.0 \text{ mA}$ PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	—	V
In UTOPIA mode ⁵ (UTOPIA pins only): $I_{OL} = 8.0 \text{ mA}$ PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	—	0.5	V

Table 5. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 6.0\text{mA}$ $\overline{BR}$ $\overline{BG}$ $\overline{ABB}/\overline{IRQ2}$ $\overline{TS}$ $A[0-31]$ $TT[0-4]$ $\overline{TBST}$ $TSIZE[0-3]$ $\overline{AACK}$ $\overline{ARTRY}$ $\overline{DBG}$ $\overline{DBB}/\overline{IRQ3}$ $D[0-63]$ $DP(0)/\overline{RSRV}/\overline{EXT_BR2}$ $DP(1)/\overline{IRQ1}/\overline{EXT_BG2}$ $DP(2)/\overline{TLBISYNC}/\overline{IRQ2}/\overline{EXT_DBG2}$ $DP(3)/\overline{IRQ3}/\overline{EXT_BR3}/\overline{CKSTP_OUT}$ $DP(4)/\overline{IRQ4}/\overline{EXT_BG3}/\overline{CORE_SREST}$ $DP(5)/\overline{TBEN}/\overline{EXT_DBG3}/\overline{IRQ5}/\overline{CINT}$ $DP(6)/\overline{CSE(0)}/\overline{IRQ6}$ $DP(7)/\overline{CSE(1)}/\overline{IRQ7}$ $\overline{PSDVAL}$ $\overline{TA}$ $\overline{TEA}$ $\overline{GBL}/\overline{IRQ1}$ $\overline{CI}/\overline{BADDR29}/\overline{IRQ2}$ $\overline{WT}/\overline{BADDR30}/\overline{IRQ3}$ $\overline{L2_HIT}/\overline{IRQ4}$ $\overline{CPU_BG}/\overline{BADDR31}/\overline{IRQ5}/\overline{CINT}$ $\overline{CPU_DBG}$ $\overline{CPU_BR}$ $\overline{IRQ0}/\overline{NMI_OUT}$ $\overline{IRQ7}/\overline{PCI_RSTINT_OUT}/\overline{APE}$ $\overline{PORESET}$ $\overline{HRESET}$ $\overline{SRESET}$ $\overline{RSTCONF}$	V_{OL}	—	0.4	V

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing.

This table lists SIU input characteristics.

Table 13. AC Characteristics for SIU Inputs¹

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11	sp10	AACK/TA/TS/DBG/BG/BR/ARTRY/TEA	6	5	3.5	0.5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	7	5	3.5	0.5	0.5	0.5
sp13a	sp10	Pipeline mode—Data bus (with or without ECC/PARITY)	5	4	2.5	0.5	0.5	0.5
sp14	sp10	DP pins	7	5	3.5	0.5	0.5	0.5
sp14a	sp10	Pipeline mode—DP pins	—	4	2.5	—	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	0.5	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 14. AC Characteristics for SIU Outputs¹

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31	sp30	PSDVAL/TEA/TA	7	6	5.5	1	1	1
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	1	1	1
sp33a	sp30	Data bus ²	6.5	6.5	5.5	0.7	0.7	0.7
sp33b	sp30	DP	6	5.5	5.5	1	1	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	1	1	1
sp35a	sp30	AP	7	7	7	1	1	1

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

² To achieve 1 ns of hold time at 66, 83, or 100 MHz, a minimum loading of 20 pF is required.

This figure shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

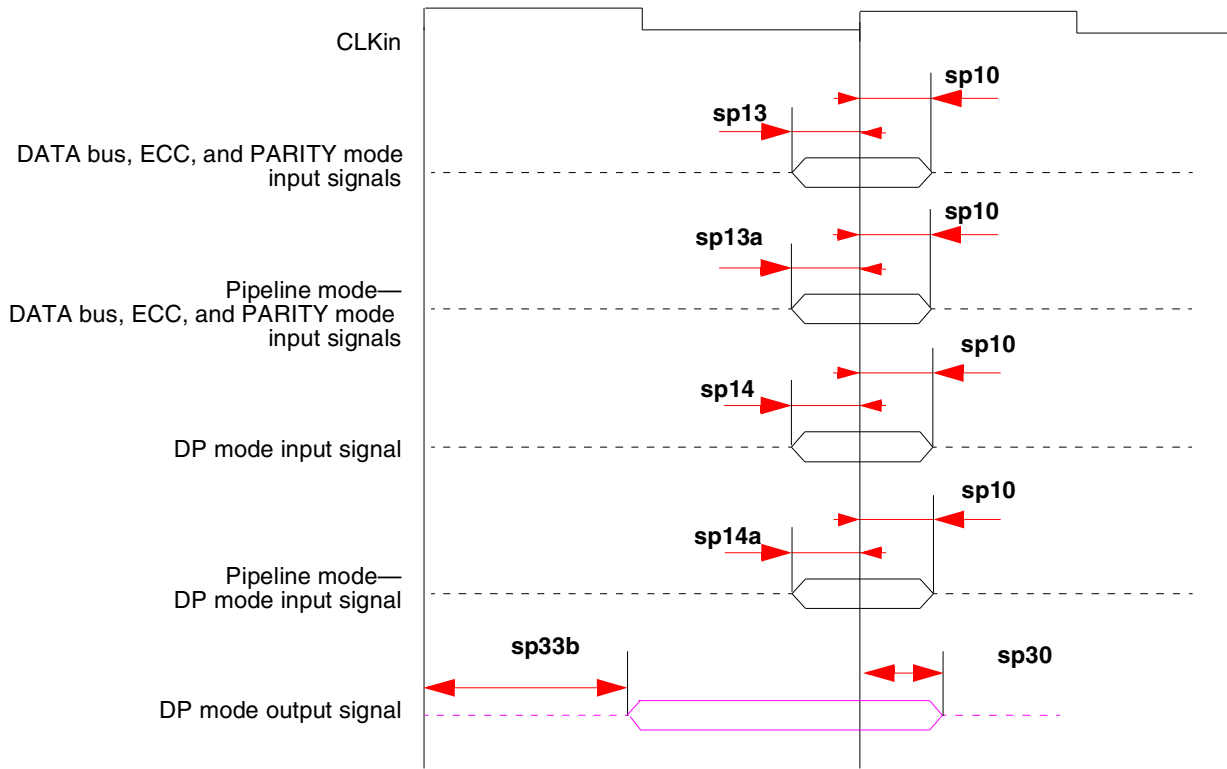


Figure 10. Parity Mode Diagram

This figure shows signal behavior in MEMC mode.

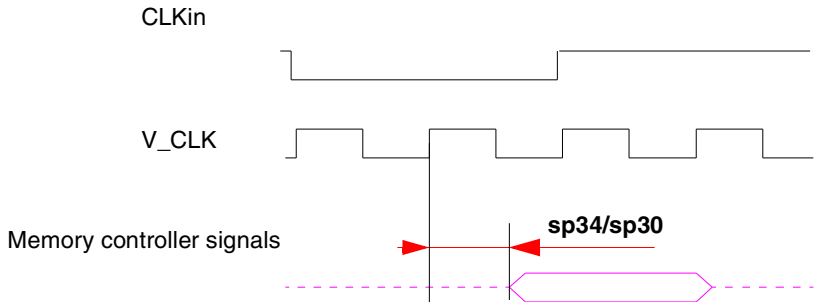


Figure 11. MEMC Mode Diagram

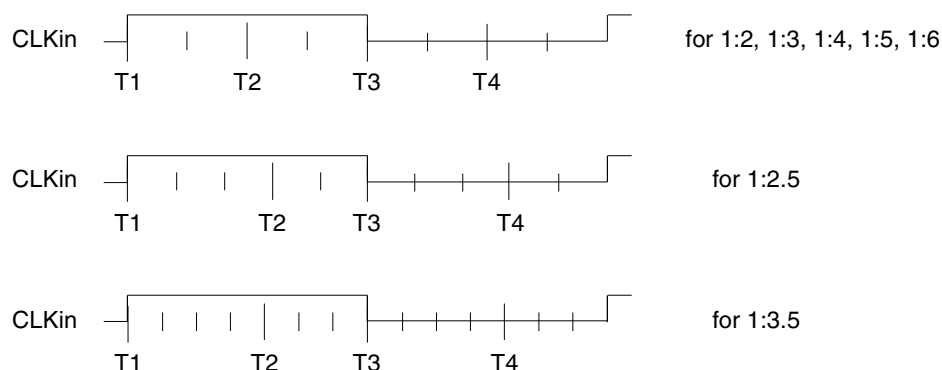
NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in [Table 15](#).

Table 15. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

This table is a representation of the information in [Table 15](#).


Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKIn's rising edge.

6.3 JTAG Timings

This table lists the JTAG timings.

Table 16. JTAG Timings¹

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	⁶
TRST assert time	t_{TRST}	25	—	ns	^{3, 6}
Input setup times Boundary-scan data TMS, TDI	t_{JTDVKH}	4	—	ns	^{4, 7}
	t_{JTIVKH}	4	—	ns	^{4, 7}

Table 18. Clock Configurations for Local Bus Mode¹ (continued)

Mode ²	Bus Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)	
	Low	High		Low	High		Low	High
0110_000	50.0	167.0	2	100.0	334.0	3.5	250.0	584.5
0110_001	50.0	167.0	2	100.0	334.0	4	250.0	668.0
0110_010	50.0	167.0	2	100.0	334.0	4.5	250.0	751.5
0110_011	Reserved							
0110_100	60.0	160.0	2.5	150.0	400.0	2.5	150.0	400.0
0110_101	50.0	160.0	2.5	125.0	400.0	3	150.0	480.0
0110_110	42.9	160.0	2.5	107.1	400.0	3.5	150.0	560.0
0110_111	40.0	160.0	2.5	100.0	400.0	4	160.0	640.0
0111_000	40.0	160.0	2.5	100.0	400.0	4.5	180.0	720.0
0111_001	Reserved							
0111_010	Reserved							
0111_011	50.0	133.3	3	150.0	400.0	3	150.0	400.0
0111_100	42.9	133.3	3	128.6	400.0	3.5	150.0	466.7
0111_101	37.5	133.3	3	112.5	400.0	4	150.0	533.3
0111_110	33.3	133.3	3	100.0	400.0	4.5	150.0	600.0
0111_111	Reserved							
1000_000	Reserved							
1000_001	Reserved							
1000_010	42.9	114.3	3.5	150.0	400.0	3.5	150.0	400.0
1000_011	37.5	114.3	3.5	131.3	400.0	4	150.0	457.1
1000_100	33.3	114.3	3.5	116.7	400.0	4.5	150.0	514.3
1000_101	30.0	114.3	3.5	105.0	400.0	5	150.0	571.4
1000_110	28.6	114.3	3.5	100.0	400.0	5.5	150.0	628.6
1100_000	Reserved							
1100_001	Reserved							
1100_010	Reserved							
1101_000	Reserved							

Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	Bus Clock ⁴ (MHz)		CPM Multiplication Factor ⁵	CPM Clock (MHz)		CPU Multiplication Factor ⁶	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0
1000_010	66.7	133.3	3	200.0	400.0	3.5	233.3	466.7	8	25.0	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	114.3	3.5	200.0	400.0	3.5	200.0	400.0	8	25.0	50.0
1001_011	57.1	114.3	3.5	200.0	400.0	4	228.6	457.1	8	25.0	50.0
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	42.9	85.7	3.5	150.0	300.0	5	214.3	428.6	6	25.0	50.0
1001_110	42.9	85.7	3.5	150.0	300.0	5.5	235.7	471.4	6	25.0	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0

Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2} (continued)

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
MODCK_H-MODCK[1-3]											
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0	266.6	4.5	225.0	300.0	4	50.0	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7

This figure shows the pinout of the ZU and VV packages as viewed from the top surface.

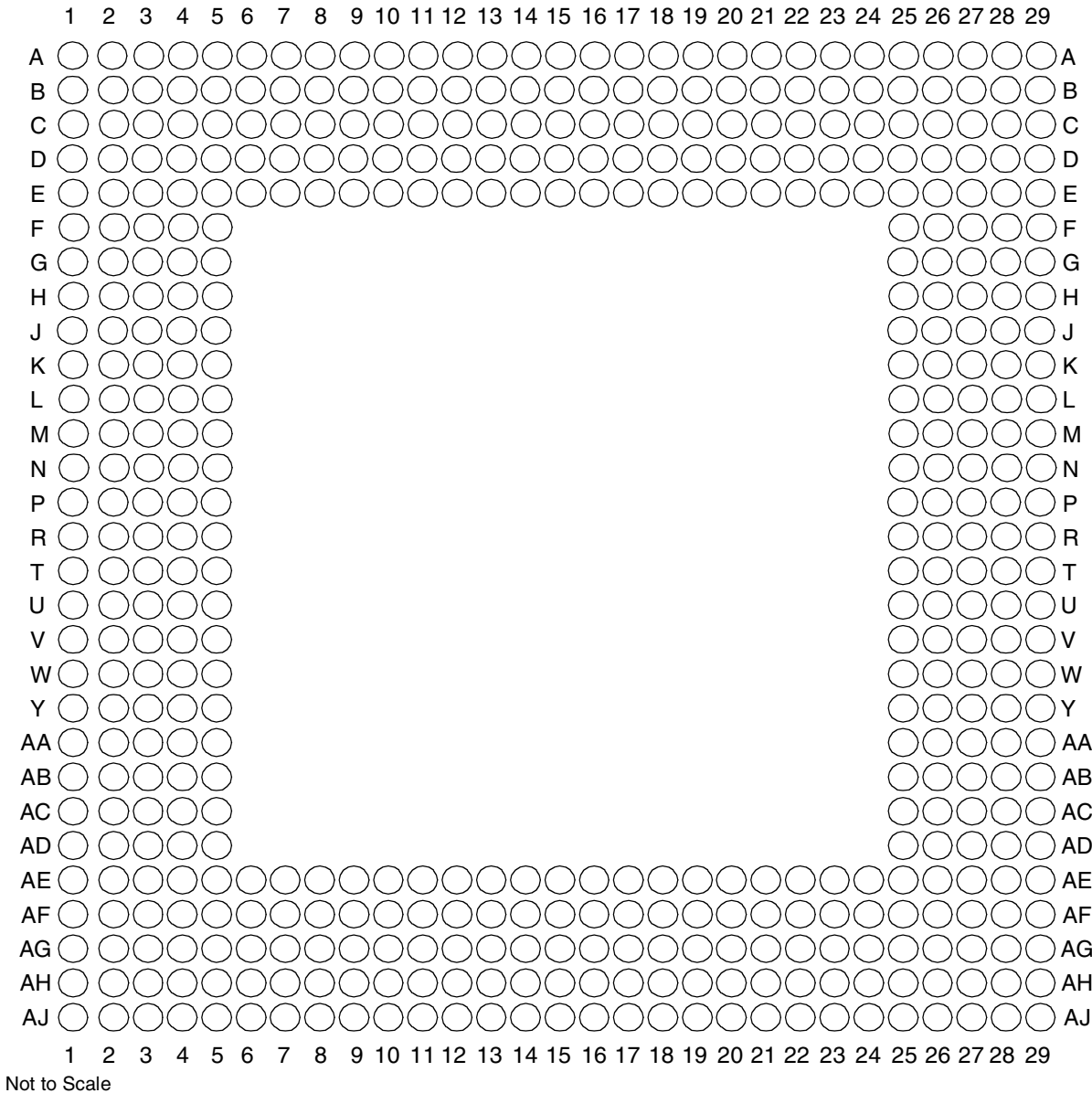


Figure 13. Pinout of the 480 TBGA Package (View from Top)

This table lists the pins of the MPC8280 and MPC8270, and [Table 24](#) defines conventions and acronyms used in this table.

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{\text{BR}}$		W5
$\overline{\text{BG}}$		F4

Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LSDWE/LGPL1/PCI_MODCKH1		C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2		E26
LSDCAS/LGPL3/PCI_MODCKH3		D25
LGTA/LUPMWAIT/LGPL4/LPBS		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
LWR		D28
L_A14/PAR		N27
L_A15/FRAME/SMI		T29
L_A16/TRDY		R27
L_A17/IRDY/CKSTP_OUT		R26
L_A18/STOP		R29
L_A19/DEVSEL		R28
L_A20/IDSEL		W29
L_A21/PERR		P28
L_A22/SERR		N26
L_A23/REQ0		AA27
L_A24/REQ1/HSEJSW		P29
L_A25/GNT0		AA26
L_A26/GNT1/HSLED		N25
L_A27/GNT2/HSENUM		AA25
L_A28/RST/CORE_SRESET		AB29
L_A29/INTA		AB28
L_A30/REQ2		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
TT1		B3
TT2		F8
TT3		A3
TT4		C3
$\overline{\text{TBST}}$		F5
TSIZ0		E3
TSIZ1		E2
TSIZ2		E1
TSIZ3		E4
$\overline{\text{AACK}}$		D3
$\overline{\text{ARTRY}}$		C2
$\overline{\text{DBG}}$		A14
$\overline{\text{DBB/IRQ3}}$		C15
D0		W4
D1		Y1
D2		V1
D3		P4
D4		N3
D5		K5
D6		J4
D7		G1
D8		AB1
D9		U4
D10		U2
D11		N6
D12		N1
D13		L1
D14		J5
D15		G3
D16		AA2
D17		W1
D18		T3
D19		T1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D20		M2
D21		K2
D22		J1
D23		G4
D24		U5
D25		T5
D26		P5
D27		P3
D28		M3
D29		K3
D30		H2
D31		G5
D32		AA1
D33		V2
D34		U1
D35		P2
D36		M4
D37		K4
D38		H3
D39		F2
D40		Y2
D41		U3
D42		T2
D43		N2
D44		M5
D45		K1
D46		H4
D47		F1
D48		W2
D49		T4
D50		R3
D51		N4
D52		M1

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PB15/FCC3_MII_TX_ER/RXD2		U24 ²
PB16/FCC3_MII_RMII_RX_ER/CLK18		R22 ²
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV		R23 ²
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	M23 ²
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	L24 ²
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6	K24 ²
PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7	L21 ²
PB22/FCC2_MII_HDLC_RMII_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7	P25 ²
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6	N25 ²
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5	E26 ²
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4	H23 ²
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	C26 ²
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	B26 ²
PB28/FCC2_MII_RX_ER/FCC2_RMII_RX_ER/ FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1		A22 ²
PB29/L1RSYNCB2/ FCC2_MII_TX_EN/FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	A21 ²
PB30/FCC2_MII_RX_DV/L1RXDB2/ FCC2_RMII_CRS_DV	FCC2_UT_TXSOC	E20 ²
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	C20 ²
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AE22 ²
PC1/DREQ2/SPISEL/BRGO6/L1RQA2		AA19 ²
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AF24 ²
PC3/FCC3_CTS/DACK2/CTS4/ USB_RP	FCC2_UT8_TXD2	AE25 ²
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AB22 ²

Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)

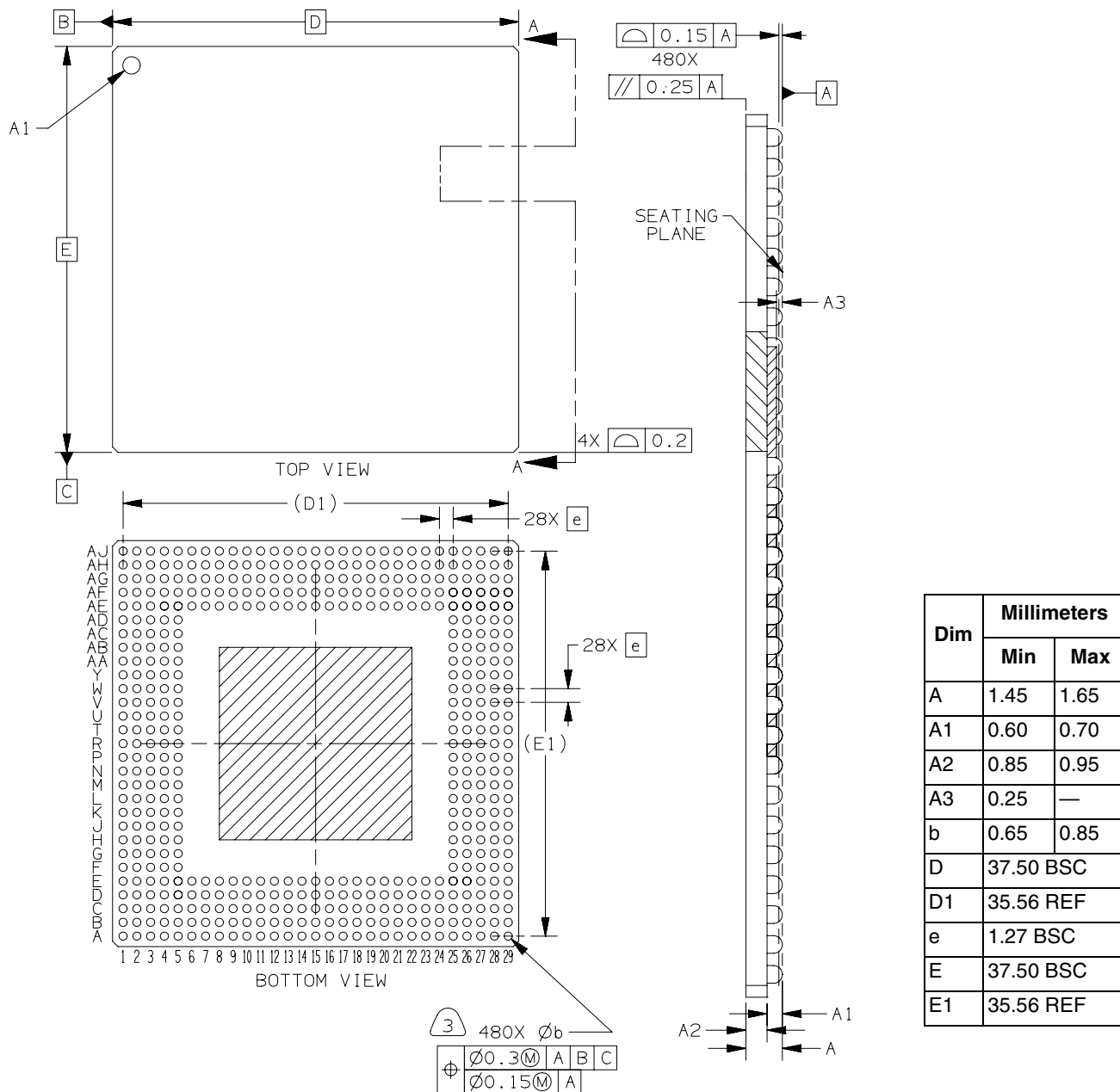
Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PD27/TXD2	FCC1_UT16_RXD7	H22 ²
PD28/RXD2	FCC1_UT16_TXD7	B22 ²
PD29/RTS1/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	D22 ²
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	C21 ²
PD31/RXD1		E19 ²
VCCSYN		D19
VCCSYN1		K6
CLKIN2		K21
SPARE4 ³		C14
PCI_MODE ⁴		AD24
SPARE6 ³		B15
No connect ⁵		E17, C23
I/O power		E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9
Core Power		L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground		B18 ⁶ , A18 ⁷ , A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

¹ Should be tied to VDDH via a 2K Ω external pull-up resistor.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA (ZU/VV) package. See Table 2, “HiP7 PowerQUICC II Device Packages.”



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls.

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
1.0	2/2004	- Removal of "Advance Information" and "Preliminary." The MPC8280 is fully qualified. - Table 2: New - Figure 1: Modification to note 2 - Section 1.1: Core frequency range is 166–450 MHz - Addition of ZQ (516 PBGA with Lead spheres) package references - Table 4: VDD and VCCSYN modified to 1.45–1.60 V - Note following Table 4: Modified - Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5) - Table 5: Changed I_{OL} for 60x signals to 6.0 mA - Table 5: Moved QREQ to V_{OL}: $I_{OL} = 3.2$ mA - Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for V_{OL} ($I_{OL} = 6.0$ mA) - Table 10: Addition of Ψ_{JT} and note 4 - Sections 4.1–4.5: New - Table 12: Modified power values (+ 150mW to each) - Table 14: Addition of note 2. Changed PCI impedance to 27 Ω. - Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41 - Table 20: Changes to sp16a, sp18a, sp20 and sp21 - Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle - Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz - Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2. - Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables. - Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6) - Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted. - Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted. - Table 23: Addition of note 5 to 'No connect' (AA1, AG4) - Addition of "Note: Temperature Reflow for the VR Package" on page 76 - Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25) - Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins: PA6—FCC2_UT_RXADDR3 PA7—FCC2_UT_TXADDR3 PA8—FCC2_UT_TXADDR4 PB14—RXD3 PC19—SPICLK PC22—FCC1_UT_TXPRTY PC28—FCC2_UT_RXADDR4 - Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1): PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28] - Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted. - Table 25: Addition of note 5 to 'No connect' (E17, C23)

Table 27. Document Revision History (continued)

Revision	Date	Substantive Changes
0.3	6/2003	- Removal of notes stating “no local bus” on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support. - References to “G2 core” changed to “G2_LE core.” See the <i>G2 Core Reference Manual</i> (G2CORERM/D). - Addition of VCCSYN to “Note” below Table 4, and to note 3 of Table 5 Figure 2: New Table 5: Addition of note 1 Table 10: Addition of θ_{JB} and θ_{JC}. Modifications to ZU package values. Table 12: Addition of various configurations, Modification of values. Addition of note 3. Table 9: Addition of 66 MHZ and 100 MHz values. Addition of sp42a/sp43a. Table 20: Addition of 66 MHZ and 100 MHz values Table 12: sp30 values. sp33b @100 MHz value. Removal of previous note 2. Modification of current note 2. Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes - Section 6.2: Addition of note on PCI timing Table 18, Table 32, Table 33, Table 36, Table 37: Addition of note 1 concerning minimum operating frequencies - Addition of statement before clock tables about selection of clock configuration and input frequency Table 23 and Table 25: Addition of note 1 to CPM pins
0.2	11/2002	Table 25 , “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 63)
0.1	—	Initial public release